

## Active Errata List

- USB – Ping-Pong databank 1 Re-transmission Failure
- USB – Ping-Pong OUT Bad Reception
- USB – Bad Remote Wake-up Generation
- UART Interface – During Reception, Clearing REN may Generate Unexpected IT
- C51 Core – Power-down Exit Failure in X2 Mode
- Timer 0/1 – Unexpected Interrupt
- USB Interface – CPU Wake-up Interrupt not Cleared if CPU Frequency Greater or Equal than 12 MHz/X2
- USB Interface – Data Corruption in Endpoint0 and FIFO
- Timer 2 – Baud Rate Generator – Long Start Time
- Timer 1 in Mode 1 Does Not Generate Baud Rate to UART
- Wrong Latch of Hardware Conditions
- Bad Suspend Resume Initialization
- Stretch MOVX Does Not Work

## Errata History

Lot Number	Errata List
A5560 or above	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13,14

## Errata Description

### 1. USB – Ping-Pong Databank 1 Re-transmission Failure

When the host does not acknowledge an IN data packet from the databank 1 of a ping-pong endpoint, the endpoint retry-mechanism sends corrupted data.

#### Workaround

None.

### 2. USB - Ping-Pong OUT Bad Reception

When the host sends a packet with a size lower than the size defined in the DPRAM endpoint (Ping-Pong Only), there is a risk of having a corrupted packet in the DPRAM with a wrong number of bytes reported. This problem occurs only in Ping-Pong mode if the 2 banks are full and bank 1 is cleared when the host is sending a packet at that time. If the packets are of the size of the DPRAM endpoint, there is no problem even in Ping-Pong mode.

If the device application software is quick enough to read the received packets to avoid the case where the 2 banks are full, there is no problem even if the packet sizes are not of the same size of the DPRAM endpoint.

#### Workaround

None.

### 3. USB - Bad Remote Wake-up Generation

The remote wake-up generates an SE0 and J state (at the end of the Upstream Resume K) that are reserved by the Host.

#### Workaround

None.

### 4. UART Interface – During Reception, Clearing REN may Generate Unexpected IT



## USB Microcontrollers

## AT89C5131

## Errata Sheet



During UART reception, if the REN bit is cleared between start bit detection and the end of reception, the UART will not discard the data (RI is set).

**Workaround**

Test REN bit at the beginning of interrupt routine just after CLR RI, and run the Interrupt routine code only if REN is set.

**5. C51 Core – Power-down Exit Failure in X2 Mode**

If CPU is configured in X2 mode when exiting from power down, the first address fetched may be lost

**Workaround** Two solutions are possible:

- a) Set CPU in X1 mode before entering in power-down mode and then restore CPU to X2 mode when the CPU is woken up.
- b) Add a NOP (0x00) opcode just after the instruction which activates the power down mode. As this NOP is randomly non executed, the behavior of the software is correct.

Example:

```
MOV PCON, #02H; Power down mode activation
NOP      ; This NOP is randomly not executed
.....  ; Put here the first opcode to execute after exiting from power down mode
```

**6. Timer 0/1 – Unexpected Interrupt**

If one of the timers 0 and 1 is in X1 mode while the other one is in X2 mode, an unexpected interrupt may randomly occur for one of the timers.

**Workaround**

Use the same mode X1 or X2 for both timers. This condition is met if PLL is used to clock the CPU.

**7. USB Interface – CPU Wake-up Interrupt Not Cleared if CPU Frequency Greater or Equal to 12 Mhz/X2**

The WUPCPU bit in USBINT register is set by the hardware when the USB macro exits from suspend mode. The firmware acknowledges this event by clearing the WUPCPU bit in the interrupt routine. If the CPU frequency is greater or equal to 12 MHz/X2, the WUPCPU bit is cleared in the USBINT register but not in the USB macro. Therefore the next time the USB macro exits from suspend mode, the WUPCPU bit is not set by the hardware and the CPU fails to exit from the power down mode.

**Workaround**

None

**8. USB Interface – Data Corruption in Endpoint0 and FIFO**

Data in Control Endpoint and FIFO may be corrupted if USB macro and CPU write simultaneously in. This condition occurs if the host cancels a control IN transaction with premature OUT and sends the following SETUP while the C51 is writing into the FIFO instead of the cancellation.

**Workaround:** There are two ways to avoid this problem.

- a) Use 32 bytes FIFO
- b) Test NAKIN and NAKOUT bits to know which way the communication is performed. Once the data has been transferred, the firmware clears the TXCMPL bit and the NAKIN bit. If the NAKIN bit is set by the hardware, this means that the host asks for more data. If the RXOUT bit is set by the hardware, this means that the host has already sent the status stage and no longer asks for data.

**9. Timer 2 – Baud Rate Generator – Long Start Time**

When Timer 2 is used as a baud rate generator, TH2 is not loaded with RCAP2H at the beginning, then UART is not operational before 10,000 machine cycles.

**Workaround**

Add the initialization of TH2 and TL2 in the initialization of Timer 2.

## 10. Timer 1 in Mode 1 Does Not Generate Baud Rate to UART

Timer 1, when used as a baud rate generator in Mode 1 (16 bits counter) for low baud rates, does not generate baud rate to UART.

### Workaround

None.

## 11. Flash/EEPROM – First Read after Load Disturbed

In the 'In-Application Programming' mode from the Flash, if the User software application loads the Column Latch Area prior to calling the programming sequence in the USB Bootloader.

The 'Read after load' issue leads to a wrong Opcode Fetch during the column latch load sequence.

### Workaround

Update of the Flash API Library. A NOP instruction has to be inserted after the load instruction.

```
MOVX @DPTR,A ;Load Column latches
NOP ; ADDED INSTRUCTION
```

## 12. Wrong Latch of Hardware Conditions

If the Reset input is controlled externally and is not synchronous with internal clock, the Hardware Conditions could be latched in the wrong status. These hardware conditions are used in the boot process and the device may not boot in the right target (Bootloader or Application)

### Workaround

If an asynchronous Reset is mandatory to reset the device, Atmel can offer a solution with a customized Bootloader. In this case, please fill a request on our Web site. We will provide you the best solution adapted to your constraints.

## 13. Bad Suspend Resume Initialization

Sometimes and randomly when the USB device is plugged to the USB interface, it may not enumerate properly. It appears that the device remains in suspend state.

### Workaround

After enabling the USB macro by means of bit USBE bit in USBCON, it is necessary to clear just after the bit WUPCPU in USBINT register

## 14. Stretch MOVX Does Not Work

When setting M0 bit in AUXR SFR (08Eh), the RD or WR pulse on a MOVX instruction on external memory is not 30 XTAL length but always standard 6 XTAL length. Thus slow external peripherals mapping in the XDATA space could not work properly.

### Workaround

None.

## Active USB Bootloader Errata List

- Start Application - Start Application With Reset Occurs Before the End of the Command
- LPC security - SSB Not Read at Startup

## USB Bootloader Errata History

Version Number	Errata List
1.0.2	1,2
1.0.3	

## USB Bootloader Errata Description

### 1. Start Application - Start Application With Reset Occurs Before the End of the Command

When receiving a Start application with reset command, the bootloader launches a reset before receiving a DFU command with no byte.

### 2. LPC security - SSB Not Read at Startup

The SSB value is not read at startup. The part can be read or written even if the security has been set.



## Headquarters

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**Atmel Corporation**  
2325 Orchard Parkway  
San Jose, CA 95131  
USA  
Tel: 1(408) 441-0311  
Fax: 1(408) 487-2600

## International

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**Atmel Asia**  
Room 1219  
Chinachem Golden Plaza  
77 Mody Road Tsimshatsui  
East Kowloon  
Hong Kong  
Tel: (852) 2721-9778  
Fax: (852) 2722-1369

**Atmel Europe**  
Le Krebs  
8, Rue Jean-Pierre Timbaud  
BP 309  
78054 Saint-Quentin-en-  
Yvelines Cedex  
France  
Tel: (33) 1-30-60-70-00  
Fax: (33) 1-30-60-71-11

**Atmel Japan**  
9F, Tonetsu Shinkawa Bldg.  
1-24-8 Shinkawa  
Chuo-ku, Tokyo 104-0033  
Japan  
Tel: (81) 3-3523-3551  
Fax: (81) 3-3523-7581

## Product Contact

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