

# Z0103NA0

## 4Q Triac

Rev. 02 — 21 March 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Planar passivated very sensitive gate four quadrant triac in a SOT54 (TO-92) plastic package intended for use in applications requiring enhanced noise immunity and direct interfacing to logic ICs and low power gate drivers.

### 1.2 Features and benefits

- Direct interfacing to logic level ICs
- Enhanced current surge capability
- Enhanced noise immunity
- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Triggering in all four quadrants
- Very sensitive gate in four quadrants

### 1.3 Applications

- General purpose low power motor control
- Home appliances
- Industrial process control
- Low power AC Fan controllers

### 1.4 Quick reference data

Table 1. Quick reference data

| Symbol              | Parameter                            | Conditions  | Min | Typ | Max  | Unit |
|---------------------|--------------------------------------|---|-----|-----|------|------|
| $V_{\text{DRM}}$    | repetitive peak off-state voltage    |   | -   | -   | 800  | V    |
| $I_{\text{TSM}}$    | non-repetitive peak on-state current | full sine wave; $T_{\text{j(init)}} = 25\text{ °C}$ ; $t_{\text{p}} = 20\text{ ms}$ ; see <a href="#">Figure 4</a> ; see <a href="#">Figure 5</a> | -   | -   | 12.5 | A    |
| $I_{\text{T(RMS)}}$ | RMS on-state current                 | full sine wave; $T_{\text{lead}} \leq 45\text{ °C}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a> ; see <a href="#">Figure 2</a>  | -   | -   | 1    | A    |

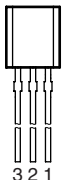
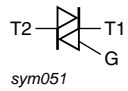


Table 1. Quick reference data ...continued

| Symbol                        | Parameter            | Conditions   | Min | Typ | Max | Unit |
|-------------------------------|----------------------|--|-----|-----|-----|------|
| <b>Static characteristics</b> |                      |  |     |     |     |      |
| $I_{GT}$                      | gate trigger current | $V_D = 12\text{ V}; I_T = 0.1\text{ A}; T2+ G+;$<br>$T_j = 25\text{ }^\circ\text{C};$ see <a href="#">Figure 7</a> | 0.2 | -   | 3   | mA   |
|                               |                      | $V_D = 12\text{ V}; I_T = 0.1\text{ A}; T2+ G-;$<br>$T_j = 25\text{ }^\circ\text{C};$ see <a href="#">Figure 7</a> | 0.2 | -   | 3   | mA   |
|                               |                      | $V_D = 12\text{ V}; I_T = 0.1\text{ A}; T2- G-;$<br>$T_j = 25\text{ }^\circ\text{C};$ see <a href="#">Figure 7</a> | 0.2 | -   | 3   | mA   |
|                               |                      | $V_D = 12\text{ V}; I_T = 0.1\text{ A}; T2- G+;$<br>$T_j = 25\text{ }^\circ\text{C};$ see <a href="#">Figure 7</a> | 0.2 | -   | 5   | mA   |

## 2. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description     | Simplified outline   | Graphic symbol   |
|-----|--------|-----------------|--|--|
| 1   | T2     | main terminal 2 |  | <br>sym051 |
| 2   | G      | gate            |  |  |
| 3   | T1     | main terminal 1 |  |  |

**SOT54 (TO-92)**

## 3. Ordering information

Table 3. Ordering information

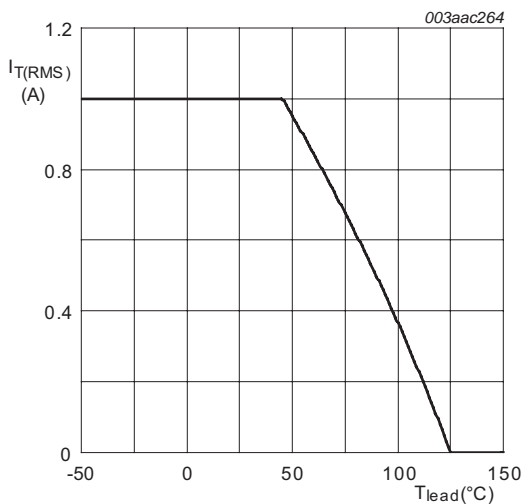
| Type number | Package |   |         |
|-------------|---------|---|---------|
|             | Name    | Description   | Version |
| Z0103NA0    | TO-92   | plastic single-ended leaded (through hole) package; 3 leads | SOT54   |

### 4. Limiting values

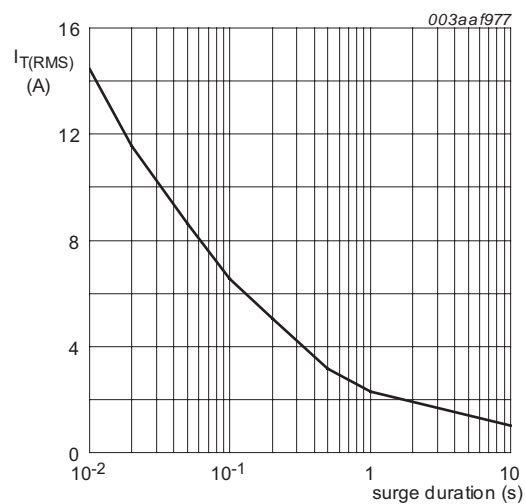
**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol       | Parameter                            | Conditions  | Min | Max  | Unit                   |
|--------------|--------------------------------------|---|-----|------|------------------------|
| $V_{DRM}$    | repetitive peak off-state voltage    |   | -   | 800  | V                      |
| $I_{T(RMS)}$ | RMS on-state current                 | full sine wave; $T_{lead} \leq 45\text{ }^{\circ}\text{C}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a> ; see <a href="#">Figure 2</a> | -   | 1    | A                      |
| $I_{TSM}$    | non-repetitive peak on-state current | full sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 20\text{ ms}$ ; see <a href="#">Figure 4</a> ; see <a href="#">Figure 5</a>         | -   | 12.5 | A                      |
|              |                                      | full sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 16.7\text{ ms}$   | -   | 13.8 | A                      |
| $I^2t$       | $I^2t$ for fusing                    | $t_p = 10\text{ ms}$ ; sine-wave pulse  | -   | 0.78 | $\text{A}^2\text{s}$   |
| $dl_T/dt$    | rate of rise of on-state current     | $I_T = 1\text{ A}$ ; $I_G = 20\text{ mA}$ ; $dl_G/dt = 100\text{ mA}/\mu\text{s}$ ; T2+ G+  | -   | 50   | $\text{A}/\mu\text{s}$ |
|              |                                      | $I_T = 1\text{ A}$ ; $I_G = 20\text{ mA}$ ; $dl_G/dt = 100\text{ mA}/\mu\text{s}$ ; T2+ G-  | -   | 50   | $\text{A}/\mu\text{s}$ |
|              |                                      | $I_T = 1\text{ A}$ ; $I_G = 20\text{ mA}$ ; $dl_G/dt = 100\text{ mA}/\mu\text{s}$ ; T2- G-  | -   | 50   | $\text{A}/\mu\text{s}$ |
|              |                                      | $I_T = 1\text{ A}$ ; $I_G = 20\text{ mA}$ ; $dl_G/dt = 100\text{ mA}/\mu\text{s}$ ; T2- G+  | -   | 20   | $\text{A}/\mu\text{s}$ |
| $I_{GM}$     | peak gate current                    |   | -   | 1    | A                      |
| $P_{GM}$     | peak gate power                      |   | -   | 2    | W                      |
| $P_{G(AV)}$  | average gate power                   | over any 20 ms period   | -   | 0.1  | W                      |
| $T_{stg}$    | storage temperature                  |   | -40 | 150  | $^{\circ}\text{C}$     |
| $T_j$        | junction temperature                 |   | -   | 125  | $^{\circ}\text{C}$     |



**Fig 1. RMS on-state current as a function of lead temperature; maximum values**



$$f = 50\text{ Hz}, T_{lead} = 45\text{ }^{\circ}\text{C}$$

**Fig 2. RMS on-state current as a function of surge duration; maximum values**

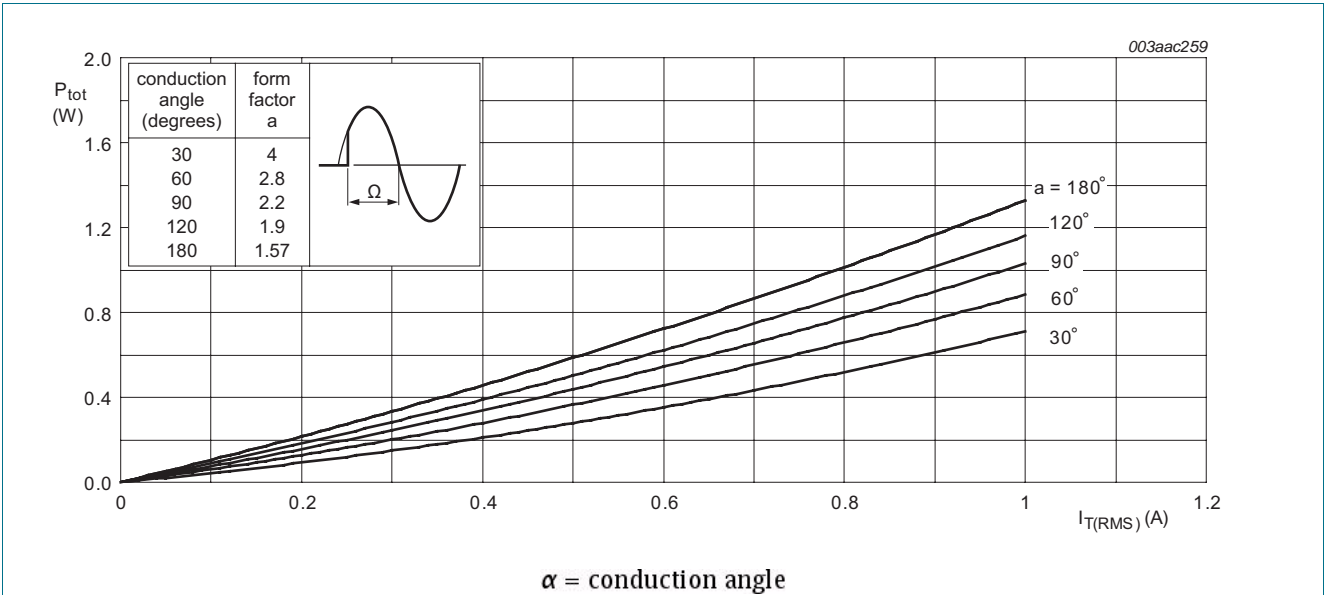


Fig 3. Total power dissipation as a function of RMS on-state current; maximum values

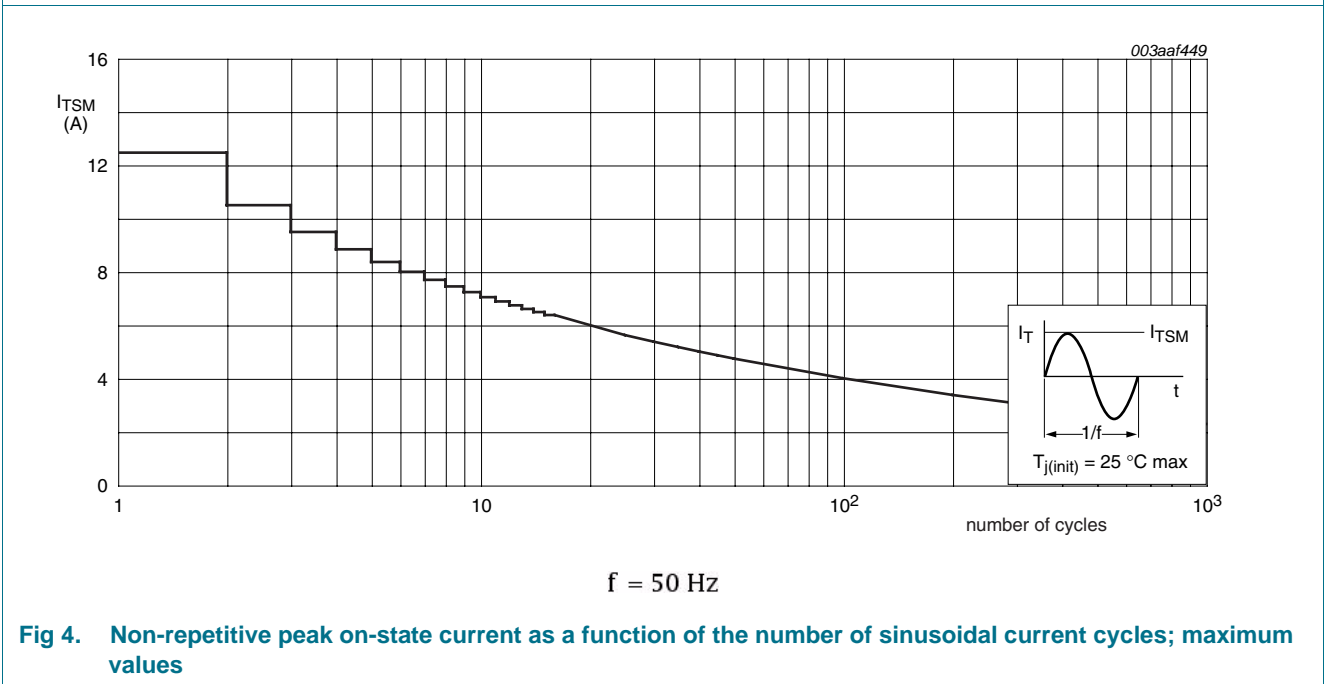


Fig 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

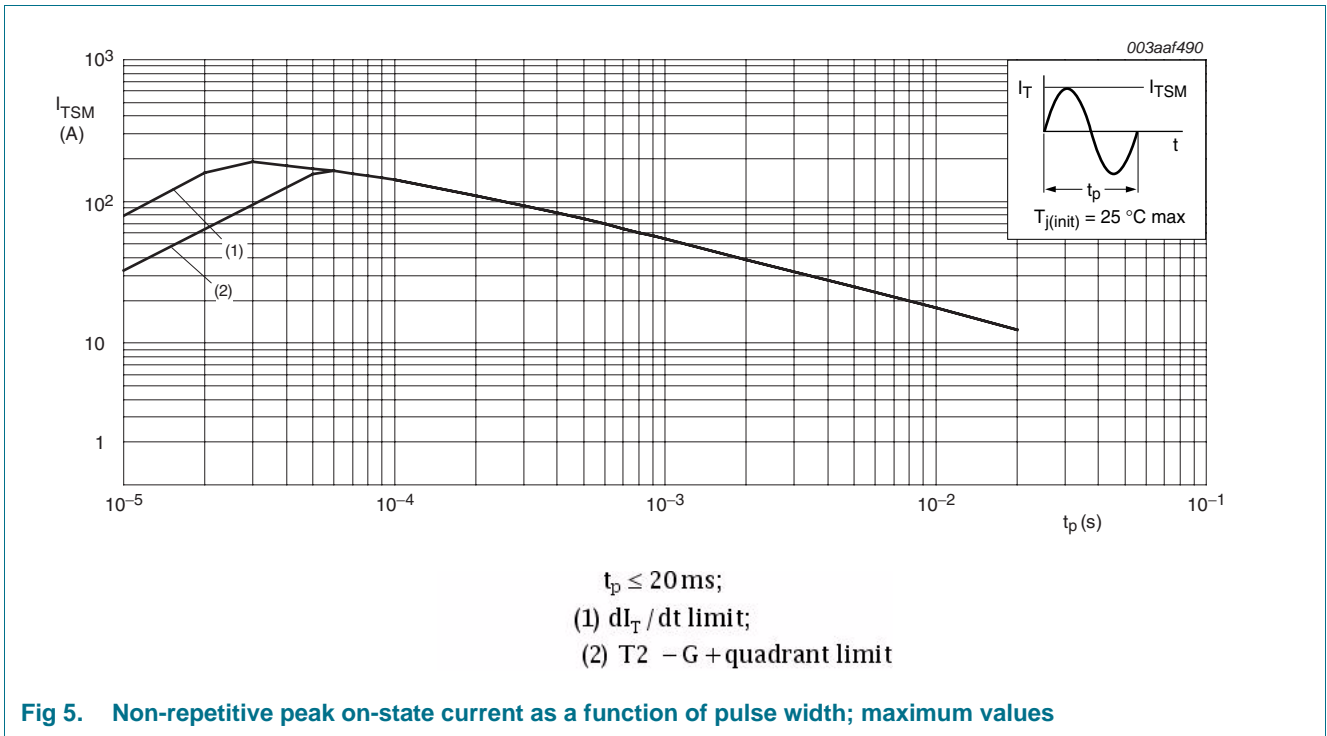
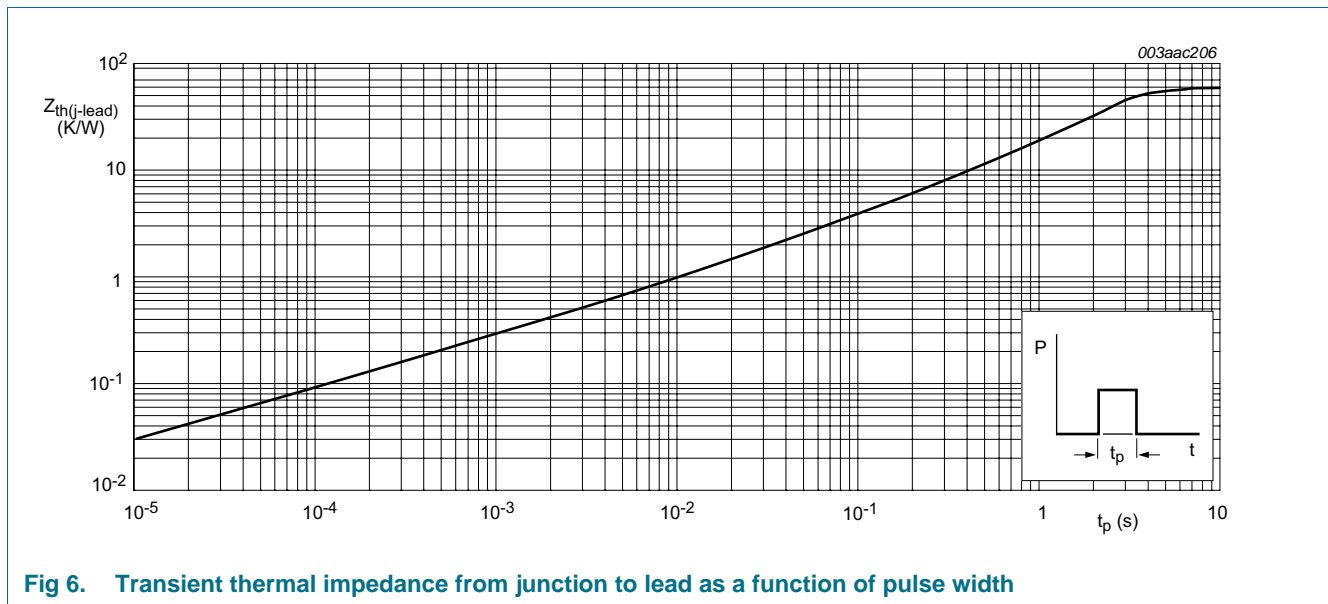


Fig 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

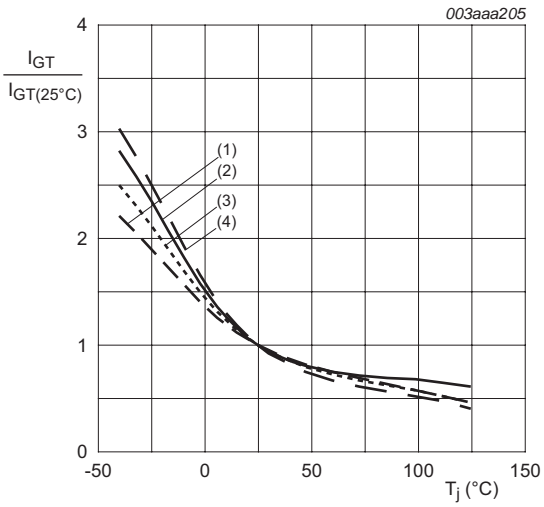
| Symbol           | Parameter                                   | Conditions  | Min | Typ | Max | Unit |
|------------------|---|---|-----|-----|-----|------|
| $R_{th(j-lead)}$ | thermal resistance from junction to lead    | full cycle; see <a href="#">Figure 6</a>                    | -   | -   | 60  | K/W  |
| $R_{th(j-a)}$    | thermal resistance from junction to ambient | full cycle; printed circuit board mounted; lead length 4 mm | -   | 150 | -   | K/W  |



## 6. Characteristics

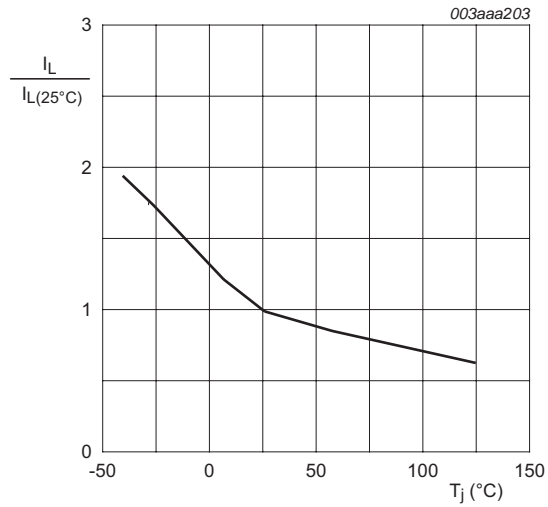
Table 6. Characteristics

| Symbol                         | Parameter                             | Conditions   | Min | Typ | Max | Unit       |
|--------------------------------|---------------------------------------|--|-----|-----|-----|------------|
| <b>Static characteristics</b>  |                                       |  |     |     |     |            |
| $I_{GT}$                       | gate trigger current                  | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G+; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 7</a>                 | 0.2 | -   | 3   | mA         |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G-; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 7</a>                 | 0.2 | -   | 3   | mA         |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G-; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 7</a>                 | 0.2 | -   | 3   | mA         |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G+; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 7</a>                 | 0.2 | -   | 5   | mA         |
| $I_L$                          | latching current                      | $V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2+ G+; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 8</a>                 | -   | -   | 7   | mA         |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2+ G-; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 8</a>                 | -   | -   | 20  | mA         |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2- G-; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 8</a>                 | -   | -   | 7   | mA         |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2- G+; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 8</a>                 | -   | -   | 7   | mA         |
| $I_H$                          | holding current                       | $V_D = 12\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 9</a>  | -   | -   | 7   | mA         |
| $V_T$                          | on-state voltage                      | $I_T = 1\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 10</a>  | -   | 1.3 | 1.6 | V          |
| $V_{GT}$                       | gate trigger voltage                  | $V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 11</a>                        | -   | -   | 1.3 | V          |
|                                |                                       | $V_D = 800\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 125\text{ °C}$ ; see <a href="#">Figure 11</a>                      | 0.2 | -   | -   | V          |
| $I_D$                          | off-state current                     | $V_D = 800\text{ V}$ ; $T_j = 125\text{ °C}$   | -   | -   | 0.5 | mA         |
| <b>Dynamic characteristics</b> |                                       |  |     |     |     |            |
| $dV_D/dt$                      | rate of rise of off-state voltage     | $V_{DM} = 536\text{ V}$ ; $T_j = 110\text{ °C}$ ; gate open circuit; exponential waveform; see <a href="#">Figure 12</a> | 80  | -   | -   | V/ $\mu$ s |
| $dV_{com}/dt$                  | rate of change of commutating voltage | $V_D = 400\text{ V}$ ; $T_j = 110\text{ °C}$ ; $dI_{com}/dt = 0.44\text{ A/ms}$ ; gate open circuit                      | 0.5 | -   | -   | V/ $\mu$ s |

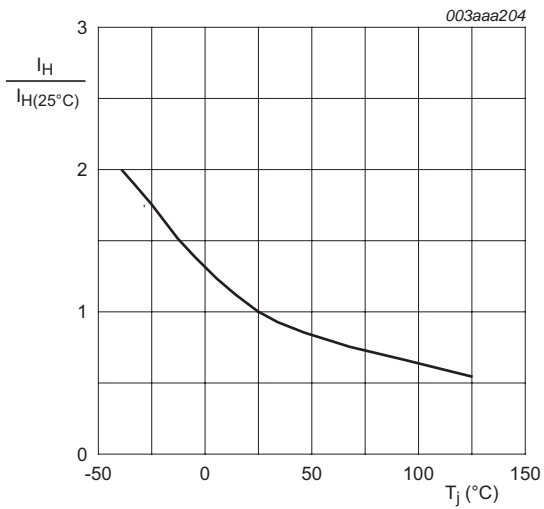


- (1) T2- G+
- (2) T2- G-
- (3) T2+ G-
- (4) T2+ G+

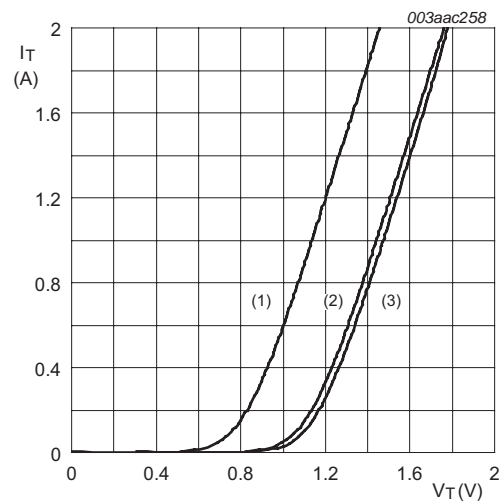
**Fig 7. Normalized gate trigger current as a function of junction temperature**



**Fig 8. Normalized latching current as a function of junction temperature**



**Fig 9. Normalized holding current as a function of junction temperature**



$V_o = 1.13 \text{ V}$

$R_s = 0.31 \text{ } \Omega$

(1)  $T_j = 125 \text{ } ^\circ\text{C}$ ; typical values

(2)  $T_j = 125 \text{ } ^\circ\text{C}$ ; maximum values

(3)  $T_j = 25 \text{ } ^\circ\text{C}$ ; maximum values

**Fig 10. On-state current as a function of on-state voltage**



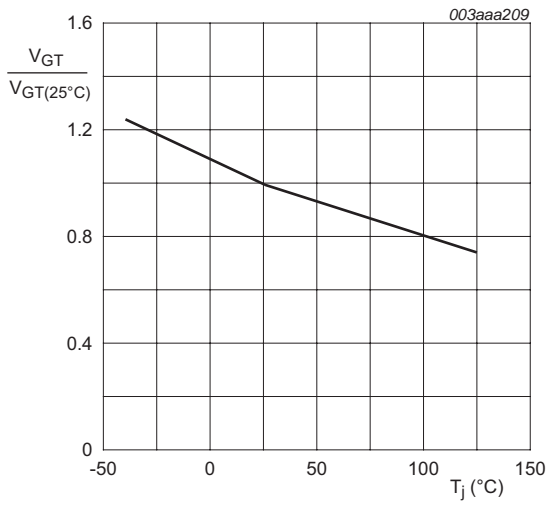
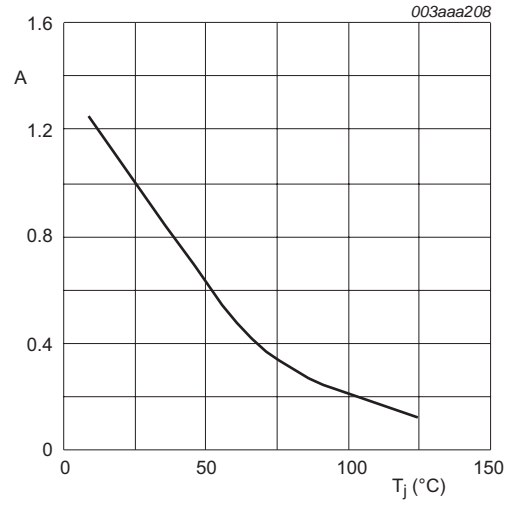


Fig 11. Normalized gate trigger voltage as a function of junction temperature



$$A = \frac{dV_D / dt}{dV_{D(25^\circ C)} / dt}$$

Fig 12. Normalized critical rate of rise of off-state voltage as a function of junction temperature; typical values

7. Package outline

Plastic single-ended leaded (through hole) package; 3 leads

SOT54

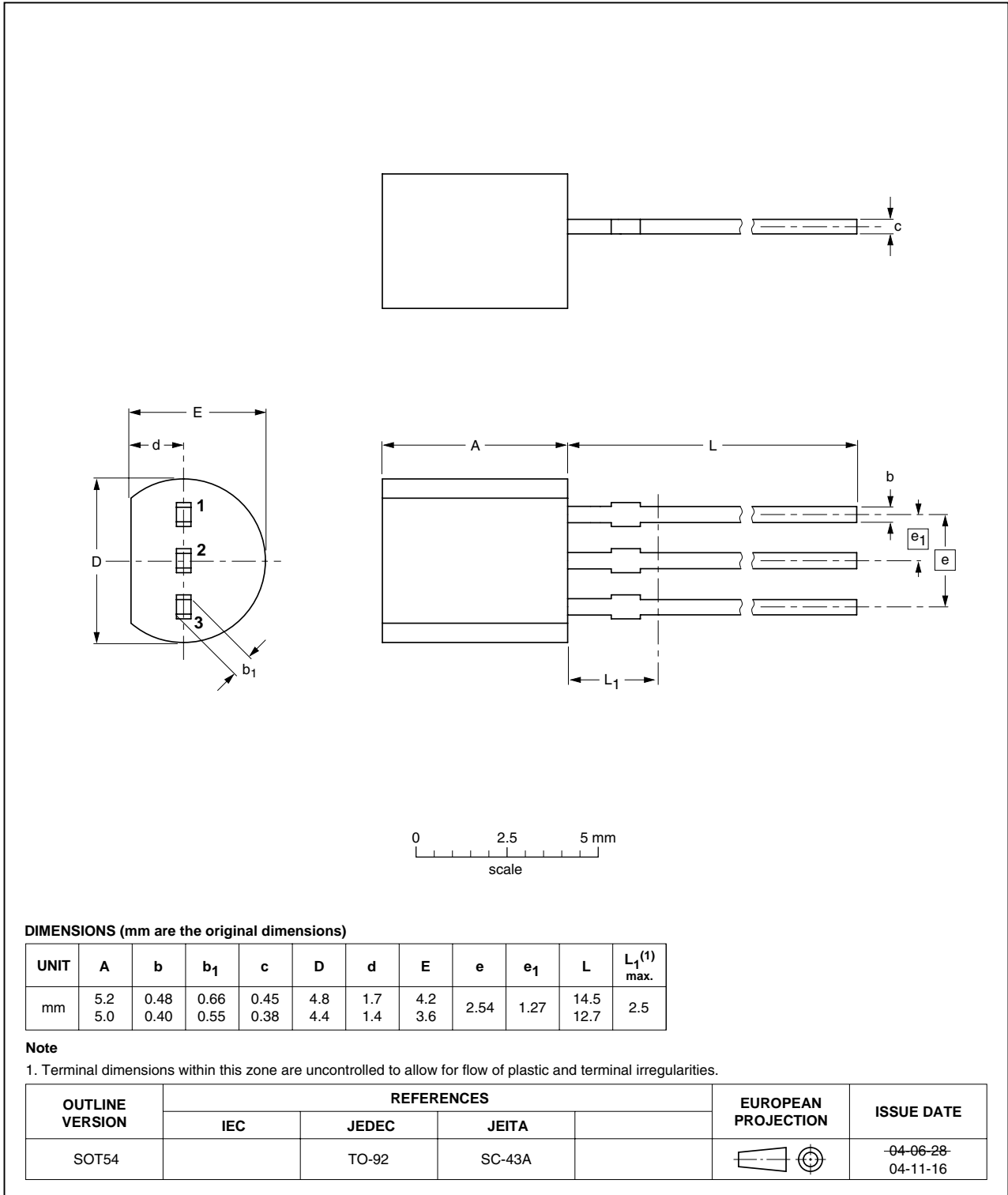


Fig 13. Package outline SOT54 (TO-92)

## 8. Revision history

Table 7. Revision history

| Document ID    | Release date                  | Data sheet status  | Change notice | Supersedes   |
|----------------|-------------------------------|--------------------|---------------|--------------|
| Z0103NA0 v.2   | 20110321                      | Product data sheet | -             | Z0103NA0 v.1 |
| Modifications: | • Various changes to content. |                    |               |              |
| Z0103NA0 v.1   | 20110103                      | Product data sheet | -             | -            |

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### 9.1 Data sheet status

| Document status <sup>[1]</sup> <sup>[2]</sup> | Product status <sup>[3]</sup> | Definition  |
|---|-------------------------------|---|
| Objective [short] data sheet                  | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet                | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet                    | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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