Variable Resolution Resolver-to-Digital Converter

AD2S80

1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein. The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. http://www.analog.com/aerospace

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/AD2S80

2.0 Part Number. The complete part number(s) of this specification follow:

Part Number	Description
AD2S80-703D	Variable Resolution Resolver-to-Digital Converter

2.1 Case Outline.

Letter	Descriptive designator	Case Outline (Lead Finish per MIL-PRF-38535)
D	GDIP2-T40	40-Lead ceramic dual-in-line package (SIDEBRAZED)

3.0 Absolute Maximum Ratings. (T_A = 25°C, unless otherwise noted)

+Vs to GND[1, 2] .....+14V
-VS to GND[1, 2] .....-14V
+VL to GND[2] .....+VS
Digital Input Voltage to GND[2] ..... -0.4V to +V_L
Demod I/P .....+14V to -VS
Integrator I/P.....+14V to -VS
VCO Input .....+14V to -VS
VREF to GND[3, 4] .....+14V to -VS
Analog Input Voltage (SIN, COS) to GND.....+14V to -VS
Power Dissipation 860mW
Storage Temperature Range.....-65°C to +150°C
Operating Temperature Range .....-55°C to +125°C
Junction Temperature (T_J).....+150°C

1 The device should be powered up as follows: -Vs should be applied before or simultaneously with the +Vs. V_L can be applied at any time with respect to +Vs and -Vs.

2 GND refers to ANALOG GND; ANALOG GND must be externally connected to DIGITAL GND.

3 SIGNAL GND is internally connected to ANALOG GND.

4 SIN, COS, and REF input voltage may be present without +VS, -VS, or +VL.

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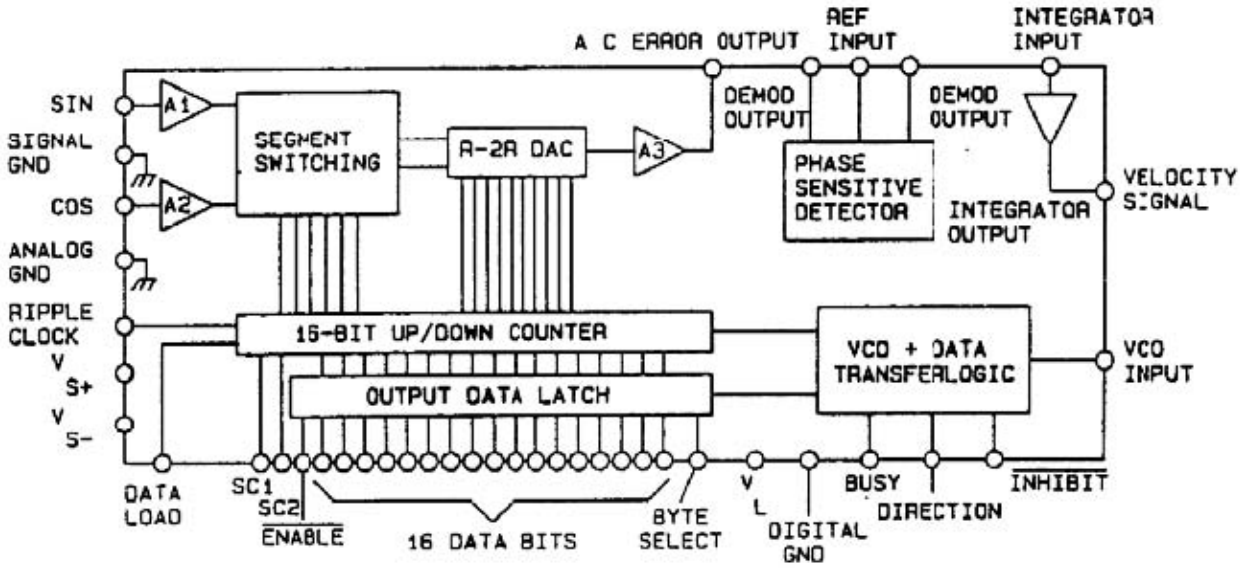
3.1 Thermal Characteristics:

Thermal Resistance, D (sidebrazed) Package

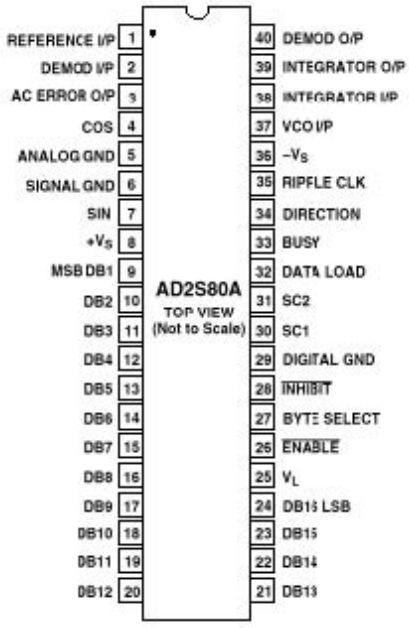
Junction-to-Case (Θ_{JC}) = 11°C/W Max

Junction-to-Ambient (Θ_{JA}) = 48°C/W Max

3.2 Functional Block Diagram:



3.3 Terminal Assignments:



4.0 Electrical Table: (See notes at end of table)

Table I

Parameter	Symbol	Conditions 1/	Sub-group	Limit Min	Limit Max	Units
Angular Accuracy 2/		V_S = ±10.8V, SCI=SC2=High V_S = ±13.2V, SC1=SC2=High 16 bit resolution	1, 2, 3		±8	Arc mins
Missing Codes 2/		V_S = ±10.8V, SCI=SC2=High V_S = ±13.2V, SC1=SC2=High 16 bit resolution	1 2, 3		±4 ±6	Codes
Total effective angular offset		Output data nulled by application of offset current to integrator input	1, 2, 3		±800	nA
Integrator output range		1 mA load	1, 2, 3	±8		V
		±V_S = 10.8V, 1 mA load	1, 2, 3	±7		
Demod O/P Scaling 2/			1, 2, 3	90	110	nA/Bit
VCO Maximum Rate			4, 5, 6		1.0	MHz
VCO Gain Scaling		Measured with VCO input, Current of ±10µA	4, 5, 6	7110	8690	Hz/µA
VCO Linearity 6/		VCO measured at 10 points over the frequency range 0 to 1MHz	4, 5, 6		±3	%
VCO Total Effective Offset		Measured with 68KΩ Input R	1, 2		380	nA
			3		400	
Digital Inputs High Voltage 3/	V_{IH}	±V_S = 10.8V	1, 2, 3	2.0		V
Digital Inputs Low Voltage 3/	V_{IL}	±V_S = 13.2V	1, 2, 3		0.8	
Digital Inputs High Current 3/	I_{IH}	±V_S = 13.2V, V_L = 5.5V V_{IH} = 5.5V	1, 2, 3		±100	µA
Digital Inputs Low Current 3/	I_{IL}	±V_S = 13.2V, V_L = 5.5V V_{IL} = 0V	1, 2, 3		±100	
Digital Inputs Low Voltage 4/	V_{IL}	$\overline{\text{ENABLE}}$ = HIGH	1, 2, 3		1.0	V
Digital Inputs Low Current 4/	I_{IL}	$\overline{\text{ENABLE}}$ = HIGH	1, 2, 3	-400		µA
Digital Outputs High Voltage 5/	V_{OH}	V_L = 4.5V, I_{OH} = 100µA	1, 2, 3	2.4		V
Digital Outputs Low Voltage 5/	V_{OL}	V_L = 5.5V, I_{OL} = 1.2mA	1, 2, 3		0.4	
High Level Three State Leakage Current	I_{OZH}	V_{OH} = 5.0V, V_L = 5.5V	1, 2, 3		±100	µA
Low level Three State Leakage Current	I_{OZL}	V_{OL} = 0V, V_L = 5.5V	1, 2, 3		±100	
Busy Pulse Width	t_{BUSY}		9, 10, 11	200	600	nS
Power Supply Current	+I_S	±V_S = ±13.2V	1, 2, 3		30	mA
	-I_S		1, 2, 3	-30		
	+I_L	V_L = 5.5V	1, 2, 3		1.5	

TABLE I NOTES:

1/ V_S = ±12V, V_L = +5V, unless otherwise specified

2/ V_{SIN}, V_{COS} = 2 V_{RMS} Maximum at 5KHz, V_{REF} = 2 V_{RMS} at 5KHz.

3/ DB1-DB16, $\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$, BYTE SELECT

4/ Digital inputs SC1, SC2, DATA LOAD are internally pulled up to +V_S.

5/ DB1-DB16, RIPPLE CLOCK, DIRECTION.

6/ VCO linearity is expressed as % (percentage) of reading.

4.1 Electrical Test Requirements:

Table II	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1, 4, 9
Final Electrical Parameters	1, 2, 3, 4, 5, 6, 9, 10, 11 1/
Group A Test Requirements	1, 2, 3, 4, 5, 6, 9, 10, 11
Group C end-point electrical parameters	1, 4, 9
Group D end-point electrical parameters	1, 4, 9
Group E end-point electrical parameters	Not applicable

1/ PDA applies to Subgroup 1.

5.0 Life Test/Burn-In Circuit:

5.1 HTRB is not applicable for this drawing.
5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B.
5.3 Steady state life test is per MIL-STD-883 Method 1005.

Rev	Description of Change	Date
A	Initiate	Oct. 12, 2000
B	Update web address	Feb. 7, 2002
C	Add subgroups 4, 5, 6, 9, 10, 11 to table II	Mar. 19, 2002
D	Update web address. Delete burn-in circuit.	June 26, 2003
E	Update header/footer and add to 1.0 Scope description.	March 11, 2008
F	Add Junction Temperature (T_J)....+150°C to section 3.0-Absolute Max. Ratings	April 3, 2008