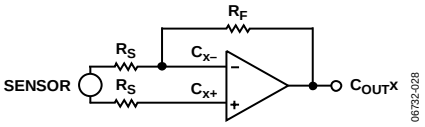


Figure 28. Recommended Comparator Connection Diagram

APPLICATION DETAILS

The AD7264 has been specifically designed to meet the requirements of any motor control shaft position feedback loop. The device can interface directly to multiple sensor types, including optical encoders, magnetoresistive sensors, and Hall effect sensors. Its flexible analog inputs, which incorporate programmable gain, ensure that identical board design can be utilized for a variety of sensors, which results in reduced design cycles and costs.

The two simultaneous sampling ADCs are used to sample the sine and cosine outputs from the sensor. No external buffering is required between the sensor/transducer and the analog inputs of the AD7264. The on-chip comparators can be used to monitor the pole sensors, which can be Hall effect sensors or the inner tracks from an optical encoder.

Figure 29 shows how the AD7264 can be used in a typical application. An optical encoder is shown in Figure 29, but other sensor types could as easily be used. Figure 29 indicates a typical application configuration only; there are several other configurations that render equally effective results.

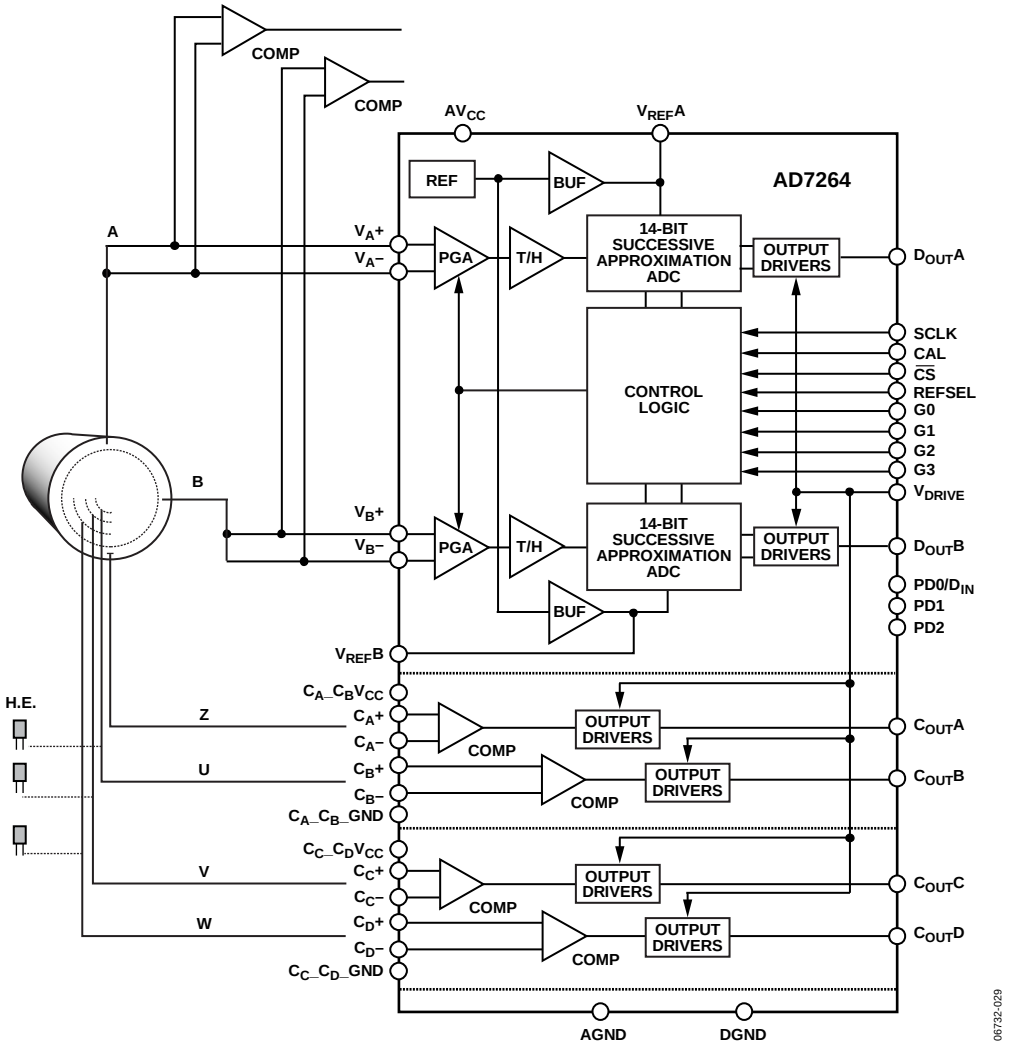


Figure 29. Typical System Connection Diagram with Optical Encoder

MODES OF OPERATION

The AD7264 allows the user to choose between two modes of operation: pin driven mode and control register mode.

PIN DRIVEN MODE

Pin driven mode allows the user to select the gain of the PGA, the power-down mode, internal or external reference, and to initiate a calibration of the offset for both ADC A and ADC B. These functions are implemented by setting the logic levels on the gain pins (G3 to G0), the power-down pins (PD2 to PD0), the REFSEL pin, and the CAL pin, respectively.

The logic state of the G3 to G0 pins determines which mode of operation is selected. Pin driven mode is selected if at least one of the gain pins is set to a logic high state. Alternatively, if all four gain pins are connected to a logic low, the control register mode of operation is selected.

GAIN SELECTION

The on-board PGA allows the user to select from 14 programmable gain stages: ×1, ×2, ×3, ×4, ×6, ×8, ×12, ×16, ×24, ×32, ×48, ×64, ×96, and ×128. The PGA accepts fully differential analog signals and provides three key functions, which include selecting gains for small amplitude input signals, driving the ADCs switched capacitive load, and buffering the source from the switching effects of the SAR ADCs. The AD7264 offers the user great flexibility in user interface, offering gain selection via the control register or by driving the gain pins to the desired logic state. The AD7264 has four gain pins, G3, G2, G1 and G0, as shown in Figure 3 and Figure 4. Each gain setting is selected by setting up the appropriate logic state on each of the four gain pins, as outlined in Table 6. If all four gain pins are connected to a logic low level, the part is put in control register mode, and the gain settings are selected via the control register.

Table 6. Gain Selection

G3	G2	G1	G0	Gain
0	0	0	0	Software control via control register
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	6
0	1	1	0	8
0	1	1	1	12
1	0	0	0	16
1	0	0	1	24
1	0	1	0	32
1	0	1	1	48
1	1	0	0	64
1	1	0	1	96
1	1	1	0	128

POWER-DOWN MODES

The AD7264 offers the user several of power-down options to enable individual device components to be powered down independently. These options can be chosen to optimize power dissipation for different application requirements. The power-down modes can be selected by either programming the device via the control register or by driving the PD pins to the appropriate logic levels. By setting the PD pins to a logic low level when in pin driven mode, all four comparators and both ADCs can be powered down. The PD2 and PD0 pins must be set to logic high and the PD1 pin set to logic low level to power up all circuitry on the AD7264. The PD pin configurations for the various power-down options are outlined in Table 7.

Table 7. Power-Down Modes

PD2	PD1	PD0	Comparator A, Comparator B	Comparator C, Comparator D	ADC A, ADC B
0	0	0	Off	Off	Off
0	0	1	Off	Off	On
0	1	0	Off	On	Off
0	1	1	On	Off	Off
1	0	0	On	On	Off
1	0	1	On	On	On
1[1]	1[1]	1[1]	Off	Off	Off

[1] PD2 = PD1 = PD0 = 1; resets the AD7264 when in pin driven mode only.

The AV_{CC} and V_{DRIVE} supplies must continue to be supplied to the AD7264 when the comparators are powered up but the ADCs are powered down. External diodes can be used from the $C_A\_C_BV_{CC}$ and/or $C_C\_C_DV_{CC}$ to both the AV_{CC} and the V_{DRIVE} supplies to ensure that they retain a supply at all times.

The AD7264 can be reset in pin driven mode only by setting the PD pins to a logic high state. When the device is reset, all the registers are cleared and the four comparators and the two ADCs are left powered down.

In the normal mode of operation with the ADCs and comparators powered on, the $C_A\_C_BV_{CC}/C_C\_C_DV_{CC}$ supplies and the AV_{CC} supply can be at different voltage levels, as indicated in Table 1. When the comparators on the AD7264 are in power-down mode and the $C_A\_C_BV_{CC}/C_C\_C_DV_{CC}$ supplies are at a potential 0.3 V greater than or less than the AV_{CC} supply, the supplies consume more current than would be the case if both sets of supplies were at the same potential. This configuration does not damage the AD7264 but results in additional current flowing in any or all of the AD7264 supply pins. This is due to ESD protection diodes within the device. In applications where power consumption in power-down mode is critical, it is recommended that the $C_A\_C_BV_{CC}/C_C\_C_DV_{CC}$ supply and the AV_{CC} supply be held at the same potential.

Power-Up Conditions

On power-up, the status of the gain pins determines which mode of operation is selected, as outlined in the Gain Selection section. All registers are set to 0.

If the AD7264 is powered up in pin driven mode, the gain pins and the PD pins should be configured to the appropriate logic states and a calibration initiated if required.

Alternatively, if the AD7264 is powered up in control register mode, the comparators and ADCs are powered down and the default gain is 1. Thus, powering up in control register mode requires a write to the device to power up the comparators and the ADCs.

It takes the AD7264 15 µs to power up when using an external reference. When the internal reference is used, 240 µs are required to power up the AD7264 with a 1 µF decoupling capacitor.

CONTROL REGISTER

The control register on the AD7264 is a 12-bit read and write register that is used to control the device when not in pin driven mode. The PD0/D_{IN} pin serves as the serial D_{IN} pin for the AD7264 when the gain pins are set to 0 (that is, the part is not in pin driven mode). The control register can be used to select the gain of the PGAs, the power-down modes, and the calibration of the offset for both ADC A and ADC B. When in the control register mode of operation, PD1 and PD2 should be connected to a low logic state. These functions can also be implemented by setting the logic levels on the gain pins, power-down pins, and CAL pin, respectively. The control register can also be used to read the offset and gain registers.

Data is loaded from the PD0/D_{IN} pin of the AD7264 on the falling edge of SCLK when $\overline{CS}$ is in a logic low state. The control register is selected by first writing the appropriate four WR bits, as outlined in Table 10. The 12 data bits must then be clocked into the control register of the device. Thus, on the 16th falling SCLK edge, the LSB is clocked into the device. One more SCLK cycle is then required to write to the internal device registers. In total, 17 SCLK cycles are required to successfully write to the AD7264. The data is transferred on the PD0/D_{IN} line while the conversion result is being processed. The data transferred on the D_{IN} line corresponds to the AD7264 configuration for the next conversion.

Only the information provided on the 12 falling clock edges after the $\overline{CS}$ falling edge and the initial four write address bits is loaded to the control register. The PD0/D_{IN} pin should have a logic low state for the four bits RD3 to RD0 when using the control register to select the power-down modes and gain setting, or when initializing a calibration. The RD bits should also be set to a logic low level to access the ADC results from both D_{OUT}A and D_{OUT}B.

The power-up status of all bits is 0, and the MSB denotes the first bit in the data stream. The bit functions are outlined in Table 9.

Table 8. Control Register Bits

MSB											LSB
Bit 11	**Bit 10**	**Bit 9**	**Bit 8**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
RD3	RD2	RD1	RD0	CAL	PD2	PD1	PD0	G3	G2	G1	G0

Table 9. Control Register Bit Function Descriptions

Bits	Mnemonic	Comment
11 to 8	RD3 to RD0	Register address bits. These bits select which register the subsequent read is from. See Table 11.
7	CAL	Setting this bit high initiates an internal offset calibration. When the calibration is completed, this pin can be reset low, and the internal offset that is stored in the on-chip offset registers is automatically removed from the ADCs results.
6 to 4	PD2 to PD0	Power-down bits. These bits select which power-down mode is programmed. See Table 7.
3 to 0	G3 to G0	Gain selection bits. These bits select which gain setting is used on the front-end PGA. See Table 6.

Table 10. Write Address Bits

WR3	WR2	WR1	WR0	Read Register Addressed
0	0	0	1	Control register

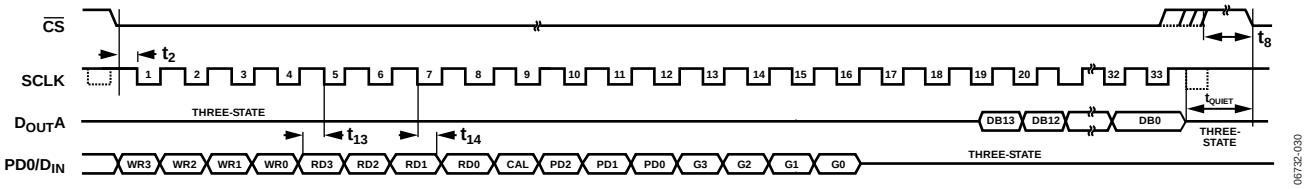


Figure 30. Timing Diagram for a Write Operation to the Control Register

ON-CHIP REGISTERS

The AD7264 contains a control register, two offset registers for storing the offsets for each ADC, and two external gain registers for storing the gain error. The control, offset, and gain registers are read and write registers. On power-up, all registers in the AD7264 are set to 0 by default.

Writing to a Register

Data is loaded from the PD0/D_{IN} pin of the AD7264 on the falling edge of SCLK when $\overline{CS}$ is in a logic low state. Four address bits and 12 data bits must be clocked into the device. Thus, on the 16th falling SCLK edge, the LSB is clocked into the AD7264. One more SCLK cycle is then required to write to the internal device registers. In total, 17 SCLK cycles are required to successfully write to the AD7264. The control and offset registers are 12-bits registers, and the gain registers are 7-bit registers.

When writing to a register, the user must first write the address bits corresponding to the selected register. Table 11 shows the decoding of the address bits. The four RD bits are written MSB first, that is, RD3 followed by RD2, RD1, and RD0. The AD7264 decodes these bits to determine which register is being addressed. The subsequent 12 bits of data are written to the addressed register.

When writing to the external gain registers, the seven bits of data immediately after the four address bits are written to the register. However, 17 SCLK cycles are still required, and the PD0/D_{IN} pin of the AD7264 should be tied low for the five additional clock cycles.

Table 11. Read and Write Register Addresses

RD3	RD2	RD1	RD0	Comment
0	0	0	0	ADC result (default)
0	0	0	1	Control register
0	0	1	0	Offset ADC A internal
0	0	1	1	Offset ADC B internal
0	1	0	0	Gain ADC A external
0	1	0	1	Gain ADC B external

Reading from a Register

The internal offset of the device, which has been measured by the AD7264 and stored in the on-chip registers during the calibration, can be read back by the user. The contents of the external gain registers can also be read. To read the contents of any register, the user must first write to the control register by writing 0001 to the WR3 to WR0 bits via the PD0/D_{IN} pin (see Table 10). The next four bits in the control register are the RD bits, which are used to select the desired register from which to read. The appropriate 4-bit addresses for each of the offset and gain registers are listed in Table 11. The remaining eight SCLK cycle bits are used to set the remaining bits in the control register to the desired state for the next ADC conversion.

The 19th SCLK falling edge clocks out the first data bit of the digital code corresponding to the value stored in the selected internal device register on the D_{OUT}A pin. D_{OUT}B outputs the conversion result from ADC B. When the selected register has been read, the control register must be reset to output the ADC results for future conversions. This is achieved by writing 0001 to the WR3 to WR0 bits, followed by 0000 to the RD bits. The remaining eight bits in the control register should then be set to the required configuration for the next ADC conversion.

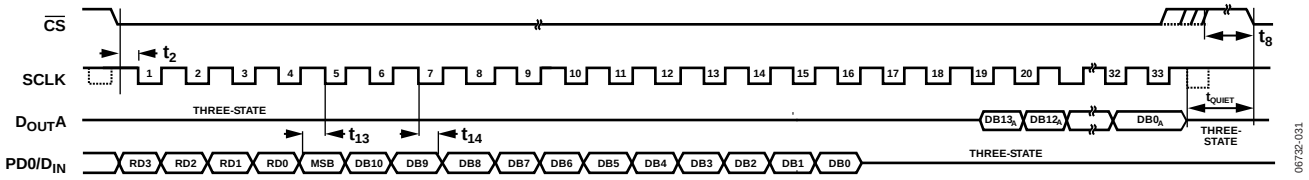


Figure 31. Timing Diagram for Writing to a Register

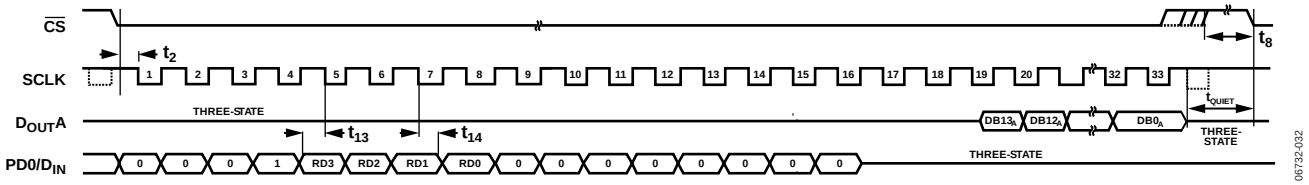


Figure 32. Timing Diagram for a Read Operation with PD0/D_{IN} as an Input

SERIAL INTERFACE

Figure 33 and Figure 34 show the detailed timing diagrams for the serial interface on the AD7264. The serial clock provides the conversion clock and controls the transfer of information from the AD7264 after the conversion. The AD7264 has two output pins corresponding to each ADC. Data can be read from the AD7264 using both $D_{OUT}A$ and $D_{OUT}B$. Alternatively, a single output pin of the user's choice can be used. The SCLK input signal provides the clock source for the serial interface.

The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode, at which point the analog input is sampled. The conversion is also initiated at this point and requires a minimum of 19 SCLK cycles to complete. The $D_{OUT}x$ lines remain in three-state while the conversion is taking place. On the 19th SCLK falling edge, the AD7264 returns to track mode and the $D_{OUT}A$ and $D_{OUT}B$ lines are enabled. The data stream consists of 14 bits of data, MSB first.

The MSB of the conversion result is clocked out on the 19th SCLK falling edge to be read by the microcontroller or DSP on the subsequent SCLK falling edge (the 20th falling edge). The remaining data is then clocked out by subsequent SCLK falling edges. Thus, the 20th falling clock edge on the serial clock has the MSB provided and also clocks out the second data bit. The remainder of the 14-bit result follows, with the final bit in the data transfer being valid for reading on the 33rd falling edge. The LSB is provided on the 32nd falling clock edge.

The AD7264-5, with its 20 MHz SCLK frequency, easily facilitates reading on the SCLK falling edge. When using a V_{DRIVE} voltage of 5 V with the AD7264, the maximum specified access time (t_4) is 23 ns, which enables reading on the subsequent falling SCLK edge after the data has been clocked out, as described previously. However, if a V_{DRIVE} voltage of 3 V is used for the AD7264 and the setup time of the microcontroller or DSP is too large to enable reading on the falling SCLK edge, it may be necessary to read on the SCLK rising edge. In this case, the MSB of the conversion result is clocked out on the 19th SCLK falling edge to be read on the 20th SCLK rising edge, as shown in Figure 35. This is possible because the hold time (t_5) is longer for lower V_{DRIVE} voltages. If the data access time is too long to accommodate the setup time of the chosen processor, an alternative to reading on the rising SCLK edge is to use a slower SCLK frequency.

On the rising edge of $\overline{CS}$, $D_{OUT}A$ and $D_{OUT}B$ go back into three-state. If $\overline{CS}$ is not brought high after 33 SCLK cycles but is instead held low for an additional 14 SCLK cycles, the data from ADC B is output on $D_{OUT}A$ after the ADC A result. Likewise, the data from ADC A is output on $D_{OUT}B$ after the ADC B result. This is illustrated in Figure 34, which shows the $D_{OUT}A$ example. In this case, the D_{OUT} line in use goes back into three-state on the 47th SCLK falling edge or the rising edge of $\overline{CS}$, whichever occurs first.

If the falling edge of SCLK coincides with the falling edge of $\overline{CS}$, the falling edge of SCLK is not acknowledged by the AD7264, and the next falling edge of SCLK is the first one registered after the falling edge of $\overline{CS}$.

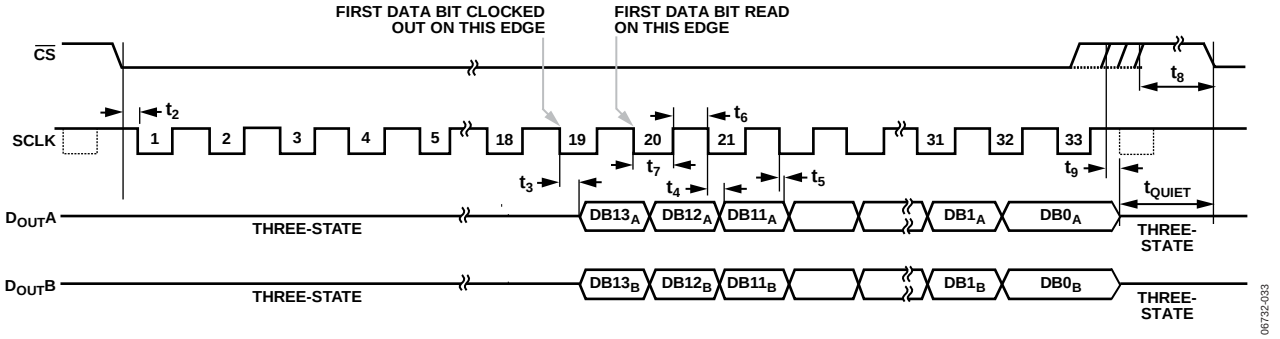


Figure 33. Normal Mode Operation

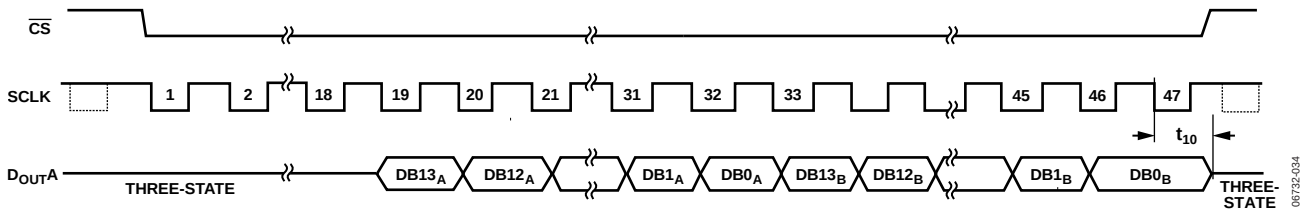


Figure 34. Reading Data from Both ADCs on One D_{OUT} Line with 47 SCLK Cycles

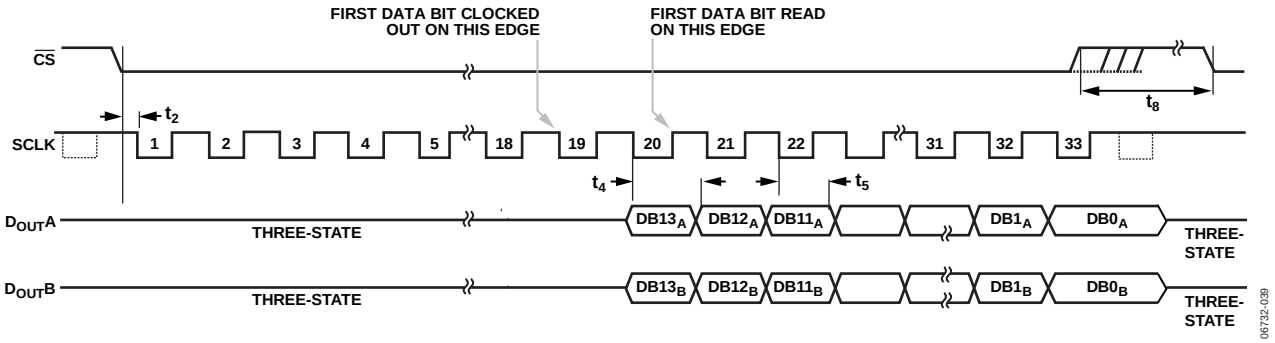


Figure 35. Serial Interface Timing Diagram When Reading Data on the Rising SCLK Edge with V_{DRIVE} = 3 V

CALIBRATION

INTERNAL OFFSET CALIBRATION

The AD7264 allows the user to calibrate the offset of the device using the CAL pin. This is achieved by setting the CAL pin to a high logic level, which initiates a calibration on the next $\overline{CS}$ falling edge. The calibration requires one full conversion cycle, which contains a $\overline{CS}$ falling edge followed by 19 SCLK cycles. The CAL pin can remain high for more than one conversion, if desired, and the AD7264 continues to calibrate.

The CAL pin should be driven high only when the $\overline{CS}$ pin is high or after 19 SCLK cycles have elapsed when $\overline{CS}$ is low, that is, between conversions. The CAL pin must be driven high t_{12} before $\overline{CS}$ goes low. If the $\overline{CS}$ pin goes low before t_{12} elapses, the calibration result will be inaccurate for the current conversion; if the CAL pin remains high, the subsequent calibration conversion is correct. If the CAL pin is set to a logic high state during a conversion, that conversion result is corrupted.

If the CAL pin has been held high for a minimum of one conversion and when t_{12} and t_{11} have been adhered to, the calibration is complete after the 19th SCLK cycle and the CAL pin can be driven to a logic low state. The next $\overline{CS}$ falling edge after the CAL pin has been driven to a low logic state initiates a conversion of the differential analog input signal for both ADC A and ADC B.

Alternatively, the control register can be used to initiate an offset calibration. This is done by setting the CAL bit in the control register to 1. The calibration is then initiated on the next $\overline{CS}$ falling edge, but the current conversion is corrupted. The ADCs on the AD7264 must remain fully powered up to complete the internal calibration.

The AD7264 registers store the offset value, which can easily be accessed by the user (see the Reading from a Register section). When the device is calibrating, the differential analog inputs for each respective ADC are shorted together internally and a conversion is performed. A digital code representing the offset is stored internally in the offset registers, and subsequent conversion results have this measured offset removed.

When the AD7264 is calibrated, the calibration results stored in the internal device registers are relevant only for the particular PGA gain selected at the time of calibration. If the PGA gain is changed, the AD7264 must be recalibrated. If the device is not recalibrated when the PGA gain is changed, the offset for the previous gain setting continues to be removed from the digital output code, which may lead to inaccuracies.

The offset range that can be calibrated for is ±500 LSB at a gain of 1. The maximum offset voltage that can be calibrated for is reduced as the gain of the PGA is increased.

Table 12 details the maximum offset voltage that can be removed by the AD7264 without compromising the available digital output code range. The least significant bit size is $AV_{CC}/2^{Bits}$, which is 5/16,384 or 305 μV for the AD7264. The maximum removable offset voltage is given by

$$\pm 500 \text{ LSB} \times \frac{305\ \mu\text{V}}{Gain}$$

Table 12. Offset Voltage Range

Gain	Maximum Removable Offset Voltage
1	±152.5 mV
2	±76.25 mV
3	±50.83 mV
32	±4.765 mV

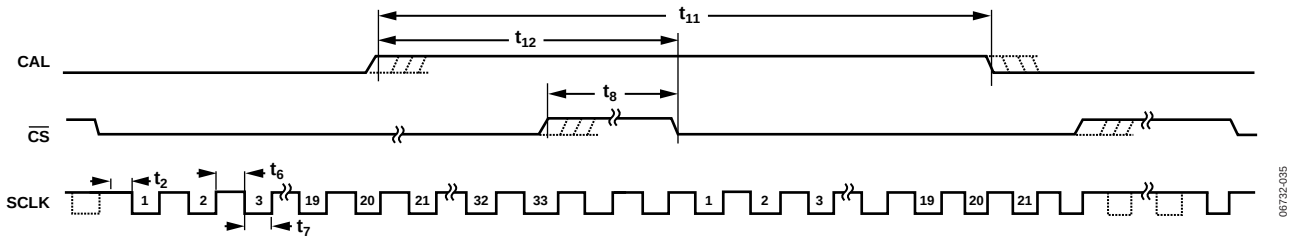


Figure 36. Calibration Timing Diagram

ADJUSTING THE OFFSET CALIBRATION REGISTER

The internal offset calibration register can be adjusted manually to compensate for any signal path offset from the sensors to the ADC. No internal calibration is required, and the CAL pin can remain at a low logic state. By changing the contents of the offset register, different amounts of offset on the analog input signal can be compensated for. Use the following steps to determine the digital code to be written to the offset register:

1. Configure the sensor to its offset state.
2. Perform a number of conversions using the AD7264.
3. Take the mean digital output code from both $D_{OUT}A$ and $D_{OUT}B$. This is a 14-bit result but the offset register is only 12 bits; thus, the 14-bit result needs to be converted to a 12-bit result that can be stored in the offset register. This is achieved by keeping the sign bit and removing the second and third MSBs.
4. The resultant digital code can then be written to the offset registers to calibrate the AD7264.

Example:

Mean digital code from $D_{OUT}A$ = 8100 (01 1111 1010 0100)
Code written to offset register = 0111 1010 0100

If a +10 mV offset is present in the analog input signal and the gain of the PGA is 2, the code that needs to be written to the offset register to compensate for the offset is

$$\frac{+10\,\text{mV}}{(305\,\mu\text{V}/2)} = 65.57 = 0000\ 0100\ 0001$$

If a −10 mV offset is present in the analog input signal and the gain of the PGA is 2, the code that needs to be written to the offset register to compensate for the offset is

$$\frac{-10\,\text{mV}}{(305\,\mu\text{V}/2)} = -65.57 = 1000\ 0100\ 0001$$

SYSTEM GAIN CALIBRATION

The AD7264 also allows the user to write to an external gain register, thus enabling the removal of any overall system gain error. Both ADC A and ADC B have independent external gain registers, allowing the user to calibrate independently the gain on both ADC A and ADC B signal paths. The gain calibration feature can be used to implement accurate gain matching between ADC A and ADC B.

The system calibration function is used by setting the sensors to which the AD7264 is connected to a 0 gain state. The AD7264 converts this analog input to a digital output code, which corresponds to the system gain and is available on the D_{OUT} pins, This digital output code can then be stored in the appropriate external register. For details on how to write to a register, see the Writing to a Register section and Table 11.

The gain calibration register contains seven bits of data. By changing the contents of the gain register, different amounts of gain on the analog input signal can be compensated for. The MSB is a sign bit, while the remaining six bits store the multiplication factor, which is used to adjust the analog input range. The gain register value is effectively multiplied by the analog input to scale the conversion result over the full range. Increasing the gain register multiplication factor compensates for a larger analog input range, and decreasing the gain register multiplier compensates for a smaller analog input range. Each bit in the gain calibration register has a resolution of 2.4×10^{-4} V (1/4096). A maximum of 1.538% of the analog range can be calibrated for. The multiplier factor stored in the gain register can be decoded as outlined in Table 13.

The gain registers can be cleared by writing all 0s to each register, as described in the Writing to a Register section. For accurate gain calibration, both the positive and negative full-scale digital output codes should be measured prior to determining the multiplication factor that is written to the gain register.

Table 13. Decoding of Multiplication Factors for Gain Calibration

Analog Input (V)	Digital Gain Error (LSB)	Gain Register Code (Sign Bit + 6 Bits)	Multiplier Equation (1 ± x/4096)	Multiplier Value	Comments
V_{IN} max	0 LSB	0 000000	1 − 0/4096	1	Sign bit = 0; negative sign in multiplier equation
V_{IN} max − 244 µV	−2 LSB	0 000001	1 − 1/4096	0.999755859	Sign bit = 0; negative sign in multiplier equation
V_{IN} max − (63 × 244 µV)	−126 LSB	0 111111	1 − 63/4096	0.98461914	Sign bit = 0; negative sign in multiplier equation
V_{IN} max	0 LSB	1 000000	1 + 0/4096	1	Sign bit = 1; plus sign in multiplier equation
V_{IN} max + 244 µV	+2 LSB	1 000001	1 + 1/4096	1.000244141	Sign bit = 1; plus sign in multiplier equation
V_{IN} max + (63 × 244 µV)	+126 LSB	1 111111	1 + 63/4096	1.015380859	Sign bit = 1; plus sign in multiplier equation

APPLICATION HINTS

GROUNDING AND LAYOUT

The analog and digital supplies to the AD7264 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The printed circuit board (PCB) that houses the AD7264 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This design facilitates the use of ground planes that can be easily separated.

To provide optimum shielding for ground planes, a minimum etch technique is generally best. All five AGND pins of the AD7264 should be sunk in the AGND plane. Digital and analog ground planes should be joined in only one place. If the AD7264 is in a system where multiple devices require an AGND to DGND connection, the connection should still be made at only one point, a star ground point, that should be established as close as possible to the ground pins on the AD7264.

Avoid running digital lines under the device because this couples noise onto the die. However, the analog ground plane should be allowed to run under the AD7264 to avoid noise coupling. The power supply lines to the AD7264 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

To avoid radiating noise to other sections of the board, fast switching signals, such as clocks, should be shielded with digital ground, and clock signals should never run near the analog inputs. Avoid crossover of digital and analog signals. To reduce the effects of feedthrough within the board, traces on opposite sides of the board should run at right angles to each other. A microstrip technique is the best method but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, while signals are placed on the solder side.

Good decoupling is also important. All analog supplies should be decoupled with 10 μF tantalum capacitors in parallel with 100 nF capacitors to GND. To achieve the best results from these decoupling components, they must be placed as close as possible to the device, ideally right up against the device. The 0.1 μF capacitors should have low effective series resistance (ESR) and low effective series inductance (ESI), such as the common ceramic types or surface-mount types. These low ESR and low ESI capacitors provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

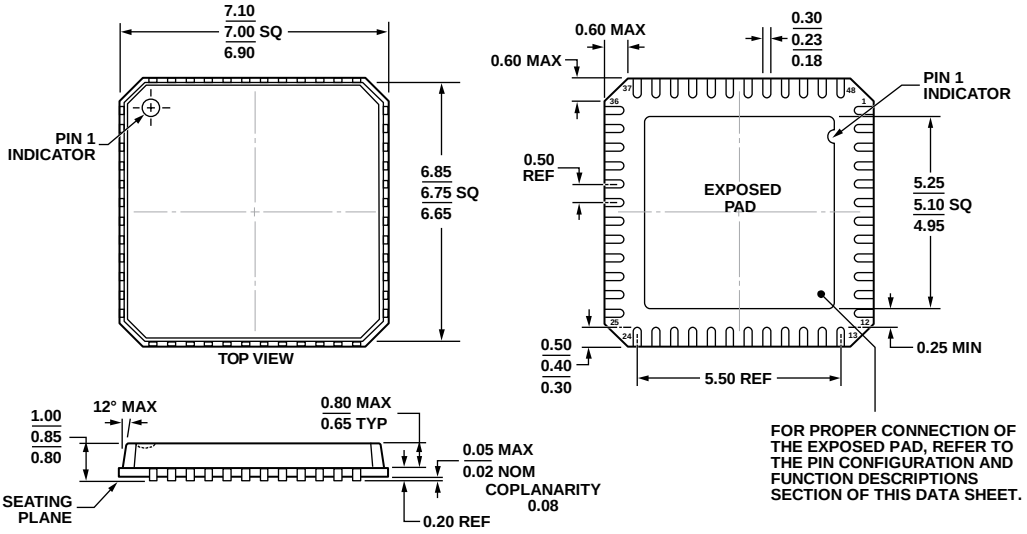
PCB DESIGN GUIDELINES FOR LFCSP

The lands on the chip scale package (CP-48-1) are rectangular. The PCB pad for these should be 0.1 mm longer than the package land length, and 0.05 mm wider than the package land width, leaving a portion of the pad exposed. To ensure that the solder joint size is maximized, the land should be centered on the pad.

The bottom of the chip scale package has a thermal pad. The thermal pad on the PCB should be at least as large as the exposed pad. On the PCB, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern to ensure that shorting is avoided.

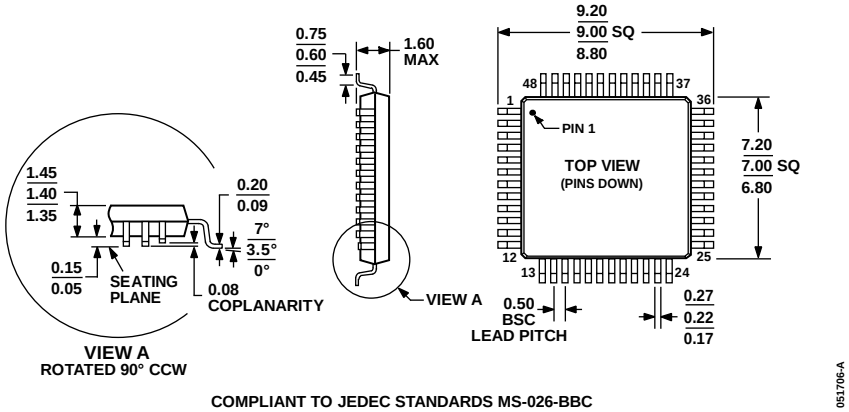
To improve thermal performance of the package, use thermal vias on the PCB, incorporating them in the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 oz copper to plug the via. The user should connect the PCB thermal pad to AGND.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VKKD-2

Figure 37. 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
7 mm × 7 mm Body, Very Thin Quad
(CP-48-1)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026-BBC

Figure 38. 48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7264BCPZ	−40°C to +105°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-48-1
AD7264BCPZ-RL7	−40°C to +105°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-48-1
AD7264BCPZ-5	−40°C to +105°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-48-1
AD7264BCPZ-5-RL7	−40°C to +105°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-48-1
AD7264BSTZ	−40°C to +105°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
AD7264BSTZ-RL7	−40°C to +105°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
AD7264BSTZ-5	−40°C to +105°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
AD7264BSTZ-5-RL7	−40°C to +105°C	48-Lead Low Profile Quad Flat Package [LQFP]	ST-48
EVAL-AD7264EDZ		Evaluation Board	
EVAL-CED1Z		Development Board	

[1] Z = RoHS Compliant Part.