Octal Ultrasound AFE With Digital Demodulator, JESD204B

Preliminary Technical Data

AD9671

FEATURES

- 8 channels of LNA, VGA, AAF, ADC, and digital demodulator/decimator
  - Low power: 150 mW per channel, TGC mode, 40 MSPS; 65mW per channel, CW mode; <30mW at power-up
  - 10 mm × 10 mm, 144-ball CSP-BGA
  - TGC channel input-referred noise: 0.8 nV/√Hz, max gain
  - Flexible power-down modes
  - Fast recovery from low power standby mode: <2 µs
  - Overload recovery: <10 ns
- Low noise preamplifier (LNA)
  - Input-referred noise: 0.78 nV/√Hz, gain = 21.6 dB
  - Programmable gain: 15.6 dB/17.9 dB/21.6 dB
  - 0.1 dB compression: 1000 mV p-p/750 mV p-p/450 mV p-p
  - Flexible active input impedance matching
- Variable gain amplifier (VGA)
  - Attenuator range: 45dB, Linear-in-dB gain control
  - Postamp gain (PGA): 21 dB/24 dB/27 dB/30 dB
- Antialiasing filter (AAF)
  - Programmable second-order LPF from 8 MHz to 18 MHz or 13.5MHz to 30MHz and HPF
- Analog-to-digital converter (ADC)
  - SNR: 75dB, 14 bits up to 125 MSPS
- JESD204B Subclass 0 coded serial digital outputs
- CW mode harmonic rejection I/Q demodulator
  - Individual programmable phase rotation
  - Output dynamic range per channel: >160 dBc/√Hz
  - Output-referred SNR: 156 dBc/√Hz, 1 kHz offset, –3dBFS
- Digital demodulator/decimator
  - I/Q demodulator with programmable oscillator
  - FIR decimation filter: 16 taps per decimation factor

GENERAL DESCRIPTION

The AD9671 is designed for low cost, low power, small size, and ease of use for medical ultrasound. It contains eight channels of a variable gain amplifier (VGA) with a low noise preamplifier (LNA), a CW harmonic rejection I/Q demodulator with programmable phase rotation, an anti-aliasing filter (AAF), an analog-to-digital converter (ADC), and a digital demodulator and decimator for data processing and bandwidth reduction. Four configurable 5-Gbps serial JESD204B CML data lanes provide an interface for further data processing.

Each channel features a maximum gain of up to 52 dB, a fully differential signal path, and an active input preamplifier termination. The channel is optimized for high dynamic performance and low power in applications where a small package size is critical.

The LNA has a single-ended-to-differential gain that is selectable through the SPI. Assuming a 15 MHz noise bandwidth (NBW) and a 21.6 dB LNA gain, the LNA input SNR is 94 dB. In CW Doppler mode, each LNA output drives an I/Q demodulator that has independently programmable phase rotation with 16 phase settings.

Power-down of individual channels is supported to increase battery life for portable applications. Standby mode allows quick power-up for power cycling. In CW Doppler operation, the VGA, AAF, and ADC are powered down. The ADC contains several features designed to maximize flexibility and minimize system cost, such as a programmable clock, data alignment, and programmable digital test pattern generation. The digital test patterns include built-in fixed patterns, built-in pseudo random patterns, and custom user-defined test patterns entered via the serial port interface. This product is protected by a U.S. patent.

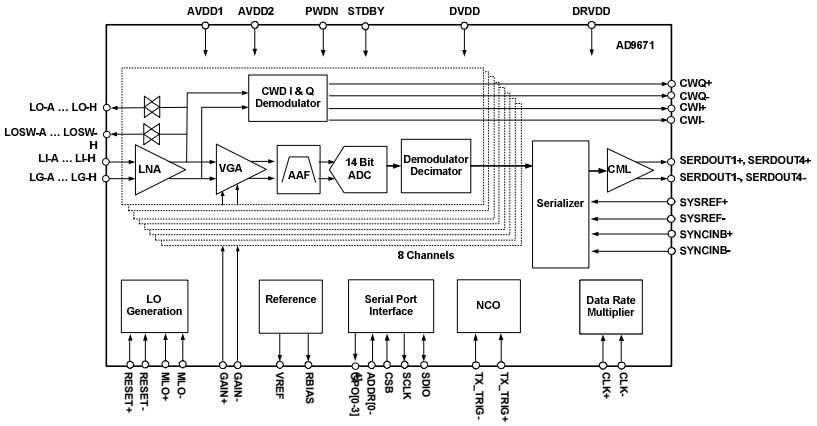

Figure 1.

Rev. PrB

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