400 MHz to 6 GHz Broadband Quadrature Modulator

Data Sheet **ADL5375-EP**

FEATURES

Output frequency range: 400 MHz to 6 GHz
1 dB output compression: ≥9.0 dBm from 450 MHz to 4 GHz
Output return loss ≤−12 dB from 450 MHz to 4.5 GHz
Noise floor: −160 dBm/Hz @ 900 MHz
Sideband suppression: ≤−50 dBc @ 900 MHz
Carrier feedthrough: ≤−45 dBm @ 900 MHz
IQ3dB bandwidth: ≥ 750 MHz
Baseband input bias level
  ADL5375-EP: 500 mV
Single supply: 4.75 V to 5.25 V
24-lead LFCSP_WQ package

ENHANCED PRODUCT FEATURES

Supports defense and aerospace applications (AQEC)
Extended temperature range −55°C to +105°C
Controlled manufacturing baseline
One assembly/test site
One fabrication site
Enhanced product change notification
Qualification data available on request

APPLICATIONS

Cellular communication systems
  GSM/EDGE, CDMA2000, W-CDMA, TD-SCDMA
WiMAX/LTE broadband wireless access systems
Satellite modems
Defense and aerospace systems

FUNCTIONAL BLOCK DIAGRAM

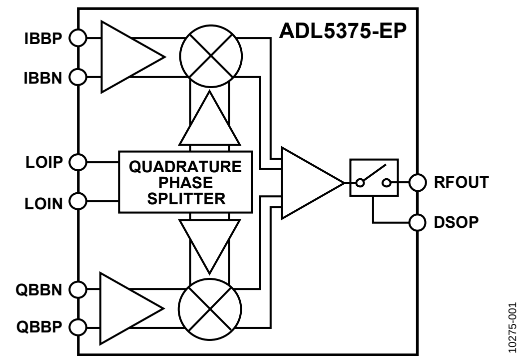

Figure 1.

GENERAL DESCRIPTION

The ADL5375-EP is a broadband quadrature modulator designed for operation from 400 MHz to 6 GHz. Its excellent phase accuracy and amplitude balance enable high performance intermediate frequency or direct radio frequency modulation for communication systems.

The ADL5375-EP features a broad baseband bandwidth, along with an output gain flatness that varies no more than 1 dB from 450 MHz to 5 GHz. These features, coupled with a broadband output return loss of ≤−12 dB, make the ADL5375-EP ideally suited for broadband zero IF or low IF-to-RF applications, broadband digital predistortion transmitters, and multiband radio designs.

The ADL5375-EP accepts two differential baseband inputs and a single-ended LO. It generates a single-ended 50 Ω output. The ADL5375-EP offers an input baseband bias level of 500 mV.

The ADL5375-EP is fabricated using an advanced silicon-germanium bipolar process. It is available in a 24-lead, exposed paddle, lead-free, LFCSP_WQ package. Performance is specified over a −55°C to +105°C temperature range. A lead-free evaluation board is also available.

Additional application and technical information can be found in the ADL5375 data sheet.

Rev. 0

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REVISION HISTORY

11/11— Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V; T_A = 25°C; LO = 0 dBm single-ended drive; baseband I/Q amplitude = 1 V p-p differential sine waves in quadrature with a 500 mV dc bias; baseband I/Q frequency (f_{BB}) = 1 MHz, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OPERATING FREQUENCY RANGE					
Low frequency			400		MHz
High frequency			6000		MHz
LO = 450 MHz					
Output Power, P_{OUT}	V_{IQ} = 1 V p-p differential		0.85		dBm
Modulator Voltage Gain	RF output divided by baseband input voltage		−3.1		dB
Output P1dB			9.6		dBm
Output Return Loss			−16.4		dB
Carrier Feedthrough			−47.5		dBm
Sideband Suppression			−37.6		dBc
Quadrature Error			1.7		Degrees
I/Q Amplitude Balance			0.07		dB
Second Harmonic	P_{OUT} − (f_{LO} + (2 × f_{BB})), P_{OUT} = 0.85 dBm		−75.9		dBc
Third Harmonic	P_{OUT} − (f_{LO} + (3 × f_{BB})), P_{OUT} = 0.85 dBm		−51.5		dBc
Output IP2	f1BB = 3.5 MHz, f2BB = 4.5 MHz, baseband I/Q amplitude per tone = 0.5 V p-p differential		65.4		dBm
Output IP3	f1BB = 3.5 MHz, f2BB = 4.5 MHz, baseband I/Q amplitude per tone = 0.5 V p-p differential		26.6		dBm
Noise Floor	I/Q inputs = 0 V differential with a dc bias only, 20 MHz carrier offset		−160.5		dBm/Hz
LO = 900 MHz					
Output Power, P_{OUT}	V_{IQ} = 1 V p-p differential		0.75		dBm
Modulator Voltage Gain	RF output divided by baseband input voltage		−3.2		dB
Output P1dB			9.6		dBm
Output Return Loss			−15.7		dB
Carrier Feedthrough			−45.1		dBm
Sideband Suppression			−52.8		dBc
Quadrature Error			0.01		Degrees
I/Q Amplitude Balance			0.07		dB
Second Harmonic	P_{OUT} − (f_{LO} + (2 × f_{BB})), P_{OUT} = 0.75 dBm		−75.8		dBc
Third Harmonic	P_{OUT} − (f_{LO} + (3 × f_{BB})), P_{OUT} = 0.75 dBm		−50.7		dBc
Output IP2	f1BB = 3.5 MHz, f2BB = 4.5 MHz, baseband I/Q amplitude per tone = 0.5 V p-p differential		62.6		dBm
Output IP3	f1BB = 3.5 MHz, f2BB = 4.5 MHz, baseband I/Q amplitude per tone = 0.5 V p-p differential		25.9		dBm
Noise Floor	I/Q inputs = 0 V differential with a dc bias only, 20 MHz carrier offset		−160.0		dBm/Hz
LO = 1900 MHz					
Output Power, P_{OUT}	V_{IQ} = 1 V p-p differential		0.53		dBm
Modulator Voltage Gain	RF output divided by baseband input voltage		−3.4		dB
Output P1dB			9.9		dBm
Output Return Loss			−16.2		dB
Carrier Feedthrough			−40.3		dBm
Sideband Suppression			−50.2		dBc
Quadrature Error			0.02		Degrees
I/Q Amplitude Balance			0.07		dB
Second Harmonic	P_{OUT} − (f_{LO} + (2 × f_{BB})), P_{OUT} = 0.53 dBm		−67.9		dBc
Third Harmonic	P_{OUT} − (f_{LO} + (3 × f_{BB})), P_{OUT} = 0.53 dBm		−51.8		dBc

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Output IP2	f1BB = 3.5 MHz, f2BB = 4.5 MHz, baseband I/Q amplitude per tone = 0.5 V p-p differential		62.6		dBm
Output IP3	f1BB = 3.5 MHz, f2BB = 4.5 MHz, baseband I/Q amplitude per tone = 0.5 V p-p differential		24.3		dBm
Noise Floor	I/Q inputs = 0 V differential with a dc bias only, 20 MHz carrier offset		−160.0		dBm/Hz
LO = 2150 MHz					
Output Power, P_{OUT}	V_{IQ} = 1 V p-p differential		0.73		dBm
Modulator Voltage Gain	RF output divided by baseband input voltage		−3.2		dB
Output P1dB			10.0		dBm
Output Return Loss			−17.1		dB
Carrier Feedthrough			−39.7		dBm
Sideband Suppression			−47.3		dBc
Quadrature Error			−0.16		Degrees
I/Q Amplitude Balance			0.07		dB
Second Harmonic	$P_{OUT} - (f_{LO} + (2 \times f_{BB}))$, P_{OUT} = 0.73 dBm		−71.3		dBc
Third Harmonic	$P_{OUT} - (f_{LO} + (3 \times f_{BB}))$, P_{OUT} = 0.73 dBm		−52.4		dBc
Output IP2	f1BB = 3.5 MHz, f2BB = 4.5 MHz, baseband I/Q amplitude per tone = 0.5 V p-p differential		61.6		dBm
Output IP3	f1BB = 3.5 MHz, f2BB = 4.5 MHz, baseband I/Q amplitude per tone = 0.5 V p-p differential		24.2		dBm
Noise Floor	I/Q inputs = 0 V differential with a dc bias only, 20 MHz carrier offset		−159.5		dBm/Hz
LO = 2600 MHz					
Output Power, P_{OUT}	V_{IQ} = 1 V p-p differential		0.61		dBm
Modulator Voltage Gain	RF output divided by baseband input voltage		−3.4		dB
Output P1dB			9.6		dBm
Output Return Loss			−19.3		dB
Carrier Feedthrough			−36.5		dBm
Sideband Suppression			−48.3		dBc
Quadrature Error			−0.37		Degrees
I/Q Amplitude Balance			0.07		dB
Second Harmonic	$P_{OUT} - (f_{LO} + (2 \times f_{BB}))$, P_{OUT} = 0.61 dBm		−60.9		dBc
Third Harmonic	$P_{OUT} - (f_{LO} + (3 \times f_{BB}))$, P_{OUT} = 0.61 dBm		−51.3		dBc
Output IP2	f1BB = 3.5 MHz, f2BB = 4.5 MHz, baseband I/Q amplitude per tone = 0.5 V p-p differential		55.0		dBm
Output IP3	f1BB = 3.5 MHz, f2BB = 4.5 MHz, baseband I/Q amplitude per tone = 0.5 V p-p differential		22.7		dBm
Noise Floor	I/Q inputs = 0 V differential with a dc bias only, 20 MHz carrier offset		−159.0		dBm/Hz
LO = 3500 MHz					
Output Power, P_{OUT}	V_{IQ} = 1 V p-p differential		0.21		dBm
Modulator Voltage Gain	RF output divided by baseband input voltage		−3.8		dB
Output P1dB			9.6		dBm
Output Return Loss			−20.7		dB
Carrier Feedthrough			−30.4		dBm
Sideband Suppression			−48.3		dBc
Quadrature Error			0.01		Degrees
I/Q Amplitude Balance			0.08		dB
Second Harmonic	$P_{OUT} - (f_{LO} + (2 \times f_{BB}))$, P_{OUT} = 0.21 dBm		−55.8		dBc
Third Harmonic	$P_{OUT} - (f_{LO} + (3 \times f_{BB}))$, P_{OUT} = 0.21 dBm		−50.2		dBc
Output IP2	f1BB = 3.5 MHz, f2BB = 4.5 MHz, baseband I/Q amplitude per tone = 0.5 V p-p differential		51.1		dBm
Output IP3	f1BB = 3.5 MHz, f2BB = 4.5 MHz, baseband I/Q amplitude per tone = 0.5 V p-p differential		23.1		dBm
Noise Floor	I/Q inputs = 0 V differential with a dc bias only, 20 MHz carrier offset		−157.6		dBm/Hz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LO = 5800 MHz					
Output Power, P_{OUT}	V_{IQ} = 1 V p-p differential		−1.36		dBm
Modulator Voltage Gain	RF output divided by baseband input voltage		−5.3		dB
Output P1dB			4.9		dBm
Output Return Loss			−7.4		dB
Carrier Feedthrough			−19.5		dBm
Sideband Suppression			−38.2		dBc
Quadrature Error			−0.51		Degrees
I/Q Amplitude Balance			−0.05		dB
Second Harmonic	$P_{OUT} − (f_{LO} + (2 \times f_{BB}))$, P_{OUT} = −1.36 dBm		−52.6		dBc
Third Harmonic	$P_{OUT} − (f_{LO} + (3 \times f_{BB}))$, P_{OUT} = −1.36 dBm		−45.7		dBc
Output IP2	f1BB = 3.5 MHz, f2BB = 4.5 MHz, baseband I/Q amplitude per tone = 0.5 V p-p differential		39.1		dBm
Output IP3	f1BB = 3.5 MHz, f2BB = 4.5 MHz, baseband I/Q amplitude per tone = 0.5 V p-p differential		14.6		dBm
Noise Floor	I/Q inputs = 0 V differential with a dc bias only, 20 MHz carrier offset		−153.0		dBm/Hz
LO INPUTS					
LO Drive Level	Characterization performed at typical level	−6	0	+6	dBm
Input Return Loss	500 MHz < f_{LO} < 3.3 GHz, see Figure 8 for return loss vs. frequency		≤−10		dB
BASEBAND INPUTS	Pin IBBP, Pin IBBN, Pin QBBP, Pin QBBN				
I/Q Input Bias Level[1]			500		mV
Absolute Voltage Level[1]	On Pin IBBP, Pin IBBN, Pin QBBP, Pin QBBN	0		1	V
Input Bias Current	Current sourcing from each baseband input		41		μA
Input Offset Current			0.1		μA
Differential Input Impedance			60		kΩ
Bandwidth (0.1 dB)	LO = 1900 MHz, baseband input = 500 mV p-p sine wave		95		MHz
OUTPUT DISABLE	Pin DSOP				
Off Isolation	P_{OUT} (DSOP low) − P_{OUT} (DSOP high)		84		dB
	DSOP high, LO leakage, LO = 2150 MHz		−55		dBm
Turn-On Settling Time	DSOP high to low (90% of envelope)		220		ns
Turn-Off Settling Time	DSOP low to high (10% of envelope)		100		ns
DSOP High Level (Logic 1)		2.0			V
DSOP Low Level (Logic 0)				0.8	V
POWER SUPPLIES	Pin VPS1 and Pin VPS2				
Voltage		4.75		5.25	V
Supply Current	DSOP = low		194		mA
	DSOP = high		126		mA

[1] The input bias level can vary as long as the voltages on the individual IBBP, IBBN, QBBP, and QBBN pins remain within the specified absolute voltage level.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, VPOS	5.5 V
IBBP, IBBN, QBBP, QBBN	0 V to 2 V
LOIP and LOIN	13 dBm
Internal Power Dissipation	1500 mW
θ_{JA} (Exposed Paddle Soldered Down)[1]	54°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−55°C to +105°C
Storage Temperature Range	−65°C to +150°C

[1] Per JDEC standard JESD 51-2.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

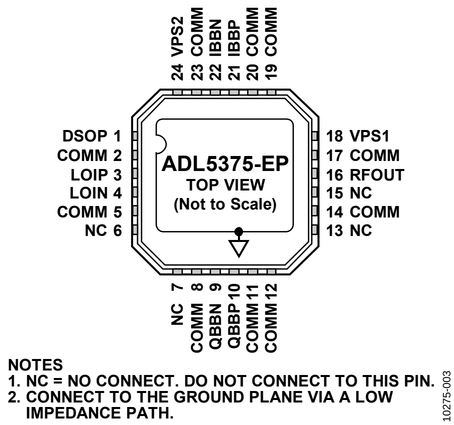

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	DSOP	Output Disable. A logic high on this pin disables the RF output. Connect this pin to ground or leave it floating to enable the output.
2, 5, 8, 11, 12, 14, 17, 19, 20, 23	COMM	Input Common Pins. Connect to the ground plane via a low impedance path.
3, 4	LOIP, LOIN	Local Oscillator Inputs. Single-ended operation: The LOIP pin is driven from the LO source through an ac-coupling capacitor while the LOIN pin is ac-coupled to ground through a capacitor. Differential operation: The LOIP and LOIN pins must be driven differentially through ac-coupling capacitors in this mode of operation.
6, 7, 13, 15,	NC	No Connect. These pins can be left open or tied to ground.
9, 10, 21, 22	QBBN, QBBP, IBBP, IBBN	Differential In-Phase and Quadrature Baseband Inputs. These high impedance inputs should be dc-biased to the recommended level (500 mV). These inputs should be driven from a low impedance source. Nominal characterized ac signal swing is 500 mV p-p on each pin. This results in a differential drive of 1 V p-p. These inputs are not self-biased and must be externally biased.
16	RFOUT	RF Output. Single-ended, 50 Ω internally biased RF output. RFOUT must be ac-coupled to the load.
18, 24	VPS1, VPS2	Positive Supply Voltage Pins. All pins should be connected to the same supply (V_S). To ensure adequate external bypassing, connect 0.1 µF and 100 pF capacitors between each pin and ground.
	EP	Exposed Paddle. Connect to the ground plane via a low impedance path.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V; T_A = 25°C; LO = 0 dBm single-ended drive; baseband I/Q amplitude = 1 V p-p differential sine waves in quadrature with a 500 mV dc bias; baseband I/Q frequency (f_{BB}) = 1 MHz, unless otherwise noted.

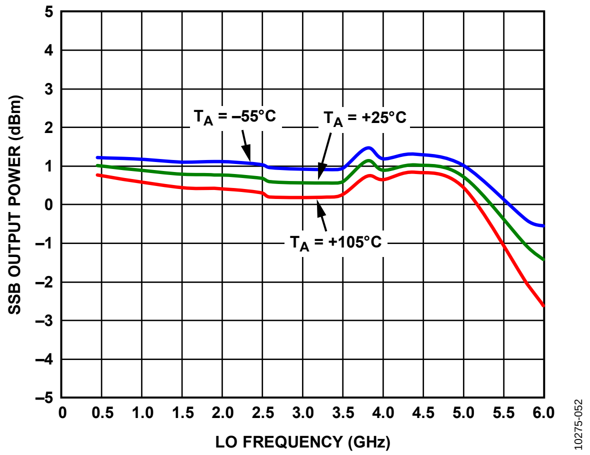

Figure 3. Single-Sideband (SSB) Output Power (P_{OUT}) vs. LO Frequency (f_{LO}) and Temperature

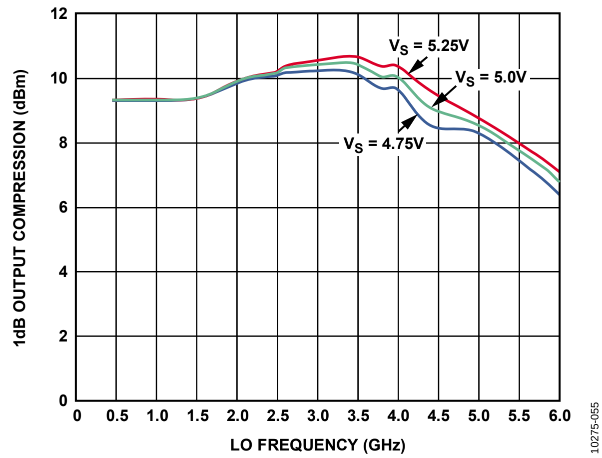

Figure 6. SSB Output 1dB Compression Point (OP1dB) vs. LO Frequency (f_{LO}) and Supply

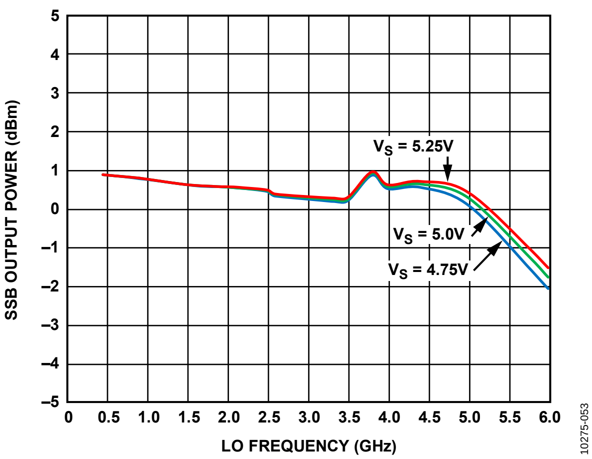

Figure 4. Single-Sideband (SSB) Output Power (P_{OUT}) vs. LO Frequency (f_{LO}) and Supply

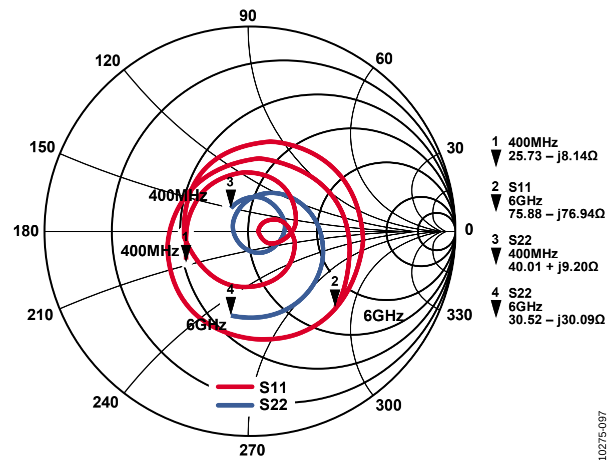

Figure 7. Smith Chart of LOIP (LOIN AC-Coupled to Ground) S11 and RFOUT S22 from 450 MHz to 6000 MHz

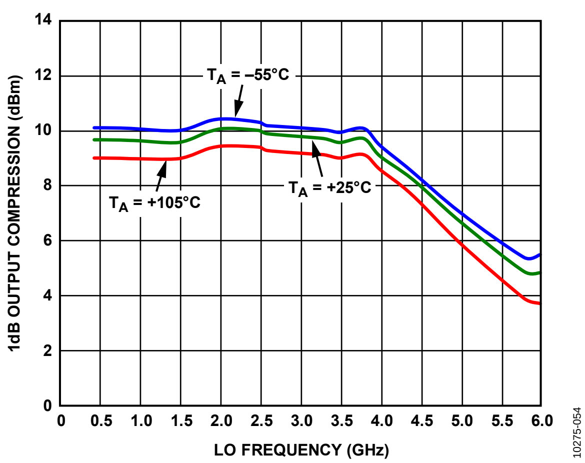

Figure 5. SSB Output 1dB Compression Point (OP1dB) vs. LO Frequency (f_{LO}) and Temperature

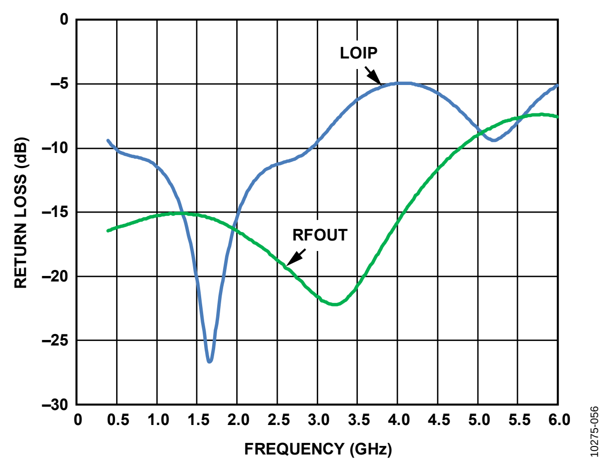

Figure 8. Return Loss of LOIP (LOIN AC-Coupled to Ground) S11 and RFOUT S22 from 450 MHz to 6000 MHz

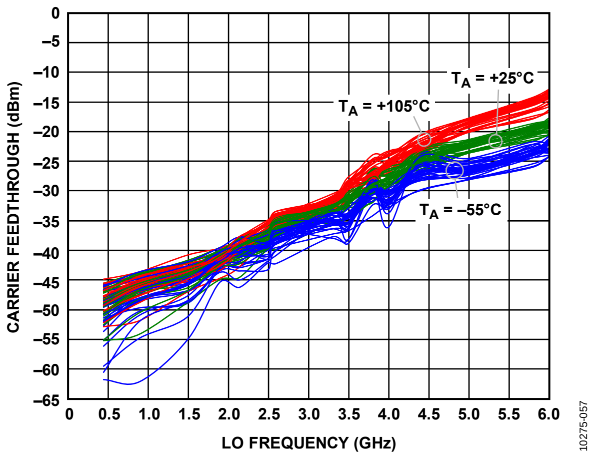

Figure 9. Carrier Feedthrough vs. LO Frequency (f_{LO}) and Temperature; Multiple Devices Shown

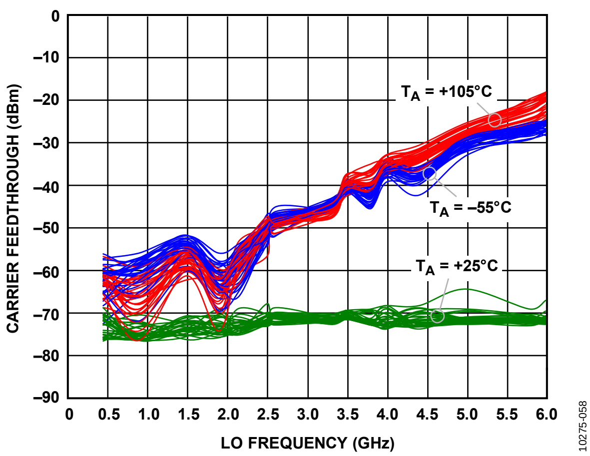

Figure 10. Carrier Feedthrough vs. LO Frequency (f_{LO}) and Temperature After Nulling at 25°C; Multiple Devices Shown

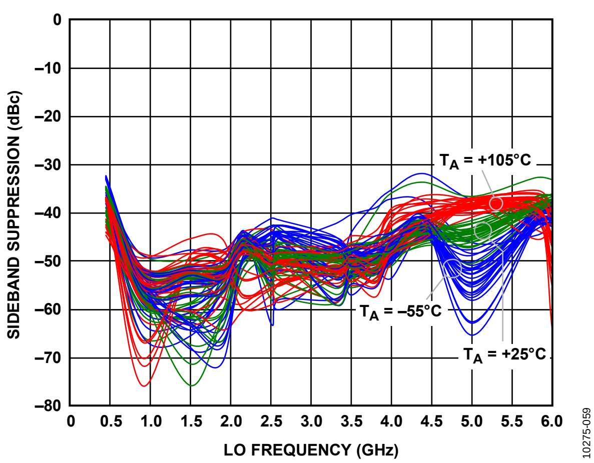

Figure 11. Sideband Suppression vs. LO Frequency (f_{LO}) and Temperature; Multiple Devices Shown

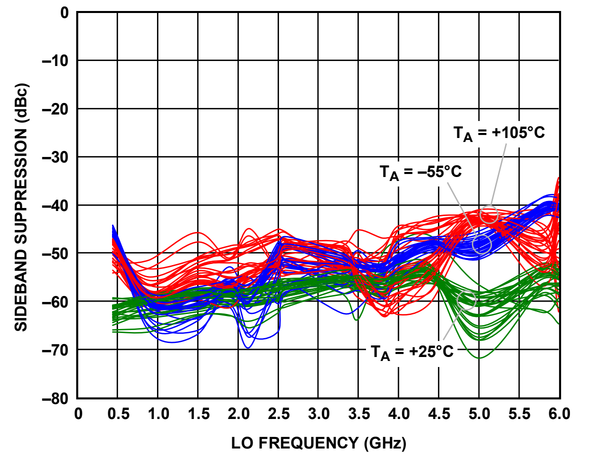

Figure 12. Sideband Suppression vs. LO Frequency (f_{LO}) and Temperature After Nulling at 25°C; Multiple Devices Shown

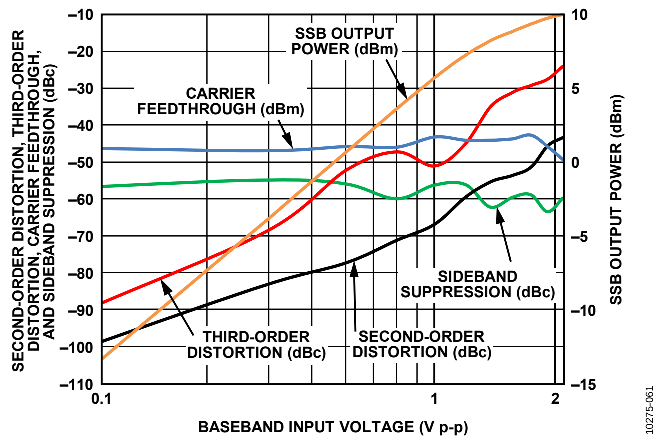

Figure 13. Second- and Third-Order Distortion, Carrier Feedthrough, Sideband Suppression, and SSB P_{OUT} vs. Baseband Differential Input Level (f_{LO} = 900 MHz)

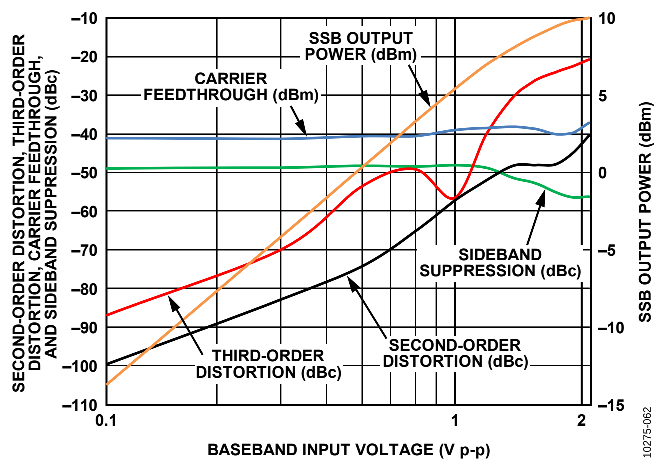

Figure 14. Second- and Third-Order Distortion, Carrier Feedthrough, Sideband Suppression, and SSB P_{OUT} vs. Baseband Differential Input Level (f_{LO} = 2150 MHz)

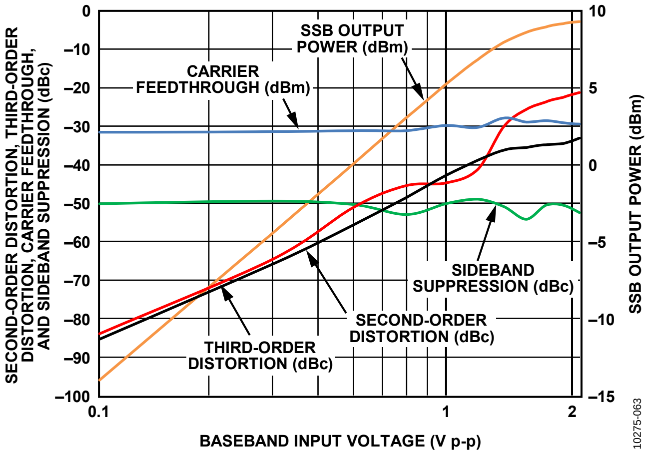

Figure 15. Second- and Third-Order Distortion, Carrier Feedthrough, Sideband Suppression, and SSB P_{OUT} vs. Baseband Differential Input Level (f_{LO} = 3500 MHz)

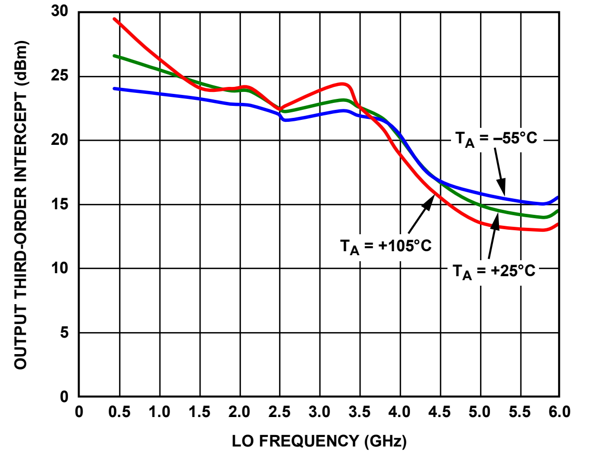

Figure 18. OIP3 vs. LO Frequency (f_{LO}) and Temperature (P_{OUT} ≈ −5 dBm)

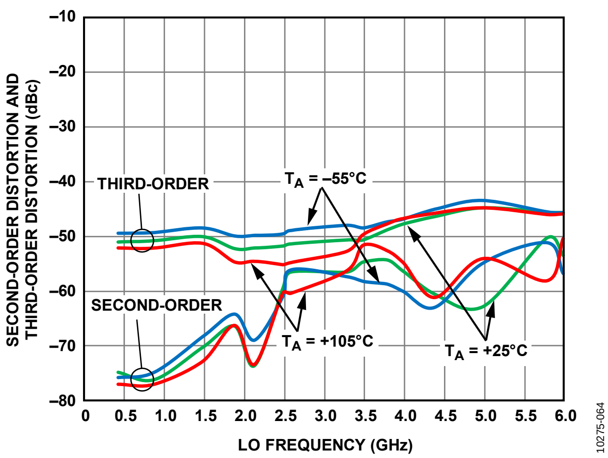

Figure 16. Second- and Third-Order Distortion vs. LO Frequency (f_{LO}) and Temperature (Baseband I/Q Amplitude = 1 V p-p Differential)

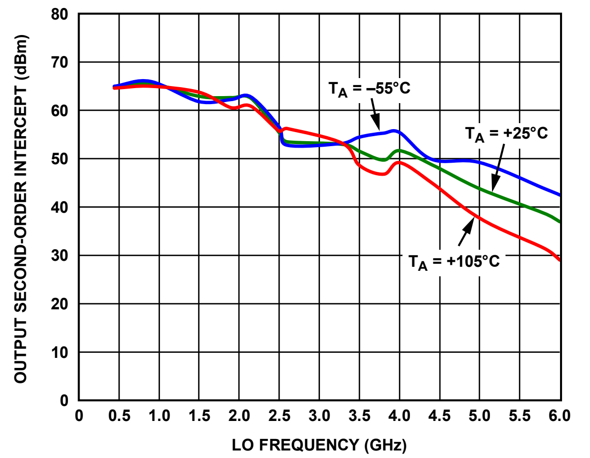

Figure 19. OIP2 vs. LO Frequency (f_{LO}) and Temperature (P_{OUT} ≈ −5 dBm)

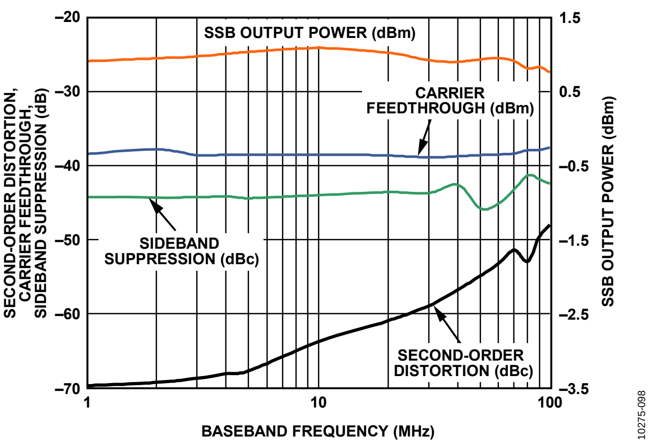

Figure 17. Second-Order Distortion, Carrier Feedthrough, Sideband Suppression, and SSB P_{OUT} vs. Baseband Frequency (f_{BB}); f_{LO} = 2140 MHz

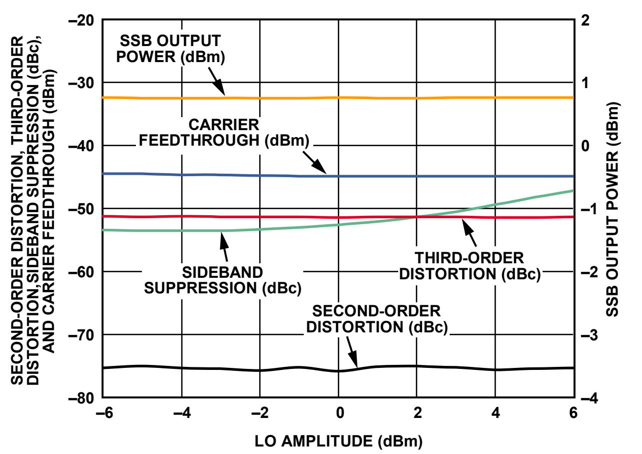

Figure 20. Second- and Third-Order Distortion, Carrier Feedthrough, Sideband Suppression, and SSB P_{OUT} vs. LO Amplitude (f_{LO} = 900 MHz)

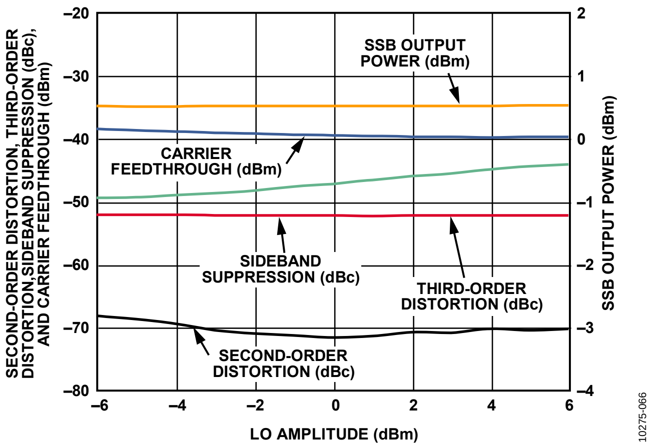

Figure 21. Second- and Third-Order Distortion, Carrier Feedthrough, Sideband Suppression, and SSB P_{OUT} vs. LO Amplitude (f_{LO} = 2150 MHz)

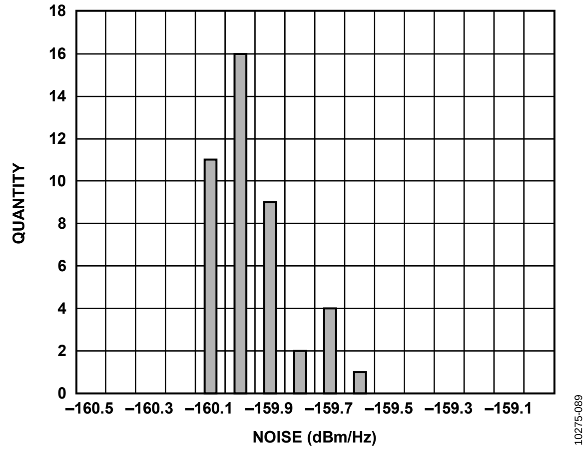

Figure 24. 20 MHz Offset Noise Floor Distribution at f_{LO} = 900 MHz (I/Q Amplitude = 0 mV p-p with 500 mV DC Bias)

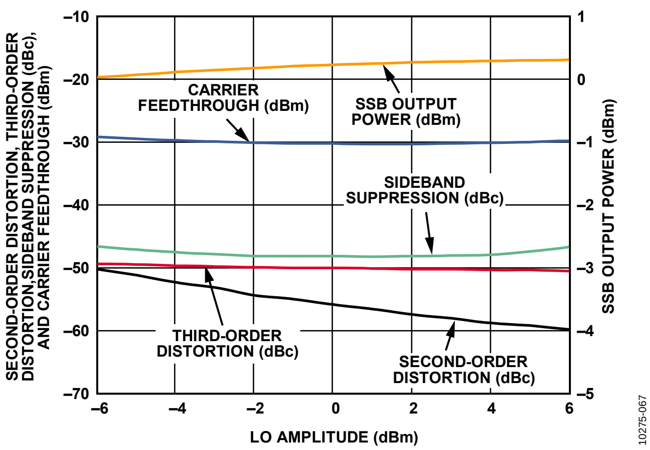

Figure 22. Second- and Third-Order Distortion, Carrier Feedthrough, Sideband Suppression, and SSB P_{OUT} vs. LO Amplitude (f_{LO} = 3500 MHz)

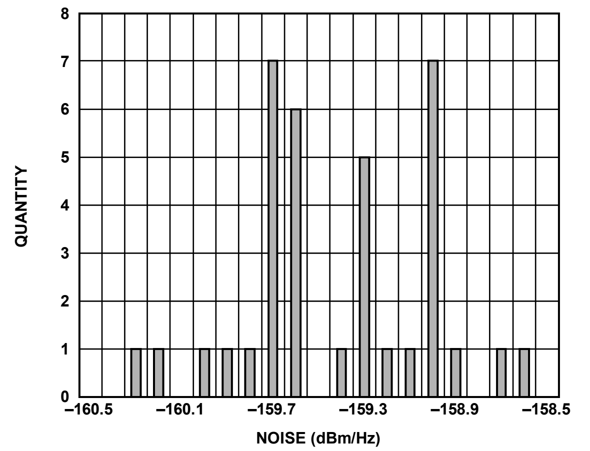

Figure 25. 20 MHz Offset Noise Floor Distribution at f_{LO} = 2140 MHz (I/Q Amplitude = 0 mV p-p with 500 mV DC Bias)

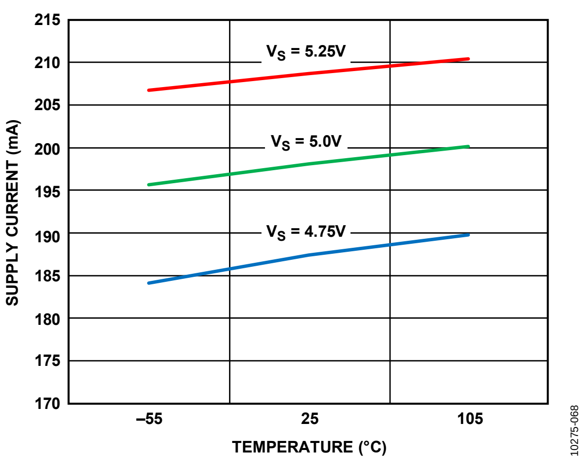

Figure 23. Power Supply Current vs. Temperature

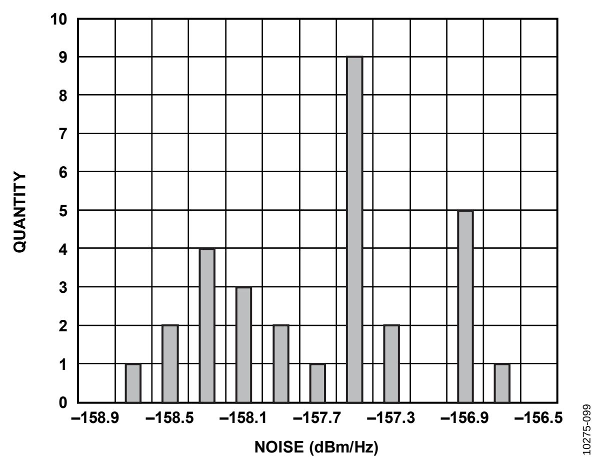

Figure 26. 20 MHz Offset Noise Floor Distribution at f_{LO} = 3500 MHz (I/Q Amplitude = 0 mV p-p with 500 mV DC Bias)

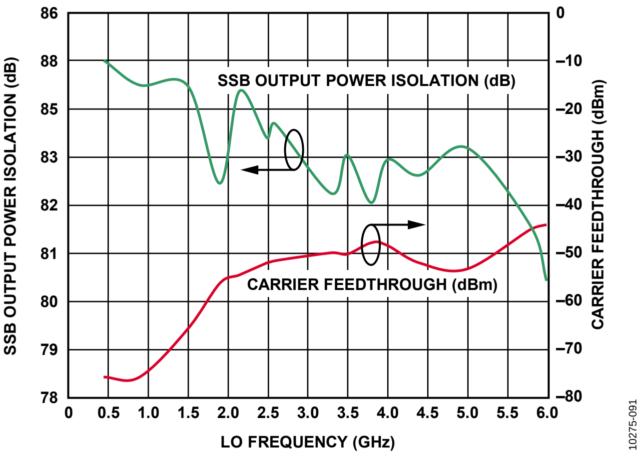

Figure 27. SSB P_{OUT} Isolation and Carrier Feedthrough with DSOP High

OUTLINE DIMENSIONS

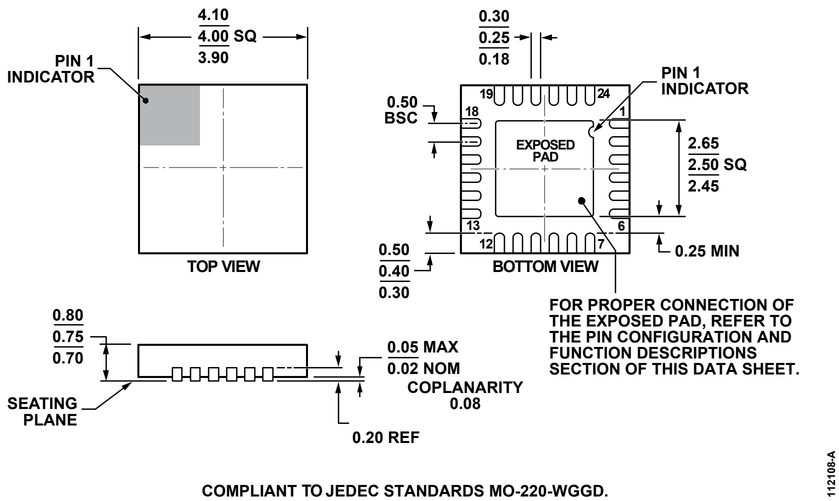

Figure 28. 24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-24-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADL5375-05SCPZEPR7	−55°C to +105°C	24-Lead LFCSP_WQ, 7" Tape and Reel	CP-24-7
ADL5375-05SCPZEPWP	−55°C to +105°C	24-Lead LFCSP_WQ, Waffle Pack	CP-24-7
ADL5375-05EP-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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