Dual 3 MHz, 800 mA Buck Regulators with One 300 mA LDO

Data Sheet

ADP5023

FEATURES

Main input voltage range: 2.3 V to 5.5 V
Two 800 mA buck regulators and one 300 mA LDO
24-lead, 4 mm × 4 mm LFCSP package
Regulator accuracy: ±1.8%
Factory programmable or external adjustable VOUTx
3 MHz buck operation with forced PWM and auto PWM/PSM modes
BUCK1/BUCK2: output voltage range from 0.8 V to 3.8 V
LDO: output voltage range from 0.8 V to 5.2 V
LDO: input supply voltage from 1.7 V to 5.5 V
LDO: high PSRR and low output noise

APPLICATIONS

Power for processors, ASIC, FPGAs, and RF chipsets
Portable instrumentation and medical devices
Space constrained devices

GENERAL DESCRIPTION

The ADP5023 combines two high performance buck regulators and one low dropout (LDO) regulator in a small, 24-lead 4 mm × 4 mm LFCSP to meet demanding performance and board space requirements.

The high switching frequency of the buck regulators enables tiny multilayer external components and minimizes the board space. When the MODE pin is set high, the buck regulators operate in forced PWM mode. When the MODE pin is set low, the buck regulators operate in PWM mode when the load current is above a predefined threshold. When the load current falls below a predefined threshold, the regulator operates in power save mode (PSM) improving the light-load efficiency.

The two bucks operate out of phase to reduce the input capacitor requirement. The low quiescent current, low dropout voltage, and wide input voltage range of the ADP5023 LDO extends the battery life of portable devices. The ADP5023 LDO maintains power supply rejection greater than 60 dB for frequencies as high as 10 kHz while operating with a low headroom voltage.

Regulators in the ADP5023 are activated though dedicated enable pins. The default output voltages can be externally set in the adjustable version or factory programmable to a wide range of preset values in the fixed voltage version.

TYPICAL APPLICATION CIRCUIT

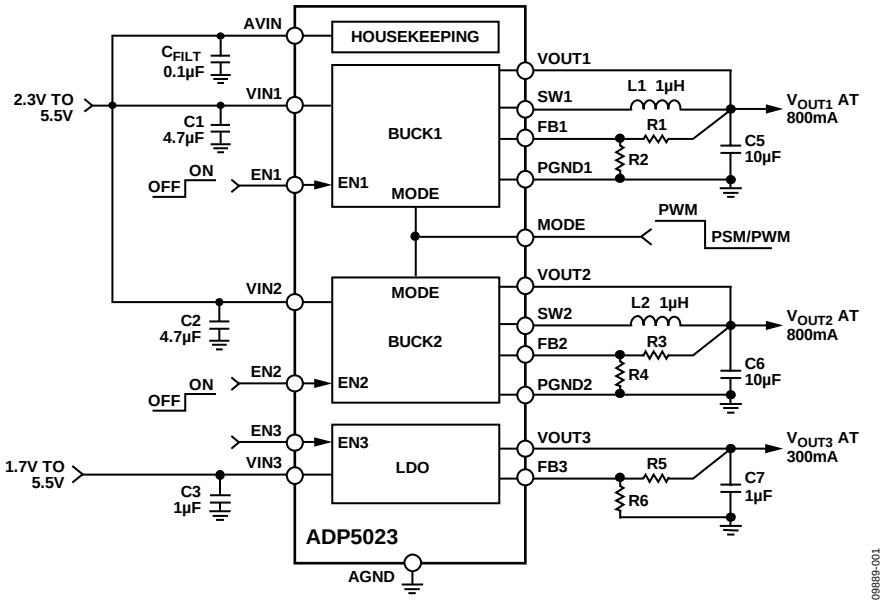


Figure 1.

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
©2011-2013 Analog Devices, Inc. All rights reserved.

TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Typical Application Circuit ... 1
Revision History ... 2
Specifications ... 3
General Specifications ... 3
BUCK1 and BUCK2 Specifications ... 4
LDO Specifications ... 5
Input and Output Capacitor, Recommended Specifications ... 5
Absolute Maximum Ratings ... 6
Thermal Resistance ... 6
ESD Caution ... 6
Pin Configuration and Function Descriptions ... 7
Typical Performance Characteristics ... 8
Theory of Operation ... 15
Power Management Unit ... 15
BUCK1 and BUCK2 ... 17
LDO ... 18
Applications Information ... 19
Buck External Component Selection ... 19
LDO External Component Selection ... 21
Power Dissipation and Thermal Considerations ... 22
Buck Regulator Power Dissipation ... 22
Junction Temperature ... 23
PCB Layout Guidelines ... 24
Typical Application Schematics ... 25
Bill of Materials ... 26
Outline Dimensions ... 27
Ordering Guide ... 27

REVISION HISTORY

1/13—Rev. B to Rev. C

Changes to Figure 9 ... 10
Changes to Ordering Guide ... 28

9/12—Rev. A to Rev. B

Changes to Feature Section ... 1
Changes to BUCK Output Voltage Accuracy Parameter and Voltage Feedback Parameter, Table 2 ... 4
Changes to LDO Output Voltage Accuracy Parameter and Voltage Feedback Parameter, Table 3 ... 5
Changes to Figure 6 to Figure 8 ... 8
Changes to Figure 30 and Figure 31 ... 12
Changes to Figure 34 and Figure 38 Caption ... 13
Changes to Undervoltage Lockout Section ... 16
Moved Power Dissipation and Thermal Consideration Section ... 22
Changes to Buck Regulator Power Dissipation Section ... 22
Updated Outline Dimensions ... 27

1/12—Rev. 0 to Rev. A

Changes to Features Section ... 1
Changes to Table 2 ... 4
Changes to Table 3 and Table 4 ... 5
Changes to Table 5 ... 6
Changes to Table 7 ... 7
Changes to Figure 34 ... 13
Changes to Buck Regulator Power Dissipation Section ... 15
Changes to Undervoltage Lockout Section ... 18
Changes to LDO Section and Figure 48 ... 20
Changes to Table 9 ... 22
Changes to Figure 52 ... 25
Changes to Ordering Guide ... 27

8/11—Revision 0: Initial Version

SPECIFICATIONS

GENERAL SPECIFICATIONS

V_{AVIN} = V_{IN1} = V_{IN2} = 2.3 V to 5.5 V; V_{IN3} = 1.7 V to 5.5 V; T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{AVIN}, V_{IN1}, V_{IN2}		2.3		5.5	V
THERMAL SHUTDOWN						
Threshold	TS_{SD}	T_J rising		150		°C
Hysteresis	TS_{SD-HYS}			20		°C
START-UP TIME[1]						
BUCK1, LDO	t_{START1}			250		µs
BUCK2	t_{START2}			300		µs
EN1, EN2, EN3, MODE INPUTS						
Input Logic High	V_{IH}		1.1			V
Input Logic Low	V_{IL}				0.4	V
Input Leakage Current	$V_{I-LEAKAGE}$			0.05	1	µA
INPUT CURRENT						
All Channels Enabled	$I_{STBY-NOSW}$	No load, no buck switching		108	175	µA
All Channels Disabled	$I_{SHUTDOWN}$	T_J = −40°C to +85°C		0.3	1	µA
VIN1 UNDERVOLTAGE LOCKOUT						
High UVLO Input Voltage Rising	$UVLO_{VIN1RISE}$				3.9	V
High UVLO Input Voltage Falling	$UVLO_{VIN1FALL}$		3.1			V
Low UVLO Input Voltage Rising	$UVLO_{VIN1RISE}$				2.275	V
Low UVLO Input Voltage Falling	$UVLO_{VIN1FALL}$		1.95			V

[1] Start-up time is defined as the time from EN1 = EN2 = EN3 from 0 V to V_{AVIN} to VOUT1, VOUT2, and VOUT3 reaching 90% of their nominal level. Start-up times are shorter for individual channels if another channel is already enabled. See the Typical Performance Characteristics section for more information.

BUCK1 AND BUCK2 SPECIFICATIONS

V_{AVIN} = V_{IN1} = V_{IN2} = 2.3 V to 5.5 V; T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.[1]

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS						
Output Voltage Accuracy	$\Delta V_{OUT1}/V_{OUT1}$, $\Delta V_{OUT2}/V_{OUT2}$	PWM mode; I_{LOAD1} = I_{LOAD2} = 0 mA	−1.8		+1.8	%
Line Regulation	$(\Delta V_{OUT1}/V_{OUT1})/\Delta V_{IN1}$, $(\Delta V_{OUT2}/V_{OUT2})/\Delta V_{IN2}$	PWM mode		−0.05		%/V
Load Regulation	$(\Delta V_{OUT1}/V_{OUT1})/\Delta I_{OUT1}$, $(\Delta V_{OUT2}/V_{OUT2})/\Delta I_{OUT2}$	PWM mode; I_{LOAD} = 0 mA to 800 mA		−0.1		%/A
VOLTAGE FEEDBACK	V_{FB1}, V_{FB2}	Models with adjustable outputs	0.491	0.5	0.509	V
OPERATING SUPPLY CURRENT		MODE = ground				
BUCK1 Only	I_{IN}	I_{LOAD1} = 0 mA, device not switching, all other channels disabled		44		µA
BUCK2 Only	I_{IN}	I_{LOAD2} = 0 mA, device not switching, all other channels disabled		55		µA
BUCK1 and BUCK2	I_{IN}	I_{LOAD1} = I_{LOAD2} = 0 mA, device not switching, LDO channels disabled		67		µA
PSM CURRENT THRESHOLD	I_{PSM}	PSM to PWM operation		100		mA
SW CHARACTERISTICS						
SW On Resistance	R_{NFET}	V_{IN1} = V_{IN2} = 3.6 V		155	240	mΩ
	R_{PFET}	V_{IN1} = V_{IN2} = 3.6 V		205	310	mΩ
	R_{NFET}	V_{IN1} = V_{IN2} = 5.5 V		137	204	mΩ
	R_{PFET}	V_{IN1} = V_{IN2} = 5.5 V		162	243	mΩ
Current Limit	I_{LIMIT1}, I_{LIMIT2}	pFET switch peak current limit	1600	1950	2300	mA
ACTIVE PULL-DOWN	R_{PDWN-B}	Channel disabled		75		Ω
OSCILLATOR FREQUENCY	f_{SW}		2.5	3.0	3.5	MHz

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).

LDO SPECIFICATIONS

V_{IN3} = (V_{OUT3} + 0.5 V) or 1.7 V (whichever is greater) to 5.5 V; C_{IN} = C_{OUT} = 1 µF; T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.[1]

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN3}		1.7		5.5	V
OPERATING SUPPLY CURRENT						
Bias Current per LDO[2]	$I_{VIN3BIAS}$	I_{OUT3} = 0 µA		10	30	µA
		I_{OUT3} = 10 mA		60	100	µA
		I_{OUT3} = 300 mA		165	245	µA
Total System Input Current	I_{IN}	Includes all current into AVIN, VIN1, VIN2, and VIN3				
LDO Only		I_{OUT3} = 0 µA, all other channels disabled		53		µA
OUTPUT CHARACTERISTICS						
Output Voltage Accuracy	$\Delta V_{OUT3}/V_{OUT3}$	100 µA < I_{OUT3} < 300 mA	−1.8		+1.8	%
Line Regulation	$(\Delta V_{OUT3}/V_{OUT3})/\Delta V_{IN3}$	I_{OUT3} = 1 mA	−0.03		+0.03	%/V
Load Regulation[3]	$(\Delta V_{OUT3}/V_{OUT3})/\Delta I_{OUT3}$	I_{OUT3} = 1 mA to 300 mA		0.001	0.003	%/mA
VOLTAGE FEEDBACK	V_{FB3}		0.491	0.5	0.509	V
DROPOUT VOLTAGE[4]	$V_{DROPOUT}$	V_{OUT3} = 5.2 V, I_{OUT3} = 300 mA		50		mV
		V_{OUT3} = 3.3 V, I_{OUT3} = 300 mA		75	140	mV
		V_{OUT3} = 2.5 V, I_{OUT3} = 300 mA		100		mV
		V_{OUT3} = 1.8 V, I_{OUT3} = 300 mA		180		mV
CURRENT-LIMIT THRESHOLD[5]	I_{LIMIT3}		335	600		mA
ACTIVE PULL-DOWN	R_{PDWN-L}	Channel disabled		600		Ω
OUTPUT NOISE						
Regulator LDO	$NOISE_{LDO}$	10 Hz to 100 kHz, V_{IN3} = 5 V, V_{OUT3} = 2.8 V		100		µV rms
POWER SUPPLY REJECTION RATIO	PSRR					
Regulator LDO		10 kHz, V_{IN3} = 3.3 V, V_{OUT3} = 2.8 V, I_{OUT3} = 1 mA		60		dB
		100 kHz, V_{IN3} = 3.3 V, V_{OUT3} = 2.8 V, I_{OUT3} = 1 mA		62		dB
		1 MHz, V_{IN3} = 3.3 V, V_{OUT3} = 2.8 V, I_{OUT3} = 1 mA		63		dB

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).
[2] This is the input current into VIN3, which is not delivered to the output load.
[3] Based on an endpoint calculation using 1 mA and 300 mA loads.
[4] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only to output voltages above 1.7 V.
[5] Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.0 V, or 2.7 V.

INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

T_A = −40°C to +125°C, unless otherwise specified.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
NOMINAL INPUT AND OUTPUT CAPACITOR RATINGS					
BUCK1, BUCK2 Input Capacitor Ratings	C_{MIN1}, C_{MIN2}	4.7		40	µF
BUCK1, BUCK2 Output Capacitor Ratings	C_{MIN1}, C_{MIN2}	10		40	µF
LDO[1] Input and Output Capacitor Ratings	C_{MIN3}, C_{MIN4}	1.0			µF
CAPACITOR ESR	R_{ESR}	0.001		1	Ω

[1] The minimum input and output capacitance should be greater than 0.70 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R- and X5R-type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use because of their poor temperature and dc bias characteristics.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
AVIN to AGND	−0.3 V to +6 V
VIN1, VIN2 to AVIN	−0.3 V to +0.3 V
PGND1, PGND2 to AGND	−0.3 V to +0.3 V
VIN3, VOUT1, VOUT2, FB1, FB2, FB3, EN1, EN2, EN3, MODE to AGND	−0.3 V to (AVIN + 0.3 V)
VOUT3 to AGND	−0.3 V to (VIN3 + 0.3 V)
SW1 to PGND1	−0.3 V to (VIN1 + 0.3 V)
SW2 to PGND2	−0.3 V to (VIN2 + 0.3 V)
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

For detailed information on power dissipation, see the Power Dissipation and Thermal Considerations section.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

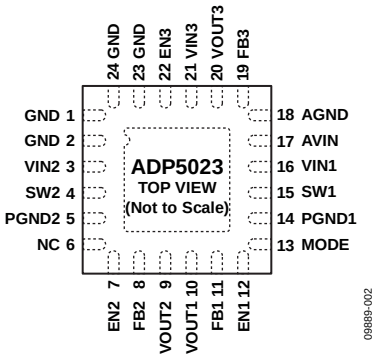
Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
24-Lead, 0.5 mm pitch LFCSP	35	3	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. IT IS RECOMMENDED THAT THE EXPOSED PAD BE SOLDERED TO THE GROUND PLANE.

Figure 2. Pin Configuration—View from Top of Die

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	AGND	Analog Ground.
2	AGND	Analog Ground.
3	VIN2	BUCK2 Input Supply (2.3 V to 5.5 V). Connect VIN2 to VIN1 and AVIN.
4	SW2	BUCK2 Switching Node.
5	PGND2	Dedicated Power Ground for BUCK2.
6	NC	No Connect. Leave this pin unconnected.
7	EN2	BUCK2 Enable Pin. High level turns on this regulator, and low level turns it off.
8	FB2	BUCK2 Feedback Input. For device models with adjustable output voltage, connect this pin to the middle of the BUCK2 resistor divider. For device models with fixed output voltage, leave this pin unconnected.
9	VOUT2	BUCK2 Output Voltage Sensing Input. Connect VOUT2 to the top of the capacitor on VOUT2.
10	VOUT1	BUCK1 Output Voltage Sensing Input. Connect VOUT1 to the top of the capacitor on VOUT1.
11	FB1	BUCK1 Feedback Input. For device models with adjustable output voltage, connect this pin to the middle of the BUCK1 resistor divider. For device models with fixed output voltage, connect this pin to the top of the capacitor on VOUT3.
12	EN1	BUCK1 Enable Pin. High level turns on this regulator, and low level turns it off.
13	MODE	BUCK1/BUCK2 Operating Mode. MODE = high: forced PWM operation. MODE = low: auto PWM/PSM operation.
14	PGND1	Dedicated Power Ground for BUCK1.
15	SW1	BUCK1 Switching Node
16	VIN1	BUCK1 Input Supply (2.3 V to 5.5 V). Connect VIN1 to VIN2 and AVIN.
17	AVIN	Analog Input Supply (2.3 V to 5.5 V). Connect AVIN to VIN1 and VIN2.
18	AGND	Analog Ground.
19	FB3	LDO Feedback Input. For device models with adjustable output voltage, connect this pin to the middle of the LDO resistor divider. For device models with fixed output voltage, leave this pin unconnected.
20	VOUT3	LDO Output Voltage.
21	VIN3	LDO Input Supply (1.7 V to 5.5 V).
22	EN3	LDO Enable Pin. High level turns on this regulator, and low level turns it off.
23	AGND	Analog Ground.
24	AGND	Analog Ground.
	EPAD (EP)	Exposed Pad. It is recommended that the exposed pad be soldered to the ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN1} = V_{IN2} = V_{IN3} = 3.6$ V, $T_A = 25°C$, unless otherwise noted.

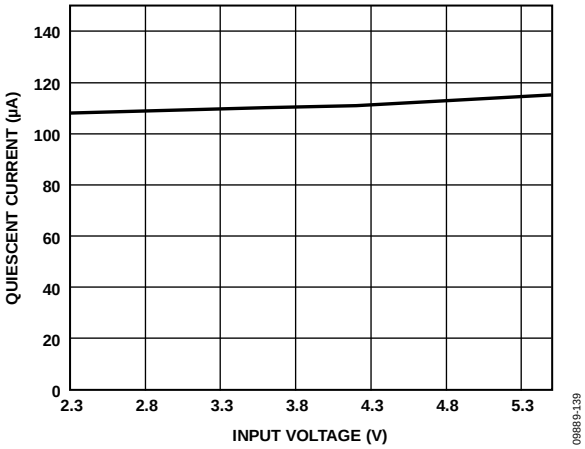


Figure 3. System Quiescent Current vs. Input Voltage, $V_{OUT1} = 3.3$ V, $V_{OUT2} = 1.8$ V, $V_{OUT3} = 1.2$ V, $V_{OUT4} = 3.3$ V, All Channels Unloaded

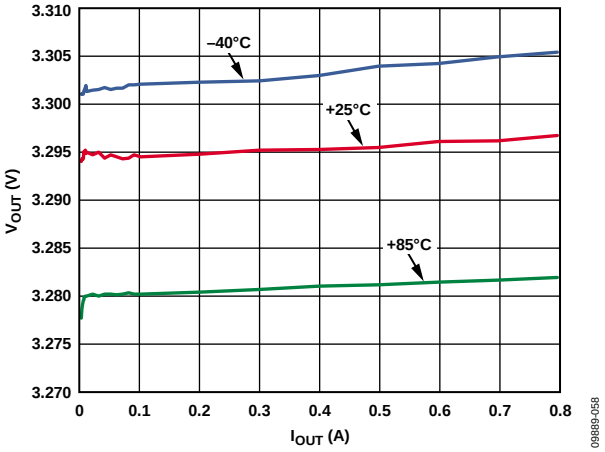


Figure 6. BUCK1 Load Regulation Across Temperature, $V_{IN} = 4.2$ V, $V_{OUT1} = 3.3$ V, PWM Mode

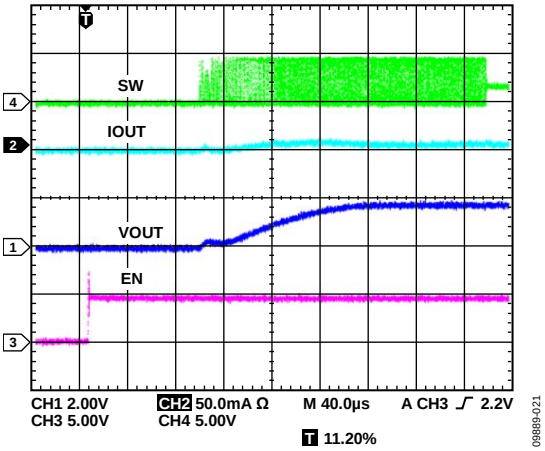


Figure 4. BUCK1 Startup, $V_{OUT1} = 1.8$ V, $I_{OUT1} = 5$ mA

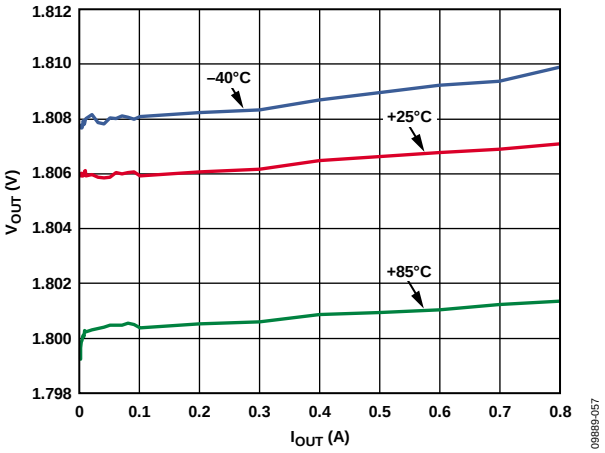


Figure 7. BUCK2 Load Regulation Across Temperature, $V_{IN} = 3.6$ V, $V_{OUT2} = 1.8$ V, PWM Mode

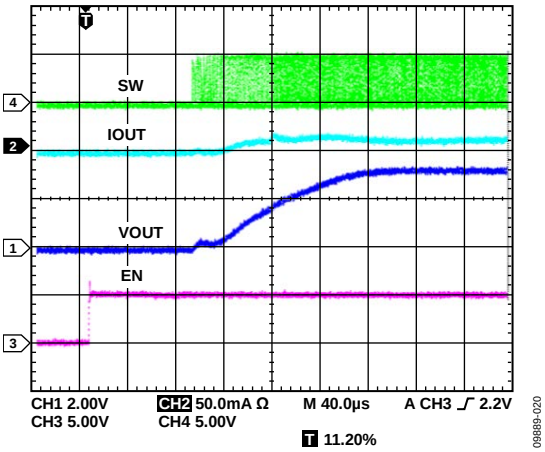


Figure 5. BUCK2 Startup, $V_{OUT2} = 3.3$ V, $I_{OUT2} = 10$ mA

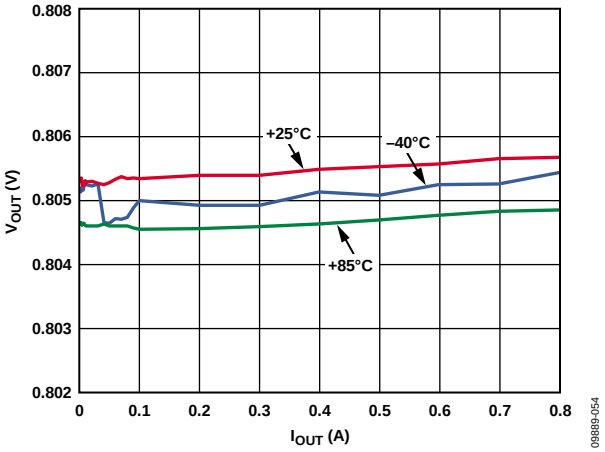


Figure 8. BUCK1 Load Regulation Across Temperature, $V_{IN} = 3.6$ V, $V_{OUT1} = 0.8$ V, PWM Mode

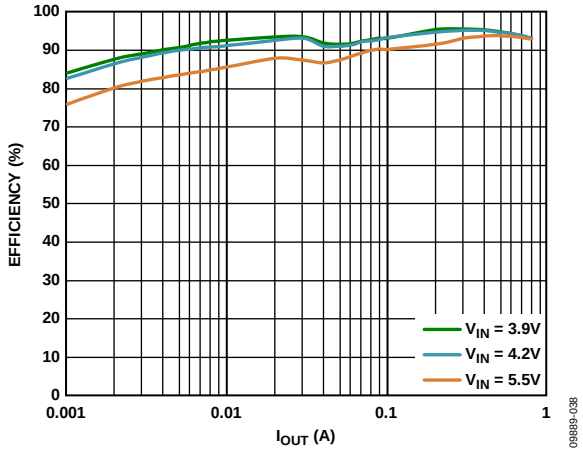


Figure 9. BUCK1 Efficiency vs. Load Current, Across Input Voltage, V_{OUT1} = 3.3 V, Auto Mode

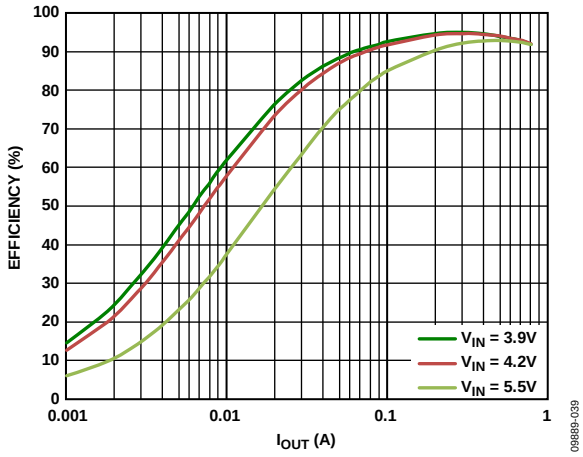


Figure 10. BUCK1 Efficiency vs. Load Current, Across Input Voltage, V_{OUT1} = 3.3 V, PWM Mode

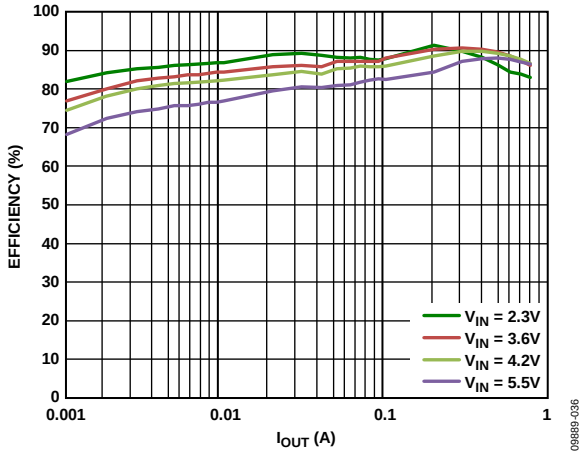


Figure 11. BUCK2 Efficiency vs. Load Current, Across Input Voltage, V_{OUT2} = 1.8 V, Auto Mode

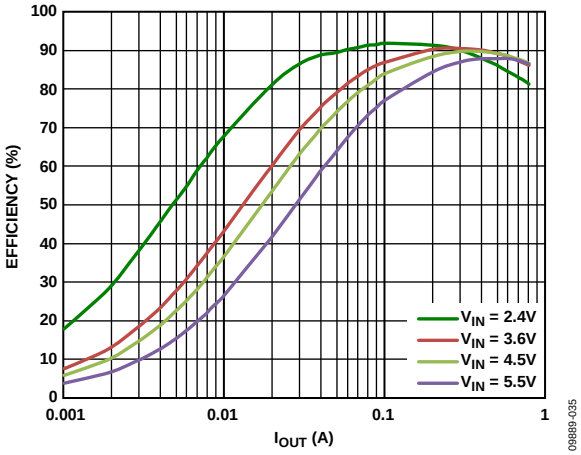


Figure 12. BUCK2 Efficiency vs. Load Current, Across Input Voltage, V_{OUT2} = 1.8 V, PWM Mode

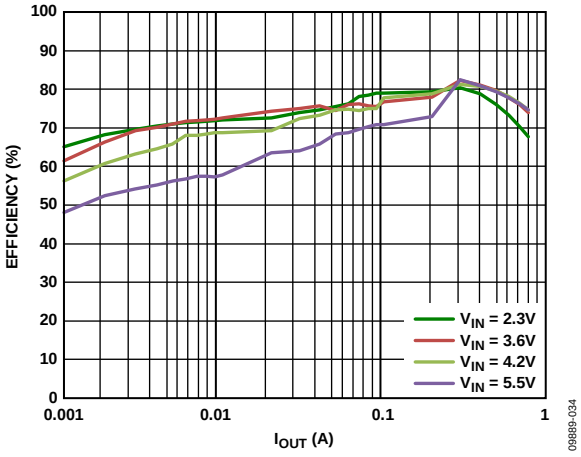


Figure 13. BUCK1 Efficiency vs. Load Current, Across Input Voltage, V_{OUT1} = 0.8 V, Auto Mode

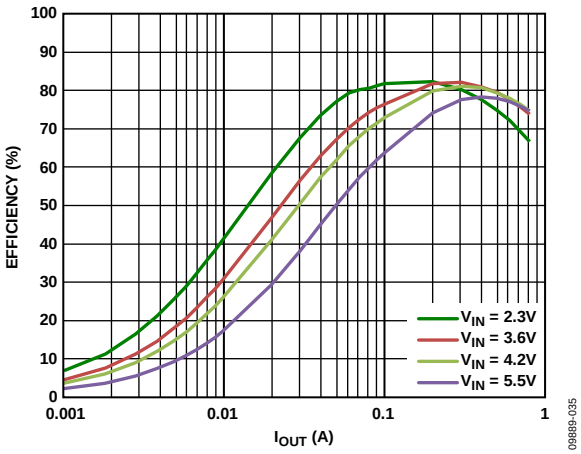


Figure 14. BUCK1 Efficiency vs. Load Current, Across Input Voltage, V_{OUT1} = 0.8 V, PWM Mode

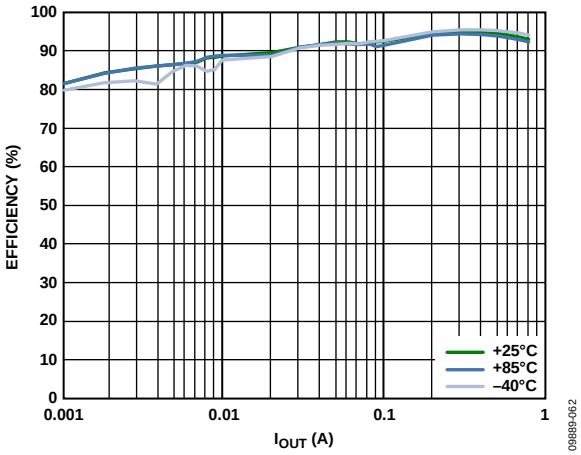


Figure 15. BUCK1 Efficiency vs. Load Current, Across Temperature, V_{IN} = 3.9 V, V_{OUT1} = 3.3 V, Auto Mode

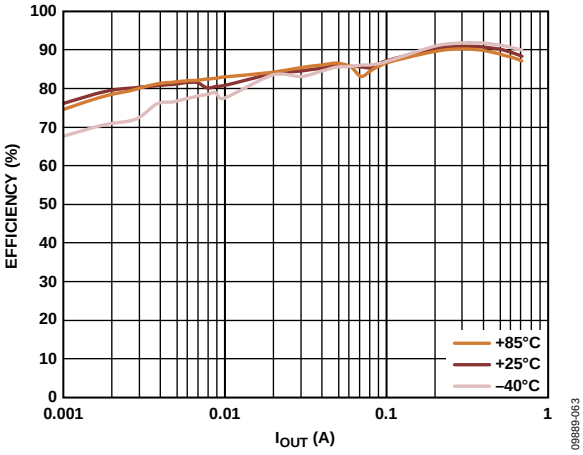


Figure 16. BUCK2 Efficiency vs. Load Current, Across Temperature, V_{OUT2} = 1.8 V, Auto Mode

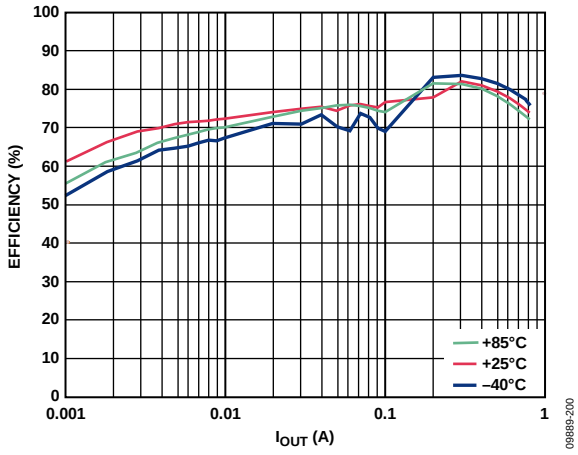


Figure 17. BUCK1 Efficiency vs. Load Current, Across Temperature, V_{OUT1} = 0.8 V, Auto Mode

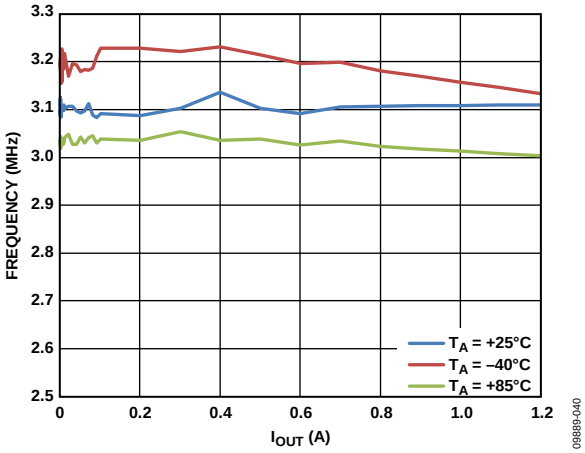


Figure 18. BUCK2 Switching Frequency vs. Output Current, Across Temperature, V_{OUT2} = 1.8 V, PWM Mode

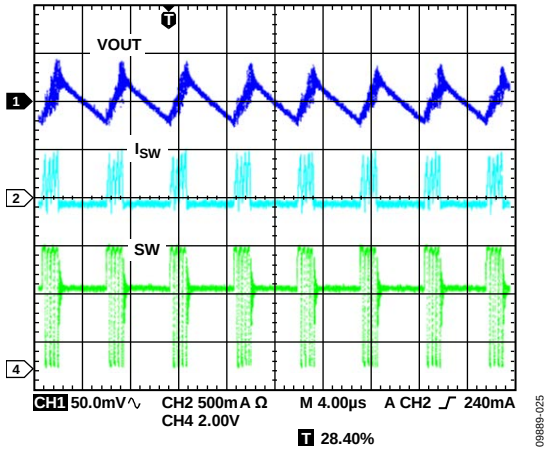


Figure 19. Typical Waveforms, V_{OUT1} = 3.3 V, I_{OUT1} = 30 mA, Auto Mode

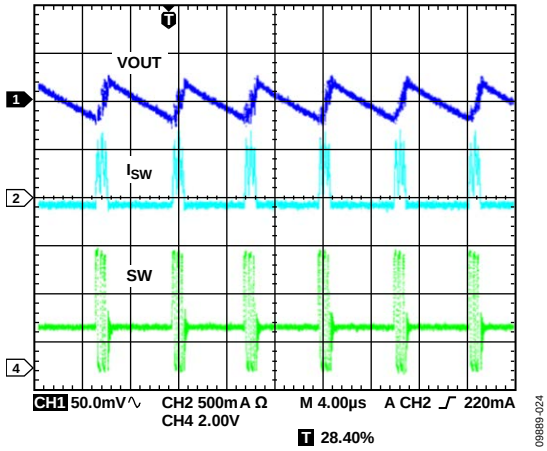


Figure 20. Typical Waveforms, V_{OUT2} = 1.8 V, I_{OUT2} = 30 mA, Auto Mode

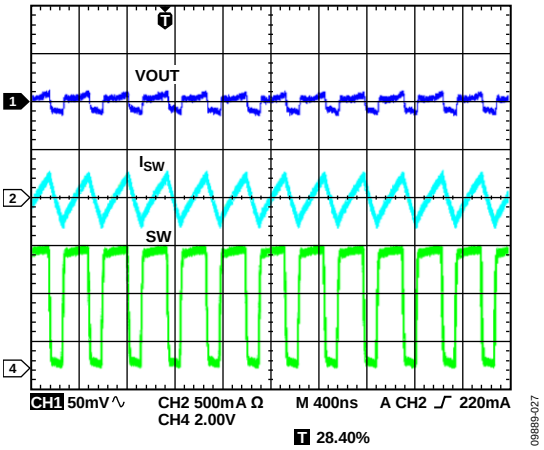


Figure 21. Typical Waveforms, V_{OUT1} = 3.3 V, I_{OUT1} = 30 mA, PWM Mode

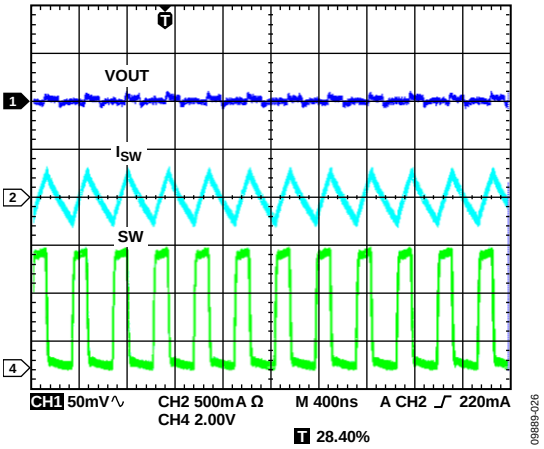


Figure 22. Typical Waveforms, V_{OUT2} = 1.8 V, I_{OUT2} = 30 mA, PWM Mode

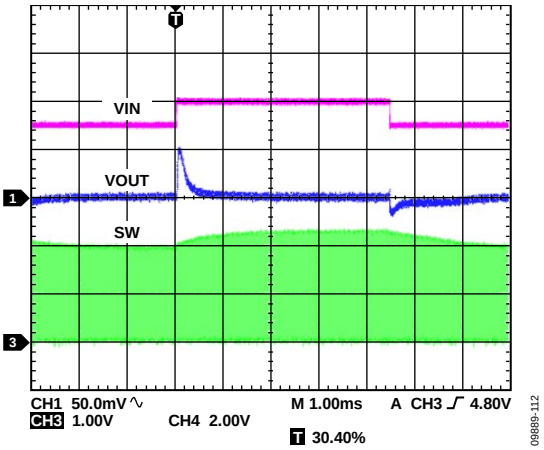


Figure 23. BUCK1 Response to Line Transient, V_{IN} = 4.5 V to 5.0 V, V_{OUT1} = 3.3 V, PWM Mode

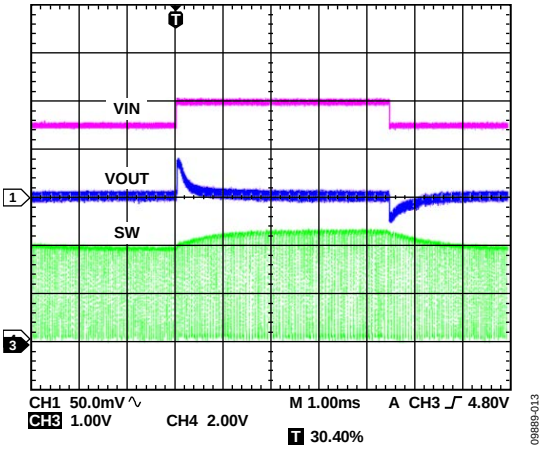


Figure 24. BUCK2 Response to Line Transient, V_{IN} = 4.5 V to 5.0 V, V_{OUT2} = 1.8 V, PWM Mode

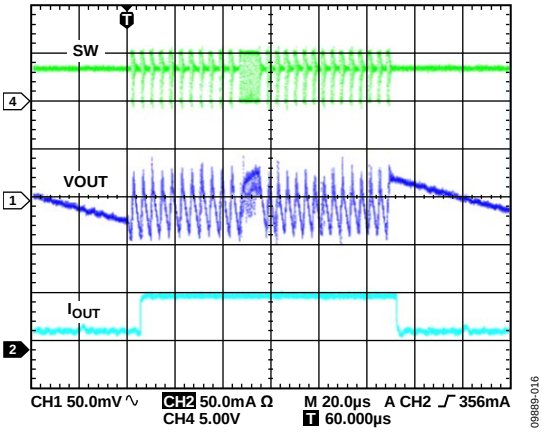


Figure 25. BUCK1 Response to Load Transient, I_{OUT1} = 1 mA to 50 mA, V_{OUT1} = 3.3 V, Auto Mode

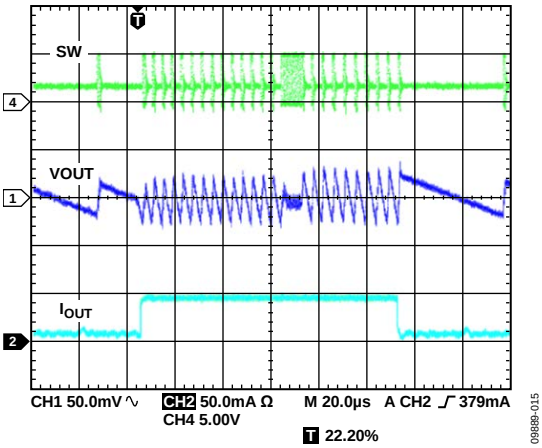


Figure 26. BUCK2 Response to Load Transient, I_{OUT2} = 1 mA to 50 mA, V_{OUT2} = 1.8 V, Auto Mode

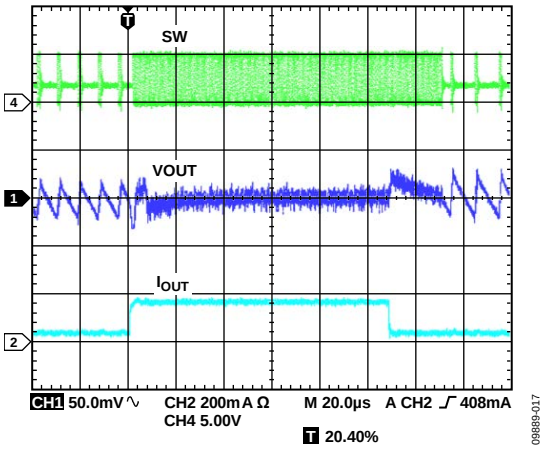


Figure 27. BUCK1 Response to Load Transient, I_{OUT1} = 20 mA to 180 mA, V_{OUT1} = 3.3 V, Auto Mode

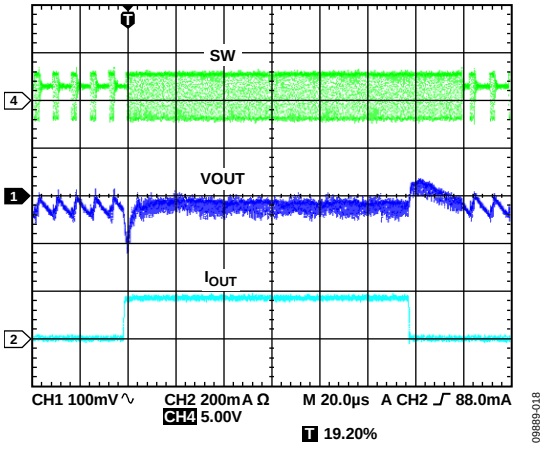


Figure 28. BUCK2 Response to Load Transient, I_{OUT2} = 20 mA to 180 mA, V_{OUT2} = 1.8 V, Auto Mode

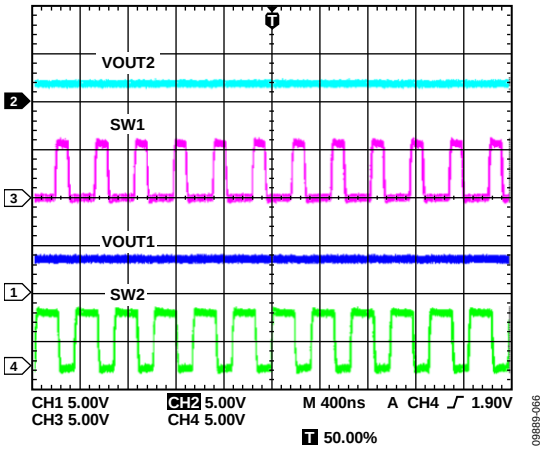


Figure 29. VOUT and SW Waveforms for BUCK1 and BUCK2 in PWM Mode Showing Out-of-Phase Operation

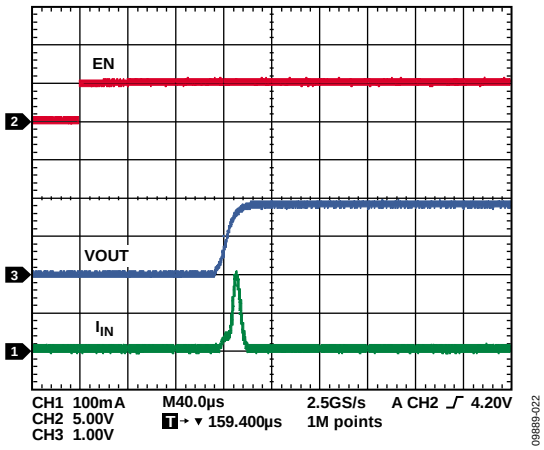


Figure 30. LDO Startup, V_{OUT3} = 1.8 V

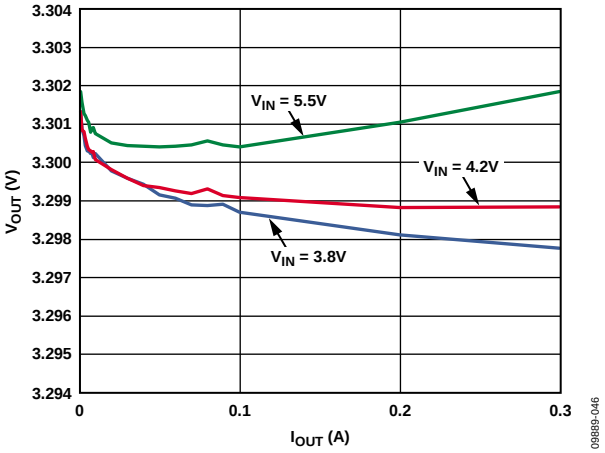


Figure 31. LDO Load Regulation Across Input Voltage, V_{OUT3} = 3.3 V

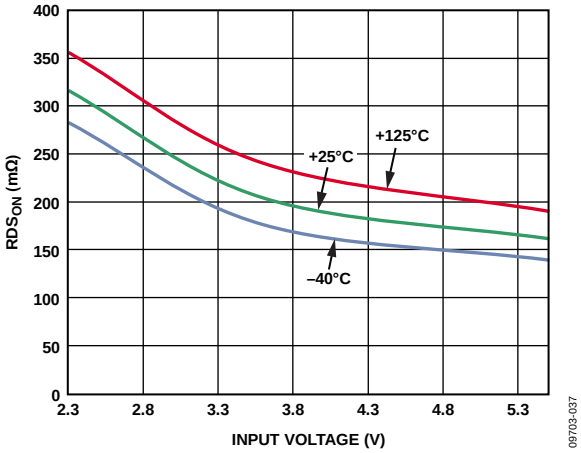


Figure 32. NMOS RDS_{ON} vs. Input Voltage Across Temperature

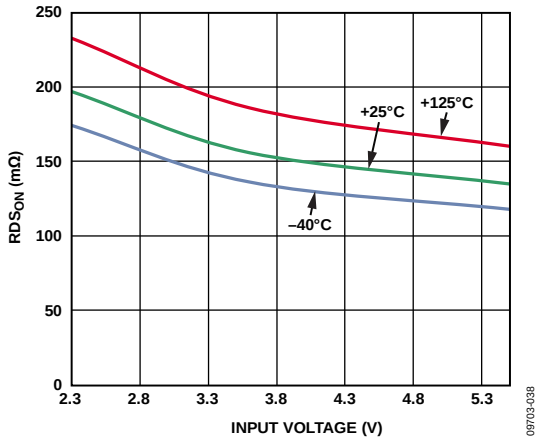


Figure 33. PMOS RDS_{ON} vs. Input Voltage Across Temperature

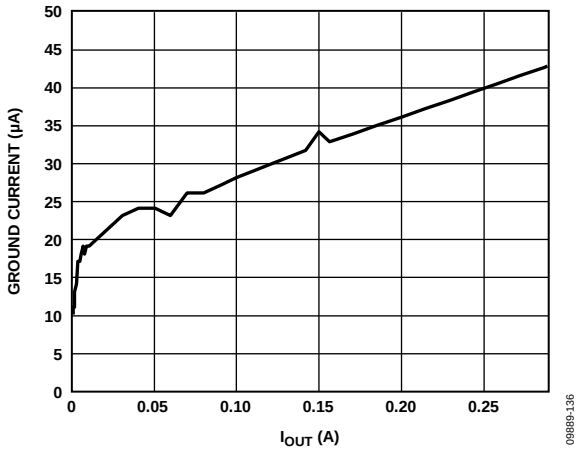


Figure 36. LDO Ground Current vs. Output Load, V_{IN3} = 3.3 V, V_{OUT3} = 2.8 V

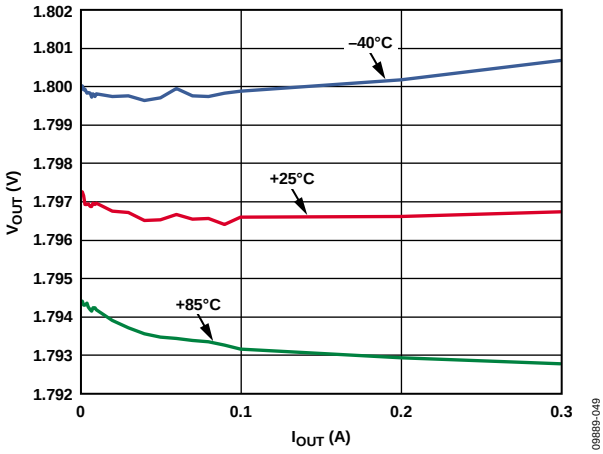


Figure 34. LDO Load Regulation Across Temperature, V_{IN3} = 3.6 V, V_{OUT3} = 1.8 V

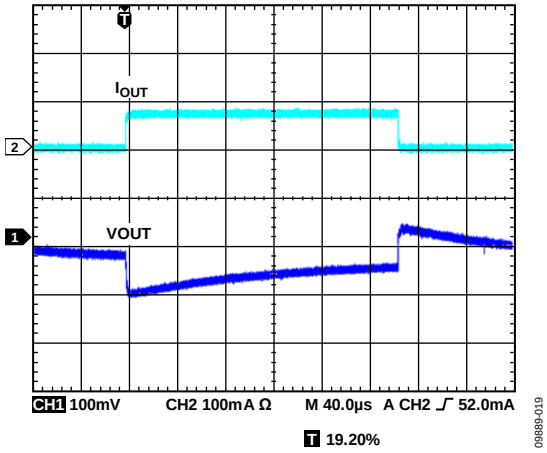


Figure 37. LDO Response to Load Transient, I_{OUT3} = 1 mA to 80 mA, V_{OUT3} = 2.8 V

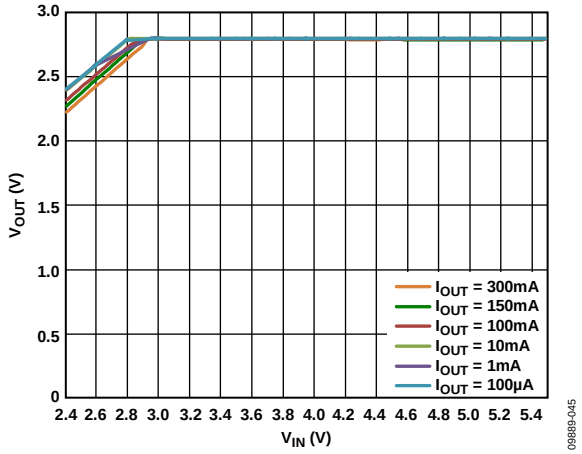


Figure 35. LDO Line Regulation Across Output Load, V_{OUT3} = 2.8 V

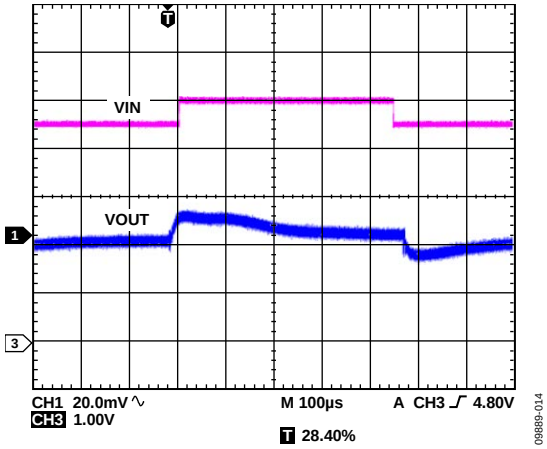


Figure 38. LDO Response to Line Transient, V_{IN} = 4.5 V to 5 V, V_{OUT3} = 2.8 V

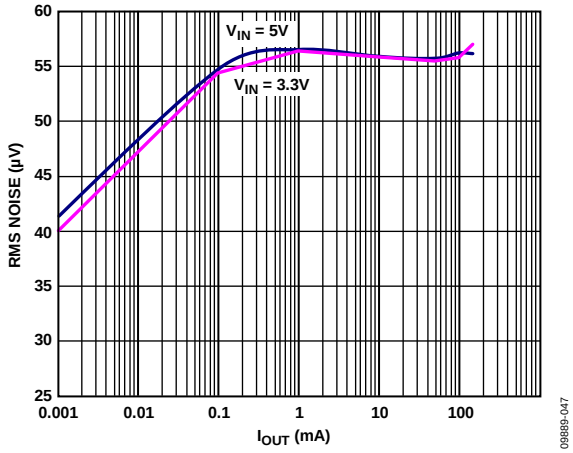


Figure 39. LDO Output Noise vs. Load Current, Across Input Voltage, V_{OUT3} = 2.8 V

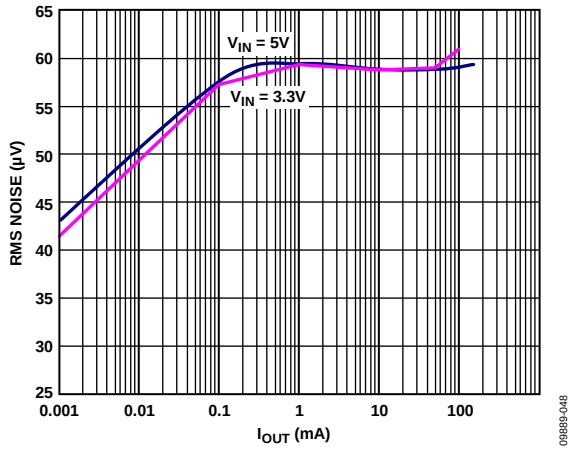


Figure 40. LDO Output Noise vs. Load Current, Across Input Voltage, V_{OUT3} = 3.0 V

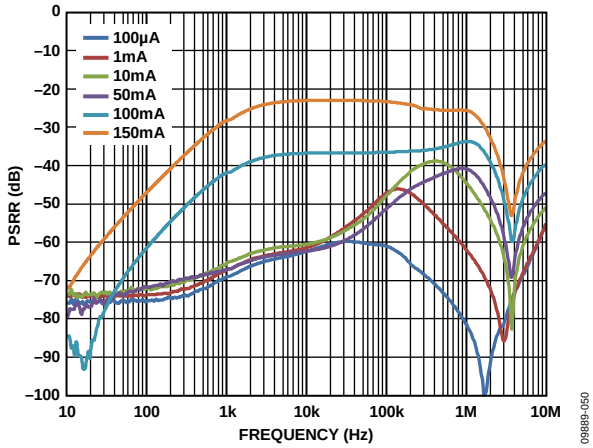


Figure 41. LDO PSRR Across Output Load, V_{IN3} = 3.3 V, V_{OUT3} = 2.8 V

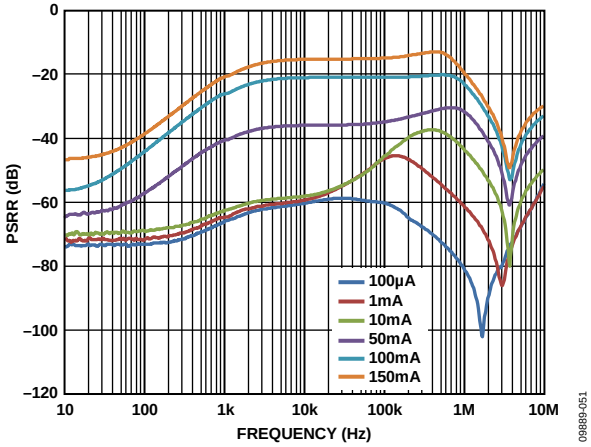


Figure 42. LDO PSRR Across Output Load, V_{IN3} = 3.3 V, V_{OUT3} = 3.0 V

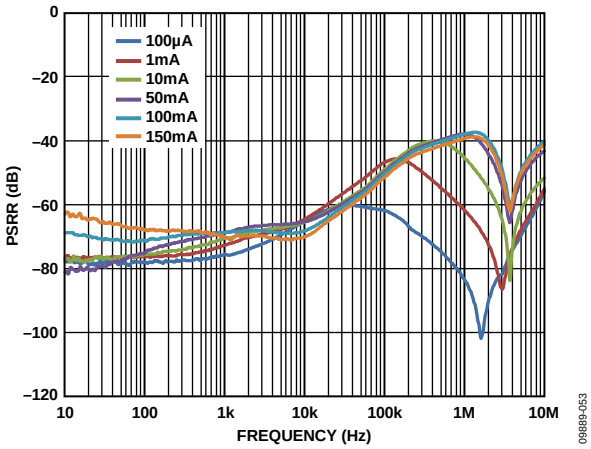


Figure 43. LDO PSRR Across Output Load, V_{IN3} = 5.0 V, V_{OUT3} = 2.8 V

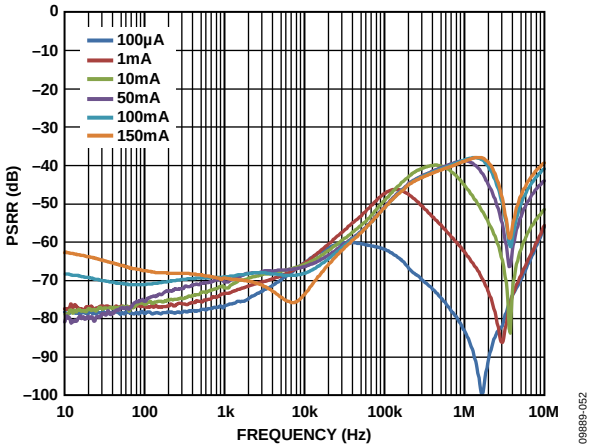


Figure 44. LDO PSRR Across Output Load, V_{IN3} = 5.0 V, V_{OUT3} = 3.0 V

THEORY OF OPERATION

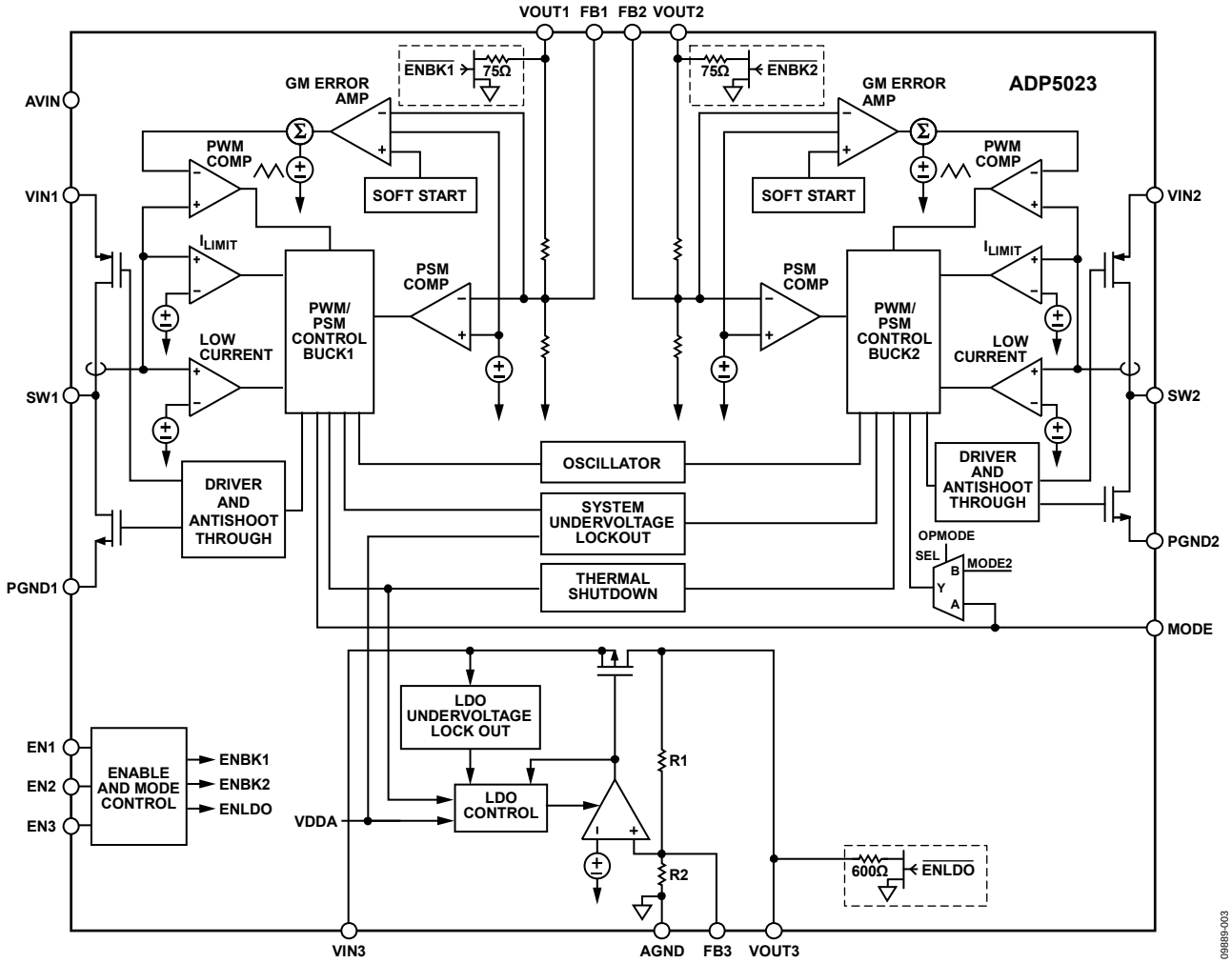


Figure 45. Functional Block Diagram

POWER MANAGEMENT UNIT

The ADP5023 is a micropower management unit (micro PMU) combining two step-down (buck) dc-to-dc converters and one low dropout linear regulator (LDO). The high switching frequency and tiny 24-lead LFCSP package allows a small power management solution.

To combine these high performance regulators into the micro PMU, there is a system controller allowing them to operate together.

The buck regulators can operate in forced PWM mode if the MODE pin is at a logic high level. In forced PWM mode, the buck switching frequency is always constant and does not change with the load current. If the MODE pin is at a logic low level, the switching regulators operate in auto PWM/PSM mode. In this mode, the regulators operate at fixed PWM frequency when the load current is above the PSM current threshold. When the load current falls below the PSM current threshold, the regulator in question enters PSM, where the switching occurs in bursts. The burst repetition rate is a function of the current load and the output capacitor value. This operating mode reduces the switching and quiescent current losses. The auto PWM/PSM mode transition is controlled independently for each buck regulator. The two bucks operate synchronized to each other.

The ADP5023 has individual enable pins (EN1 to EN3) controlling the activation of each regulator. The regulators are activated by a logic level high applied to the respective EN pin. EN1 controls BUCK1, EN2 controls BUCK2, and EN3 controls LDO.

Regulator output voltages are set through external resistor dividers or can be optionally factory programmed to default values (see the Ordering Guide section).

When a regulator is turned on, the output voltage ramp rate is controlled though a soft start circuit to avoid a large inrush current due to the charging of the output capacitors.

Thermal Protection

In the event that the junction temperature rises above 150°C, the thermal shutdown circuit turns off all the regulators. Extreme junction temperatures can be the result of high current

operation, poor circuit board design, or high ambient temperature. A 20°C hysteresis is included so that when thermal shutdown occurs, the regulators do not return to operation until the on-chip temperature drops below 130°C. When coming out of thermal shutdown, all regulators restart with soft-start control.

Undervoltage Lockout

To protect against battery discharge, undervoltage lockout (UVLO) circuitry is integrated into the system. If the input voltage on AVIN drops below a typical 2.15 V UVLO threshold, all channels shut down. In the buck channels, both the power switch and the synchronous rectifier turn off. When the voltage on AVIN rises above the UVLO threshold, the part is enabled once more.

Alternatively, the user can select device models with a UVLO set at a higher level, suitable for 5 V supply applications. For these models, the device reaches the turn-off threshold when the input supply drops to 3.65 V typical.

In case of a thermal or UVLO event, the active pull-downs (if factory enabled) are enabled to discharge the output capacitors quickly. The pull-down resistors remain engaged until the thermal fault event is no longer present, or the input supply voltage falls below the V_{POR} voltage level. The typical value of V_{POR} is approximately 1 V.

Enable/Shutdown

The ADP5023 has an individual control pin for each regulator. A logic level high applied to the ENx pin activates a regulator, whereas a logic level low turns off a regulator.

Figure 46 shows the regulator activation timings for the ADP5023 when all enable pins are connected to AVIN. Also shown is the active pull-down activation.

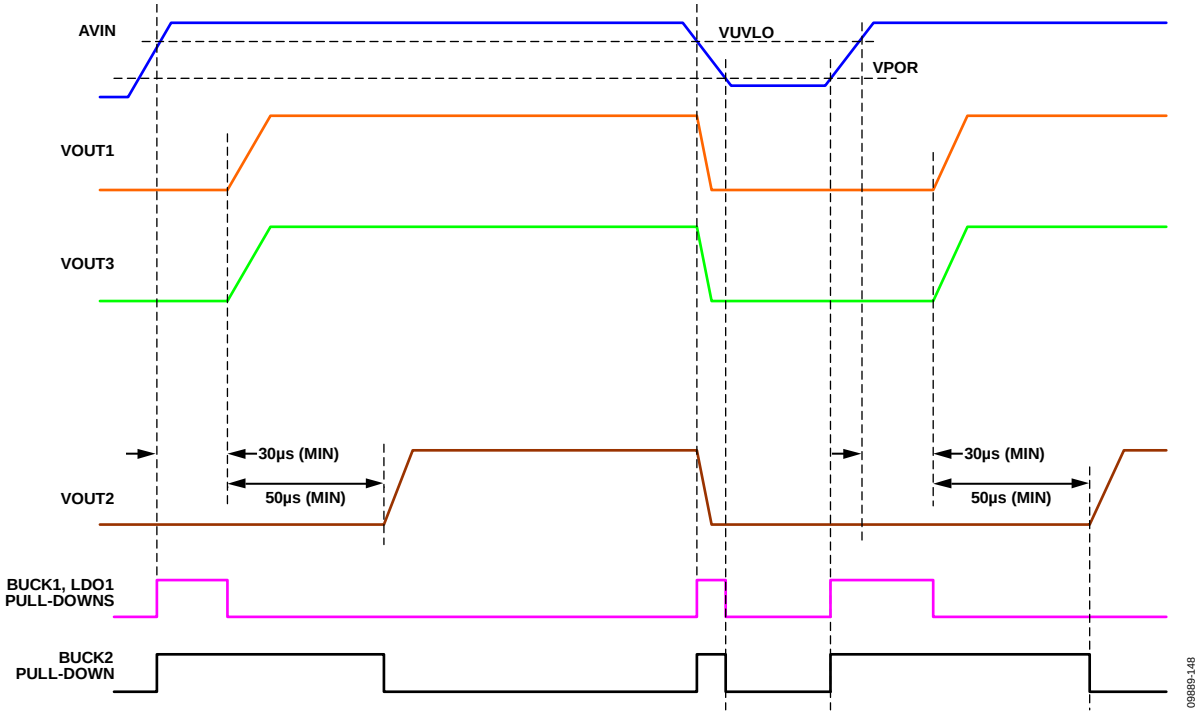
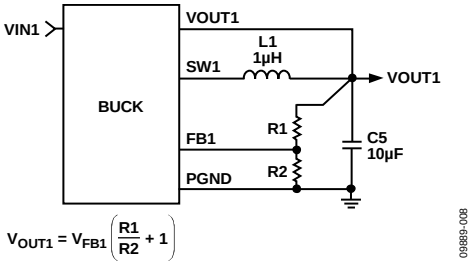


Figure 46. Regulator Sequencing on ADP5023 (EN1 = EN2 = EN3 = V_{AVIN})

BUCK1 AND BUCK2

The buck uses a fixed frequency and high speed current mode architecture. The buck operates with an input voltage of 2.3 V to 5.5 V.

The buck output voltage is set through external resistor dividers, shown in Figure 47 for BUCK1. The output voltage can optionally be factory programmed to default values as indicated in the Ordering Guide section. In this event, R1 and R2 are not needed, and FB1 can be left unconnected. In all cases, VOUT1 must be connected to the output capacitor. FB1 is 0.5 V.



$$V_{OUT1} = V_{FB1}\left(\frac{R1}{R2} + 1\right)$$

Figure 47. BUCK1 External Output Voltage Setting

Control Scheme

The bucks operate with a fixed frequency, current mode PWM control architecture at medium to high loads for high efficiency, but shift to a power save mode (PSM) control scheme at light loads to lower the regulation power losses. When operating in fixed frequency PWM mode, the duty cycle of the integrated switches is adjusted and regulates the output voltage. When operating in PSM at light loads, the output voltage is controlled in a hysteretic manner, with higher output voltage ripple. During part of this time, the converter is able to stop switching and enters an idle mode, which improves conversion efficiency.

PWM Mode

In PWM mode, the bucks operate at a fixed frequency of 3 MHz set by an internal oscillator. At the start of each oscillator cycle, the pFET switch is turned on, sending a positive voltage across the inductor. Current in the inductor increases until the current sense signal crosses the peak inductor current threshold that turns off the pFET switch and turns on the nFET synchronous rectifier. This sends a negative voltage across the inductor, causing the inductor current to decrease. The synchronous rectifier stays on for the rest of the cycle. The buck regulates the output voltage by adjusting the peak inductor current threshold.

Power Save Mode (PSM)

The bucks smoothly transition to PSM operation when the load current decreases below the PSM current threshold. When either of the bucks enters PSM, an offset is induced in the PWM regulation level, which makes the output voltage rise. When the output voltage reaches a level approximately 1.5% above the PWM regulation level, PWM operation is turned off. At this point, both power switches are off, and the buck enters an idle mode. The output capacitor discharges until the output voltage falls to the PWM regulation voltage, at which point the device drives the inductor to make the output voltage rise again to the upper threshold. This process is repeated while the load current is below the PSM current threshold.

The ADP5023 has a dedicated MODE pin controlling the PSM and PWM operation. A high logic level applied to the MODE pin forces both bucks to operate in PWM mode. A logic level low sets the bucks to operate in auto PSM/PWM.

PSM Current Threshold

The PSM current threshold is set to 100 mA. The bucks employ a scheme that enables this current to remain accurately controlled, independent of input and output voltage levels. This scheme also ensures that there is very little hysteresis between the PSM current threshold for entry to and exit from the PSM. The PSM current threshold is optimized for excellent efficiency over all load currents.

Oscillator/Phasing of Inductor Switching

The ADP5023 ensures that both bucks operate at the same switching frequency when both bucks are in PWM mode.

Additionally, the ADP5023 ensures that when both bucks are in PWM mode, they operate out of phase, whereby the BUCK2 pFET starts conducting exactly half a clock period after the BUCK1 pFET starts conducting.

Short-Circuit Protection

The bucks include frequency foldback to prevent output current runaway on a hard short. When the voltage at the feedback pin falls below half the target output voltage, indicating the possibility of a hard short at the output, the switching frequency is reduced to half the internal oscillator frequency. The reduction in the switching frequency allows more time for the inductor to discharge, preventing a runaway of output current.

Soft Start

The bucks have an internal soft start function that ramps the output voltage in a controlled manner upon startup, thereby limiting the inrush current. This prevents possible input voltage drops when a battery or a high impedance power source is connected to the input of the converter.

Current Limit

Each buck has protection circuitry to limit the amount of positive current flowing through the pFET switch and the amount of negative current flowing through the synchronous rectifier. The positive current limit on the power switch limits the amount of current that can flow from the input to the output. The negative current limit prevents the inductor current from reversing direction and flowing out of the load.

100% Duty Operation

With a drop in input voltage, or with an increase in load current, the buck may reach a limit where, even with the pFET switch on 100% of the time, the output voltage drops below the desired output voltage. At this limit, the buck transitions to a mode where the pFET switch stays on 100% of the time. When

the input conditions change again and the required duty cycle falls, the buck immediately restarts PWM regulation without allowing overshoot on the output voltage.

Active Pull-Downs

All regulators have optional, factory-programmable, active pull-down resistors discharging the respective output capacitors when the regulators are disabled. The pull-down resistors are connected between VOUTx and AGND. Active pull-downs are disabled when the regulators are turned on. The typical value of the pull-down resistor is 600 Ω for the LDO and 75 Ω for the bucks. Figure 46 shows the activation timings for the active pull-downs during regulator activation and deactivation.

LDO

The ADP5023 contains one LDO with low quiescent current and low dropout voltage, and provides up to 300 mA of output current. Drawing a low 10 µA quiescent current (typical) at no load makes the LDO ideal for battery-operated portable equipment.

The LDO operates with an input voltage of 1.7 V to 5.5 V. The wide operating range makes these LDO suitable for cascading configurations where the LDO supply voltage is provided from one of the buck regulators.

The LDO output voltage is set through external resistor dividers as shown in Figure 48 for LDO. The output voltage can optionally be factory programmed to default values as indicated in the Ordering Guide section. In this event, Ra and Rb are not needed, and FB3 must be connected to the top of the capacitor on VOUT3. FB3 is 0.5 V.

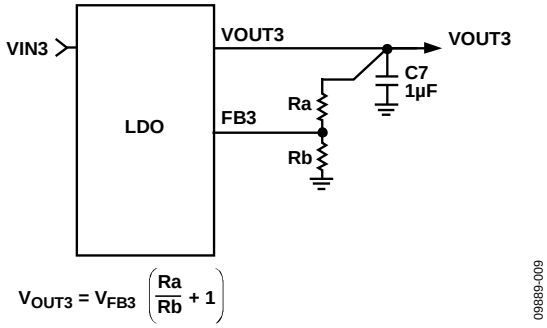


Figure 48. LDO External Output Voltage Setting

The LDO also provides high power supply rejection ratio (PSRR), low output noise, and excellent line and load transient response with only a small 1 µF ceramic input and output capacitor.

APPLICATIONS INFORMATION

BUCK EXTERNAL COMPONENT SELECTION

Trade-offs between performance parameters such as efficiency and transient response can be made by varying the choice of external components in the applications circuit, as shown in Figure 1.

Feedback Resistors

For the adjustable model, referring to Figure 47, the total combined resistance for R1 and R2 is not to exceed 400 kΩ.

Inductor

The high switching frequency of the ADP5023 bucks allows the selection of small chip inductors. For best performance, use inductor values between 0.7 µH and 3 µH. Suggested inductors are shown in Table 8.

The peak-to-peak inductor current ripple is calculated using the following equation:

$$I_{RIPPLE} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

where:
f_{SW} is the switching frequency.
L is the inductor value.

The minimum dc current rating of the inductor must be greater than the inductor peak current. The inductor peak current is calculated using the following equation:

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{I_{RIPPLE}}{2}$$

Inductor conduction losses are caused by the flow of current through the inductor, which has an associated internal dc resistance (DCR). Larger sized inductors have smaller DCR, which may decrease inductor conduction losses. Inductor core losses are related to the magnetic permeability of the core material. Because the bucks are high switching frequency dc-to-dc converters, shielded ferrite core material is recommended for its low core losses and low EMI.

Output Capacitor

Higher output capacitor values reduce the output voltage ripple and improve load transient response. When choosing this value, it is also important to account for the loss of capacitance due to output voltage dc bias.

Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended for best performance. Y5V and Z5U dielectrics are not recommended for use with any dc-to-dc converter because of their poor temperature and dc bias characteristics.

The worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage is calculated using the following equation:

$$C_{EFF} = C_{OUT} \times (1 - TEMPCO) \times (1 - TOL)$$

where:
C_{EFF} is the effective capacitance at the operating voltage.
$TEMPCO$ is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10% and C_{OUT} is 9.2 µF at 1.8 V, as shown in Figure 49.

Substituting these values in the equation yields

$$C_{EFF} = 9.2\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 7.0\ \mu F$$

To guarantee the performance of the bucks, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

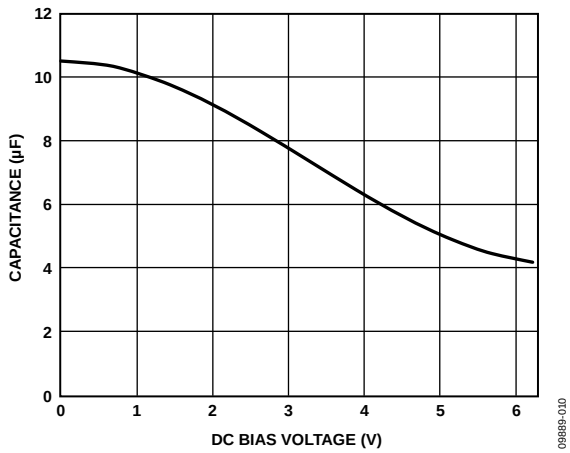


Figure 49. Capacitance vs. Voltage Characteristic

Table 8. Suggested 1.0 µH Inductors

Vendor	Model	Dimensions (mm)	I_{SAT} (mA)	DCR (mΩ)
Murata	LQM2MPN1R0NG0B	2.0 × 1.6 × 0.9	1400	85
Murata	LQM18FN1R0M00B	3.2 × 2.5 × 1.5	2300	54
Taiyo Yuden	CBC3225T1R0MR	3.2 × 2.5 × 2.5	2000	71
Coilcraft	XFL4020-102ME	4.0 × 4.0 × 2.1	5400	11
Coilcraft	XPL2010-102ML	1.9 × 2.0 × 1.0	3750	89
Toko	MDT2520-CN	2.5 × 2.0 × 1.2	1350	85

The peak-to-peak output voltage ripple for the selected output capacitor and inductor values is calculated using the following equation:

$$V_{RIPPLE} = \frac{I_{RIPPLE}}{8 \times f_{SW} \times C_{OUT}} \approx \frac{V_{IN}}{(2\pi \times f_{SW})^2 \times L \times C_{OUT}}$$

Capacitors with lower equivalent series resistance (ESR) are preferable to guarantee low output voltage ripple, as shown in the following equation:

$$ESR_{COUT} \leq \frac{V_{RIPPLE}}{I_{RIPPLE}}$$

The effective capacitance needed for stability, which includes temperature and dc bias effects, is a minimum of 7 µF and a maximum of 40 µF.

The buck regulators require 10 µF output capacitors to guarantee stability and response to rapid load variations and to transition into and out of the PWM/PSM modes. A list of suggested capacitors is shown in Table 9. In certain applications where one or both buck regulator powers a processor, the operating state is known because it is controlled by software. In this condition, the processor can drive the MODE pin according to the operating state; consequently, it is possible to reduce the output capacitor from 10 µF to 4.7 µF because the regulator does not expect a large load variation when working in PSM mode (see Figure 50).

Input Capacitor

Higher value input capacitors help to reduce the input voltage ripple and improve transient response. Maximum input capacitor current is calculated using the following equation:

$$I_{CIN} \geq I_{LOAD(MAX)} \sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}}$$

To minimize supply noise, place the input capacitor as close as possible to the VINx pin of the buck. As with the output capacitor, a low ESR capacitor is recommended.

The effective capacitance needed for stability, which includes temperature and dc bias effects, is a minimum of 3 µF and a maximum of 10 µF. A list of suggested capacitors is shown in Table 10.

Table 9. Suggested 10 µF Capacitors

Vendor	Type	Model	Case Size	Voltage Rating (V)
Murata	X5R	GRM188R60J106	0603	6.3
TDK	X5R	C1608JB0J106K	0603	6.3
Panasonic	X5R	ECJ1VB0J106M	0603	6.3

Table 10. Suggested 4.7 µF Capacitors

Vendor	Type	Model	Case Size	Voltage Rating (V)
Murata	X5R	GRM188R60J475ME19D	0402	6.3
Taiyo Yuden	X5R	JMK107BJ475	0402	6.3
Panasonic	X5R	ECJ-0EB0J475M	0402	6.3

Table 11. Suggested 1.0 µF Capacitors

Vendor	Type	Model	Case Size	Voltage Rating (V)
Murata	X5R	GRM155B30J105K	0402	6.3
TDK	X5R	C1005JB0J105KT	0402	6.3
Panasonic	X5R	ECJ0EB0J105K	0402	6.3
Taiyo Yuden	X5R	LMK105BJ105MV-F	0402	10.0

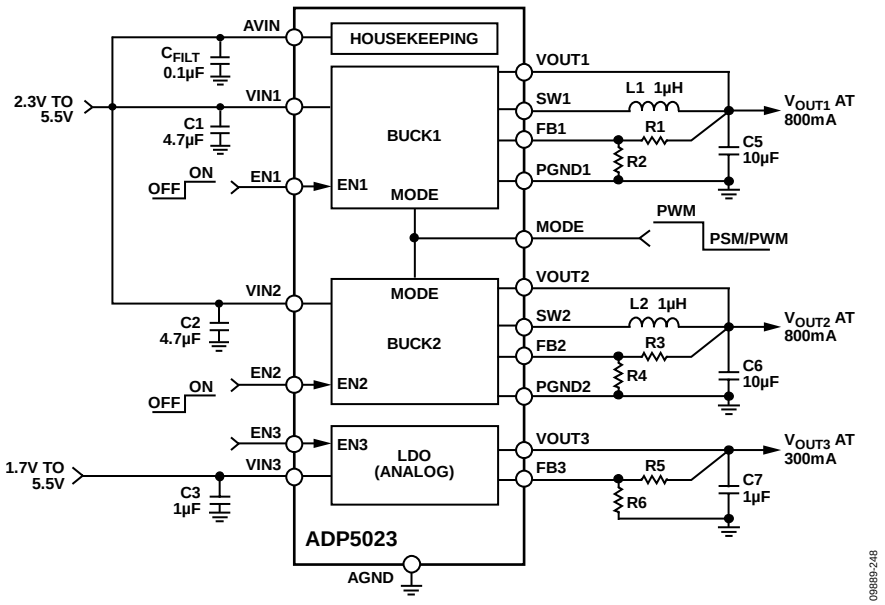


Figure 50. Processor System Power Management with PSM/PWM Control

LDO EXTERNAL COMPONENT SELECTION

Feedback Resistors

For the adjustable model, the maximum value of Rb is not to exceed 200 kΩ (see Figure 48).

Output Capacitor

The ADP5023 LDO is designed for operation with small, space-saving ceramic capacitors, but functions with most commonly used capacitors as long as care is taken with the ESR value. The ESR of the output capacitor affects stability of the LDO control loop. A minimum of 0.70 µF capacitance with an ESR of 1 Ω or less is recommended to ensure stability of the ADP5023. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP5023 to large changes in load current.

Input Bypass Capacitor

Connecting a 1 µF capacitor from VIN3 to ground reduces the circuit sensitivity to printed circuit board (PCB) layout, especially when long input traces or high source impedance are encountered. If greater than 1 µF of output capacitance is required, increase the input capacitor to match it.

Input and Output Capacitor Properties

Use any good quality ceramic capacitors with the ADP5023 as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended for best performance. Y5V and Z5U dielectrics are not recommended for use with any LDO because of their poor temperature and dc bias characteristics.

Figure 51 depicts the capacitance vs. voltage bias characteristic of a 0402 1 µF, 10 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is about ±15% over the −40°C to +85°C temperature range and is not a function of package or voltage rating.

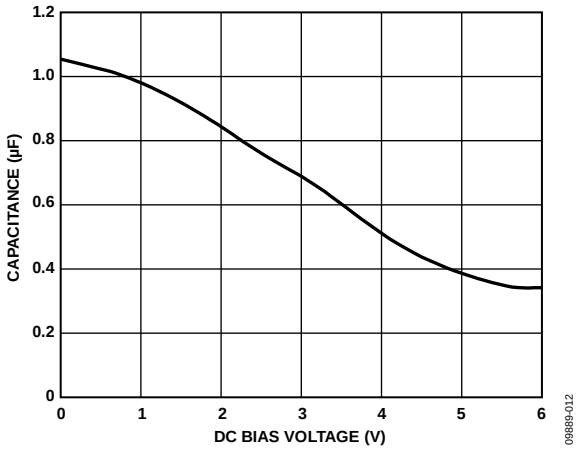


Figure 51. Capacitance vs. Voltage Characteristic

Use the following equation to determine the worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL)$$

where:
C_{BIAS} is the effective capacitance at the operating voltage.
TEMPCO is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10% and C_{BIAS} is 0.85 µF at 1.8 V as shown in Figure 51.

Substituting these values into the following equation:

$$C_{EFF} = 0.85\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 0.65\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP5023, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors are evaluated for each application.

POWER DISSIPATION AND THERMAL CONSIDERATIONS

The ADP5023 is a highly efficient µPMU, and, in most cases, the power dissipated in the device is not a concern. However, if the device operates at high ambient temperatures and maximum loading condition, the junction temperature can reach the maximum allowable operating limit (125°C).

When the temperature exceeds 150°C, the ADP5023 turns off all the regulators, allowing the device to cool down. When the die temperature falls below 130°C, the ADP5023 resumes normal operation.

This section provides guidelines to calculate the power dissipated in the device and ensure that the ADP5023 operates below the maximum allowable junction temperature.

The efficiency for each regulator on the ADP5023 is given by

$$\eta = \frac{P_{OUT}}{P_{IN}} \times 100\% \quad (1)$$

where:
η is the efficiency.
P_{IN} is the input power.
P_{OUT} is the output power.

Power loss is given by

$$P_{LOSS} = P_{IN} - P_{OUT} \quad (2a)$$

or

$$P_{LOSS} = P_{OUT}(1 - \eta)/\eta \quad (2b)$$

Power dissipation can be calculated in several ways. The most intuitive and practical is to measure the power dissipated at the input and all the outputs. Perform the measurements at the worst-case conditions (voltages, currents, and temperature). The difference between input and output power is dissipated in the device and the inductor. Use Equation 4 to derive the power lost in the inductor, and from this use Equation 3 to calculate the power dissipation in the ADP5023 buck converter.

A second method to estimate the power dissipation uses the efficiency curves provided for the buck regulator, and the power lost on the LDO can be calculated using Equation 12. When the buck efficiency is known, use Equation 2b to derive the total power lost in the buck regulator and inductor, use Equation 4 to derive the power lost in the inductor, and then calculate the power dissipation in the buck converter using Equation 3. Add the power dissipated in the buck and in the LDO to find the total dissipated power.

Note that the buck efficiency curves are typical values and may not be provided for all possible combinations of V_{IN}, V_{OUT}, and I_{OUT}. To account for these variations, it is necessary to include a safety margin when calculating the power dissipated in the buck.

A third way to estimate the power dissipation is analytical and involves modeling the losses in the buck circuit provided by Equation 8 to Equation 11 and the losses in the LDO provided by Equation 12.

BUCK REGULATOR POWER DISSIPATION

The power loss of the buck regulator is approximated by

$$P_{LOSS} = P_{DBUCK} + P_L \quad (3)$$

where:
P_{DBUCK} is the power dissipation on one of the ADP5023 buck regulators.
P_L is the inductor power losses.

The inductor losses are external to the device and do not have any effect on the die temperature.

The inductor losses are estimated (without core losses) by

$$P_L \approx I_{OUT1(RMS)}^2 \times DCR_L \quad (4)$$

where:
DCR_L is the inductor series resistance.
$I_{OUT1(RMS)}$ is the rms load current of the buck regulator.

$$I_{OUT1(RMS)} = I_{OUT1} \times \sqrt{1 + \frac{r}{12}} \quad (5)$$

where r is the normalized inductor ripple current

$$r = V_{OUT1} \times (1 - D)/(I_{OUT1} \times L \times f_{SW}) \quad (6)$$

where:
L is the inductance.
f_{SW} is the switching frequency.
D is the duty cycle.

$$D = V_{OUT1}/V_{IN1} \quad (7)$$

ADP5023 buck regulator power dissipation, P_{DBUCK}, includes the power switch conductive losses, the switch losses, and the transition losses of each channel. There are other sources of loss, but these are generally less significant at high output load currents, where the thermal limit of the application is. Equation 8 captures the calculation that must be made to estimate the power dissipation in the buck regulator.

$$P_{DBUCK} = P_{COND} + P_{SW} + P_{TRAN} \quad (8)$$

The power switch conductive losses are due to the output current, I_{OUT1}, flowing through the P-MOSFET and the N-MOSFET power switches that have internal resistance, RDS_{ON-P} and RDS_{ON-N}. The amount of conductive power loss is found by

$$P_{COND} = [RDS_{ON-P} \times D + RDS_{ON-N} \times (1 - D)] \times I_{OUT1(RMS)}^2 \quad (9)$$

where RDS_{ON-P} is approximately 0.2 Ω, and RDS_{ON-N} is approximately 0.16 Ω at 25°C junction temperature and VIN1 = VIN2 = 3.6 V. At VIN1 = VIN2 = 2.3 V, these values change to 0.31 Ω and 0.21 Ω, respectively, and at VIN1 = VIN2 = 5.5 V, the values are 0.16 Ω and 0.14 Ω, respectively.

Switching losses are associated with the current drawn by the driver to turn on and turn off the power devices at the switching frequency. The amount of switching power loss is given by

$$P_{SW} = (C_{GATE\text{-}P} + C_{GATE\text{-}N}) \times V_{IN1}^2 \times f_{SW} \quad (10)$$

where:
$C_{GATE\text{-}P}$ is the P-MOSFET gate capacitance.
$C_{GATE\text{-}N}$ is the N-MOSFET gate capacitance.

For the ADP5023, the total of ($C_{GATE\text{-}P} + C_{GATE\text{-}N}$) is approximately 150 pF.

The transition losses occur because the P-channel power MOSFET cannot be turned on or off instantaneously, and the SW node takes some time to slew from near ground to near V_{OUT1} (and from V_{OUT1} to ground). The amount of transition loss is calculated by

$$P_{TRAN} = V_{IN1} \times I_{OUT1} \times (t_{RISE} + t_{FALL}) \times f_{SW} \quad (11)$$

where t_{RISE} and t_{FALL} are the rise time and the fall time of the switching node, SW. For the ADP5023, the rise and fall times of SW are in the order of 5 ns.

If the preceding equations and parameters are used for estimating the converter efficiency, it must be noted that the equations do not describe all of the converter losses, and the parameter values given are typical numbers. The converter performance also depends on the choice of passive components and board layout; therefore, a sufficient safety margin should be included in the estimate.

LDO Regulator Power Dissipation

The power loss of a LDO regulator is given by

$$P_{DLDO} = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND}) \quad (12)$$

where:
I_{LOAD} is the load current of the LDO regulator.
V_{IN} and V_{OUT} are input and output voltages of the LDO, respectively.
I_{GND} is the ground current of the LDO regulator.

Power dissipation due to the ground current is small and it can be ignored.

The total power dissipation in the ADP5023 simplifies to

$$P_D = P_{DBUCK1} + P_{DBUCK2} + P_{DLDO} \quad (13)$$

JUNCTION TEMPERATURE

In cases where the board temperature T_A is known, the thermal resistance parameter, θ_{JA}, can be used to estimate the junction temperature rise. T_J is calculated from T_A and P_D using the formula

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (14)$$

The typical θ_{JA} value for the 24-lead, 4 mm × 4 mm LFCSP is 35°C/W (see Table 6). A very important factor to consider is that θ_{JA} is based on 4-layer, 4 in × 3 in, 2.5 oz copper, as per JEDEC standard, and real applications may use different sizes and layers. It is important to maximize the copper used to remove the heat from the device. Copper exposed to air dissipates heat better than copper used in the inner layers. The exposed pad should be connected to the ground plane with several vias.

If the case temperature can be measured, the junction temperature is calculated by

$$T_J = T_C + (P_D \times \theta_{JC}) \quad (15)$$

where T_C is the case temperature and θ_{JC} is the junction-to-case thermal resistance provided in Table 6.

When designing an application for a particular ambient temperature range, calculate the expected ADP5023 power dissipation (P_D) due to the losses of all channels by using Equation 8 to Equation 13. From this power calculation, the junction temperature, T_J, can be estimated using Equation 14.

The reliable operation of the converter and the two LDO regulators can be achieved only if the estimated die junction temperature of the ADP5023 (Equation 14) is less than 125°C. Reliability and mean time between failures (MTBF) is highly affected by increasing the junction temperature. Additional information about product reliability can be found from the *ADI Reliability Handbook*, which can be found at www.analog.com/reliability_handbook.

PCB LAYOUT GUIDELINES

Poor layout can affect ADP5023 performance, causing electromagnetic interference (EMI) and electromagnetic compatibility (EMC) problems, ground bounce, and voltage losses. Poor layout can also affect regulation and stability. A good layout is implemented using the following guidelines. Also, refer to User Guide UG-271.

- Place the inductor, input capacitor, and output capacitor close to the IC using short tracks. These components carry high switching frequencies, and large tracks act as antennas.
- Route the output voltage path away from the inductor and SW node to minimize noise and magnetic interference.
- Maximize the size of ground metal on the component side to help with thermal dissipation.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.
- Connect VIN1, VIN2, and AVIN together close to the IC using short tracks.

TYPICAL APPLICATION SCHEMATICS

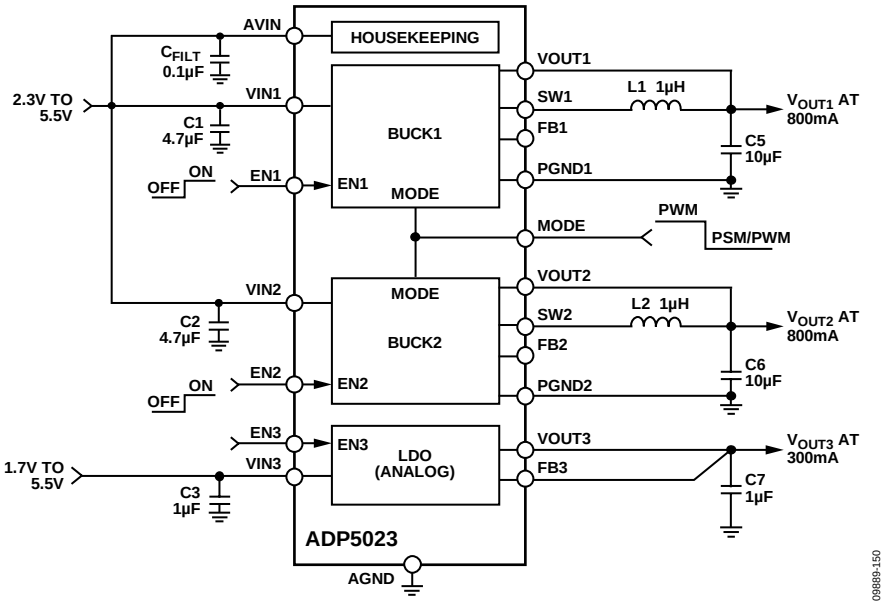


Figure 52. ADP5023 Fixed Output Voltages with Enable Pins

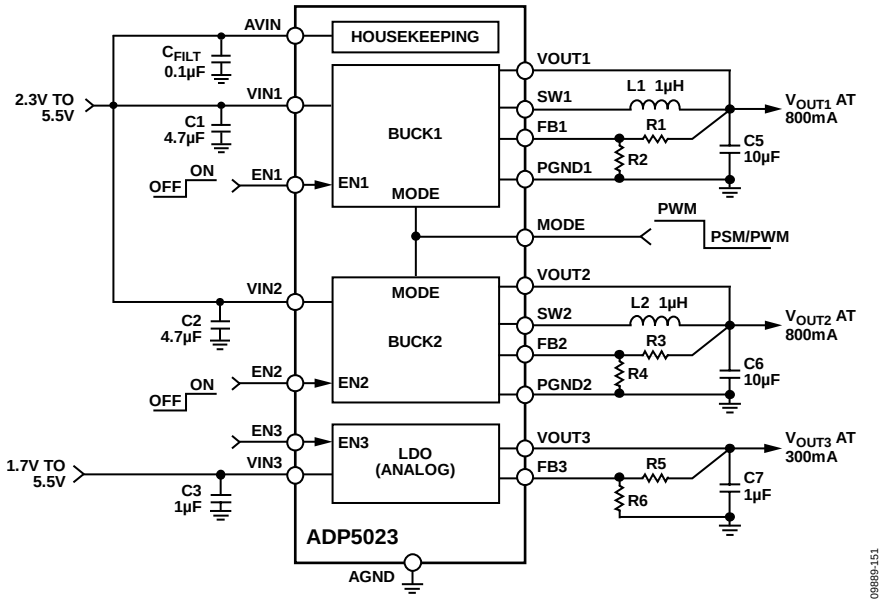


Figure 53. ADP5023 Adjustable Output Voltages with Enable Pins

BILL OF MATERIALS

Table 12.

Reference	Value	Part Number	Vendor	Package or Dimension (mm)
C_{AVIN}	0.1 µF, X5R, 6.3 V	JMK105BJ104MV-F	Taiyo-Yuden	0402
C3, C7	1 µF, X5R, 6.3 V	LMK105BJ105MV-F	Taiyo-Yuden	0402
C1, C2	4.7 µF, X5R, 6.3 V	ECJ-0EB0J475M	Panasonic-ECG	0402
C5, C6	10 µF, X5R, 6.3 V	JMK107BJ106MA-T	Taiyo-Yuden	0603
L1, L2	1 µH, 0.18 Ω, 850 mA	BRC1608T1R0M	Taiyo-Yuden	0603
	1 µH, 0.085 Ω, 1400 mA	LQM2MPN1R0NG0B	Murata	2.0 × 1.6 × 0.9
	1 µH, 0.059 Ω, 900 mA	EPL2014-102ML	Coilcraft	2.0 × 2.0 × 1.4
	1 µH, 0.086 Ω, 1350 mA	MDT2520-CN	Toko	2.5 × 2.0 × 1.2
IC1	Three-regulator micro PMU	ADP5023	Analog Devices	24-lead LFCSP

OUTLINE DIMENSIONS

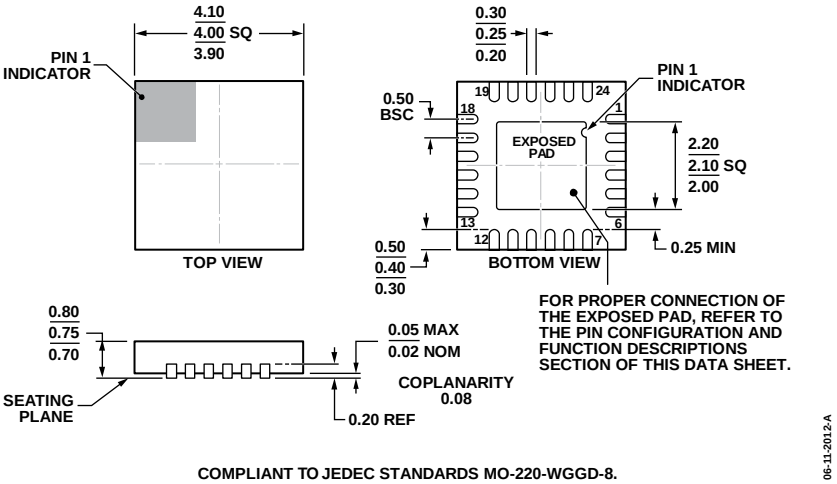


Figure 54. 24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-24-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Output Voltage[2]	UVLO[3]	Active Pull-Down[4]	Package Description	Package Option
ADP5023ACPZ-R7	−40°C to +125°C	Adjustable	Low	Enabled on buck channels	24-Lead Frame Chip Scale Package [LFCSP_WQ]	CP-24-10
ADP5023ACPZ-R2	−40°C to +125°C	Adjustable	Low	Enabled on buck channels	24-Lead Frame Chip Scale Package [LFCSP_WQ]	CP-24-10
ADP5023ACPZ-1-R7	−40°C to +125°C	VOUT1 = 1.2 V VOUT2 = 3.3 V VOUT3 = 2.8 V	Low	Enabled on buck channels	24-Lead Frame Chip Scale Package [LFCSP_WQ]	CP-24-10
ADP5023ACPZ-2-R7	−40°C to +125°C	Adjustable	High	Enabled on all channels	24-Lead Frame Chip Scale Package [LFCSP_WQ]	CP-24-10
ADP5023CP-EVALZ					Evaluation Board for ADP5023ACPZ-R7	

[1] Z = RoHS Compliant Part.
[2] For additional options, contact a local sales or distribution representative. Additional options available are:
BUCK1 and BUCK2: 3.3 V, 3.0 V, 2.8 V, 2.5 V, 2.3 V, 2.0 V, 1.8 V, 1.6 V, 1.5 V, 1.4 V, 1.3 V, 1.2 V, 1.1 V, 1.0 V, 0.9 V or adjustable.
LDO: 3.3 V, 3.0 V, 2.8 V, 2.5 V, 2.25 V, 2 V, 1.8 V, 1.7 V, 1.6 V, 1.5 V, 1.2 V, 1.1 V, 1.0 V, 0.9 V, 0.8 V or adjustable.
[3] UVLO: Low or High.
[4] BUCK1, BUCK2, LDO: Active pull-down resistor is programmable to be either enabled or disabled.

NOTES

©2011-2013 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D09889-0-1/13(C)