REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. - phn	08-06-18	Thomas M. Hess

REV																				
SHEET																				
REV																				
SHEET																				
REV STATUS				REV			A	A												
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	

PMIC N/A

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DRAWING APPROVAL DATE
08-01-09

REVISION LEVEL
A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, CMOS, ASIC, SINGLE SPACEWIRE LINK HIGH SPEED CONTROLLER, MONOLITHIC SILICON

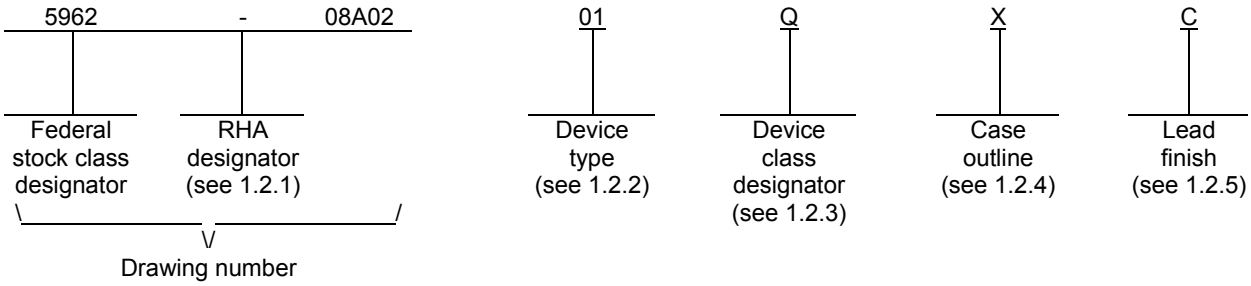
SIZE	CAGE CODE	
A	**67268**	**5962-08A02**

SHEET 1 OF 13

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01 1/	AT7912E	Single SpaceWire link High Speed Controller
02	AT7912F	Single SpaceWire link High Speed Controller

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	100	Multilayer Quad Flat Pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Device type 01 is no longer available.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range (V_{CC})	-0.5V to 7.0 V dc
Power dissipation (Pd)	0.7 W
Storage temperature range	-65°C to 150°C
Maximum junction temperature (T_J)	175°C
Thermal resistance junction to case (θ_{jc})	5 °C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V to 5.5 V dc or 3.0 V to 3.6 V dc
Ambient operating temperature (T_A)	-55°C to 125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil;quicksearch/ or www.dodssp.daps.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ All voltage referenced to ground unless otherwise specified

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block or logic diagram(s). The block or logic diagram(s) shall be as specified on figure 3.

3.2.4 Timing waveforms. The timing waveforms shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 123 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

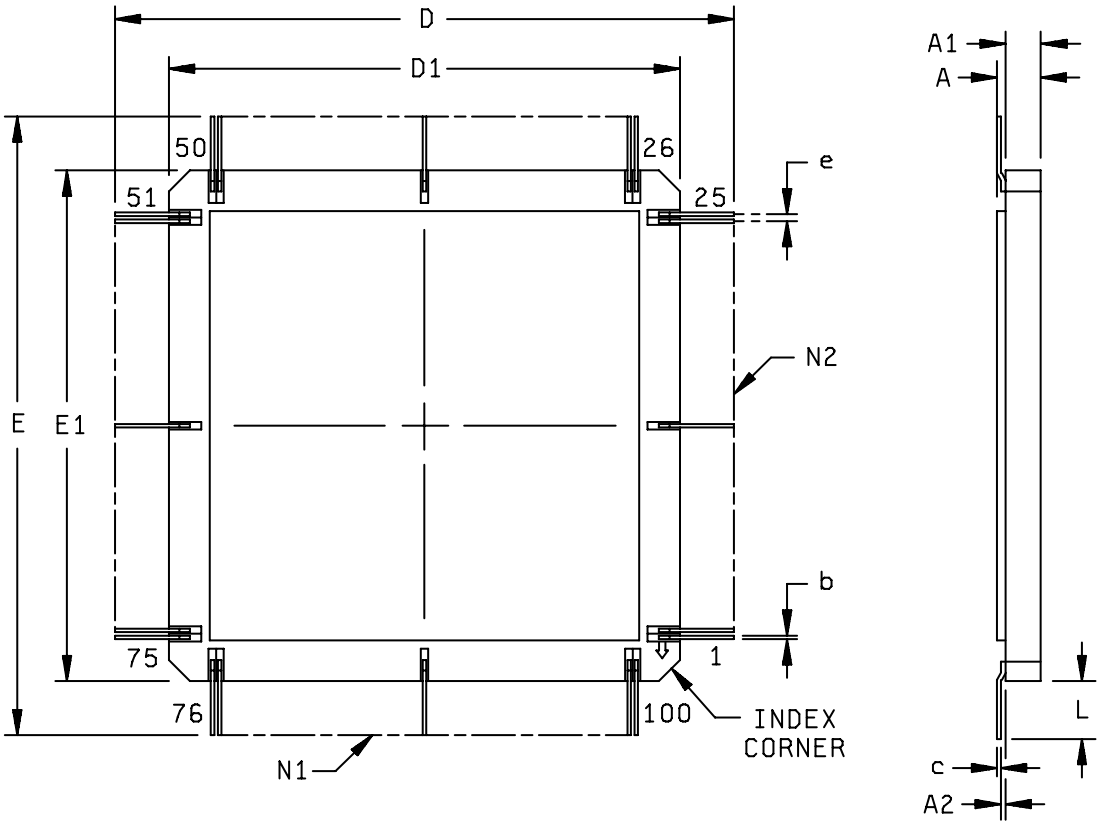
Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ **$4.5\ V \le V_{CC} \le 5.5\ V$** unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Low level input voltage	V_{IL}		1,2,3		0.8	V
High level input voltage	V_{IH}		1,2,3	2.2		V
Low level input current	I_{IL}	V_{IN} = GND, V_{CC} = 5.5 V	1,2,3	-5		µA
Low level input current Pull-down	I_{ILPD}	V_{IN} = GND, V_{CC} = 5.5 V	1,2,3	-5		µA
Low level input current Pull-up	I_{ILPU}	V_{IN} = GND, V_{CC} = 5.5V	1,2,3	-120		µA
High level input current	I_{IH}	V_{IN} = V_{CC} = 5.5 V	1,2,3		5	µA
High level input current Pull-up	I_{IHPU}	V_{IN} = V_{CC} = 5.5 V	1,2,3		5	µA
High level input current Pull-down	I_{IHPD}	V_{IN} = V_{CC} = 5.5 V	1,2,3		330	µA
Output leakage low current	I_{OZL}	Outputs disabled V_{OUT} = GND	1,2,3	-5		µA
Output leakage low current Pull-down output	I_{OZLPD}	Outputs disabled, V_{OUT} = GND	1,2,3	-5		µA
Output leakage low current Pull-up output	I_{OZLPU}	Outputs disabled V_{OUT} = GND	1,2,3	-120		µA
Output leakage high current	I_{OZH}	Outputs disabled, V_{OUT} = V_{CC}	1,2,3		5	µA
Output leakage high current Pull-up output	I_{OZHPU}	Outputs disabled, V_{OUT}=V_{CC}	1,2,3		5	µA
Output leakage high current Pull-down output	I_{OZHPD}	Outputs disabled, V_{OUT}=V_{CC}	1,2,3		330	µA
Low level output voltage	V_{OL}	V_{CC} = 4.5 V I_{OL} = 3, 6, 12 mA	1,2,3		0.4	V
High level output voltage	V_{OH}	V_{CC} = 4.5 V I_{OH} = -3, -6, -12 mA	1,2,3	3.9		V
Output short circuit current	I_{OS}	V_{OUT} = V_{CC} V_{OUT} = GND	1,2,3		90 1/ 180 2/ 270 3/	mA
Supply current when not clocked	I_{CCSB}		1,2,3		2	mA
Supply current in RESET	I_{CCRES}		1,2,3		22	mA
Supply current in IDLE	I_{CCIDLE}		1,2,3		75	mA
Operating supply current	I_{CCOP}		1,2,3		120	mA
Input capacitance 4/	C_{IN}	V_{CC} = 0 V	4		15	pF
Input/Output capacitance 4/	C_{IO}	V_{CC} = 0 V	4		15	pF
CLK low to TDO high	t_{p1}		9,10,11		20	ns
CLK high to TMR1_EXP low	t_{p2}		9,10,11		23	ns
CLK high to LDO low	t_{p3}		9,10,11		16	ns
CLK10 high to HINTR* low	t_{p4}		9,10,11		25	ns
CLK10 high to IOB18 low	t_{p5}		9,10,11		16	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ **$3.0\ V \le V_{CC} \le 3.6\ V$** unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Low level input voltage	V_{IL}		1, 2, 3		0.8	V
High level input voltage	V_{IH}		1, 2, 3	2.0		V
Low level input current	I_{IL}	V_{IN} = GND, V_{CC} = 3.3 V	1, 2, 3	-1		µA
Low level input current Pull-down	I_{ILPD}	V_{IN} = GND, V_{CC} = 3.3 V	1, 2, 3	-1		µA
Low level input current Pull-up	I_{ILPU}	V_{IN} = GND, V_{CC} = 3.3 V	1, 2, 3	-60		µA
High level input current	I_{IH}	$V_{IN} = V_{CC}$ = 3.3V	1, 2, 3		1	µA
High level input current Pull-up	I_{IHPU}	$V_{IN} = V_{CC}$ = 3.3V	1, 2, 3		1	µA
High level input current Pull-down	I_{IHPD}	$V_{IN} = V_{CC}$ = 3.3V	1, 2, 3		150	µA
Output leakage low current	I_{OZL}	Outputs disabled, V_{OUT} = GND	1, 2, 3	-1		µA
Output leakage low current Pull-down output	I_{OZLPD}	Outputs disabled, V_{OUT} = GND	1, 2, 3	-1		µA
Output leakage low current Pull-up output	I_{OZLPU}	Outputs disabled, V_{OUT} = GND	1, 2, 3	-60		µA
Output leakage high current	I_{OZH}	Outputs disabled, $V_{OUT} = V_{CC}$	1, 2, 3		1	µA
Output leakage high current Pull-up output	I_{OZHPU}	Outputs disabled, $V_{OUT} = V_{CC}$	1, 2, 3		1	µA
Output leakage high current Pull-down output	I_{OZHPD}	Outputs disabled, $V_{OUT} = V_{CC}$	1, 2, 3		150	µA
Low level output voltage	V_{OL}	V_{CC} = 3.0V I_{OL} = 1, 2, 4 mA	1, 2, 3		0.4	V
high level output voltage	V_{OH}	V_{CC} = 3.0V I_{OH} = 1.5, 3, 6 mA	1, 2, 3	2.4		V
Output short circuit current	I_{OS}	$V_{OUT} = V_{CC}$ V_{OUT} = GND	1, 2, 3		50 1/ 100 2/ 155 3/	mA
Supply current when not clocked	I_{CCSB}		1, 2, 3		1	mA
Supply current in RESET	I_{CCRES}		1, 2, 3		10	mA
Supply current in IDLE	I_{CCIDLE}		1, 2, 3		23	mA
Operating supply current	I_{CCOP}		1, 2, 3		40	mA
Input capacitance 4/	C_{IN}	V_{CC} = 0 V	4		15	pF
Input/Output capacitance 4/	C_{IO}	V_{CC} = 0 V	4		15	pF
CLK low to TDO high	t_{p1}		9, 10, 11		33	ns
CLK high to TMR1_EXP low	t_{p2}		9, 10, 11		38	ns
CLK high to LDO low	t_{p3}		9, 10, 11		27	ns
CLK10 high to HINTR* low	t_{p4}		9, 10, 11		41	ns
CLK10 high to IOB18 low	t_{p5}		9, 10, 11		27	ns

1/ Applicable for HDATA[7:0], HINTR*, TMR1_EXP, TMR2_EXP, TxD1, DATA[15:0], GPIO[7:0], IOB[24:22], IOB27 and TDO pins.
2/ Applicable for IOB[21:0] pins.
3/ Applicable for LDO and LSO pins.
4/ This parameter is tested initially and after major process changes, otherwise guaranteed.



	Millimeters		Inches	
A	2.21	2.67	.087	.105
A1	1.83	2.24	.072	.088
A2	0.254 REF		.010 REF	
c	0.15	0.20	.006	.008
D/E	31.80	32.80	1.252	1.291
D1/E1	18.80	19.30	.740	.760
e	0.635 BSC		.025 BSC	
L	6.50	6.75	.256	.266
N1/N2	25		25	

NOTE:

Lid is connected to ground.

FIGURE 1. Case outline.

Pin Number	Name	Pin Number	Name	Pin Number	Name	Pin Number	Name
1	PLLOUT	26	IOB9	51	DATA4	76	TMR2_CLK
2	GND	27	VCC	52	DATA5	77	RxD1
3	VCC	28	GND	53	DATA6	78	TMR1_EXP
4	VCC	29	IOB10	54	DATA7	79	TMR2_EXP
5	LDO	30	IOB11	55	DATA8	80	TxD1
6	LSO	31	IOB12	56	VCC	81	HDATA0
7	LDI	32	IOB13	57	GND	82	HDATA1
8	LSI	33	IOB14	58	DATA9	83	HDATA2
9	GND	34	IOB15	59	DATA10	84	HDATA3
10	TCK	35	IOB16	60	DATA11	85	HDATA4
11	TMS	36	IOB17	61	VCC	86	HDATA5
12	TDI	37	IOB18	62	GND	87	HDATA6
13	TRST*	38	IOB19	63	DATA12	88	VCC
14	TDO	39	IOB20	64	DATA13	89	GND
15	GND	40	IOB21	65	DATA14	90	HDATA7
16	VCC	41	IOB22	66	DATA15	91	HDATNADR*
17	IOB0	42	IOB23	67	GPIO0	92	HSEL*
18	IOB1	43	IOB24	68	GPIO1	93	HWRNRD
19	IOB2	44	IOB25	69	GPIO2	94	HINTR*
20	IOB3	45	IOB26	70	GPIO3	95	RESET*
21	IOB4	46	IOB27	71	GPIO4	96	CLK
22	IOB5	47	DATA0	72	GPIO5	97	VCC_3VOLT
23	IOB6	48	DATA1	73	GPIO6	98	GND
24	IOB7	49	DATA2	74	GPIO7	99	GND
25	IOB8	50	DATA3	75	TMR1_CLK	100	VCC

FIGURE 2. Terminal connections.

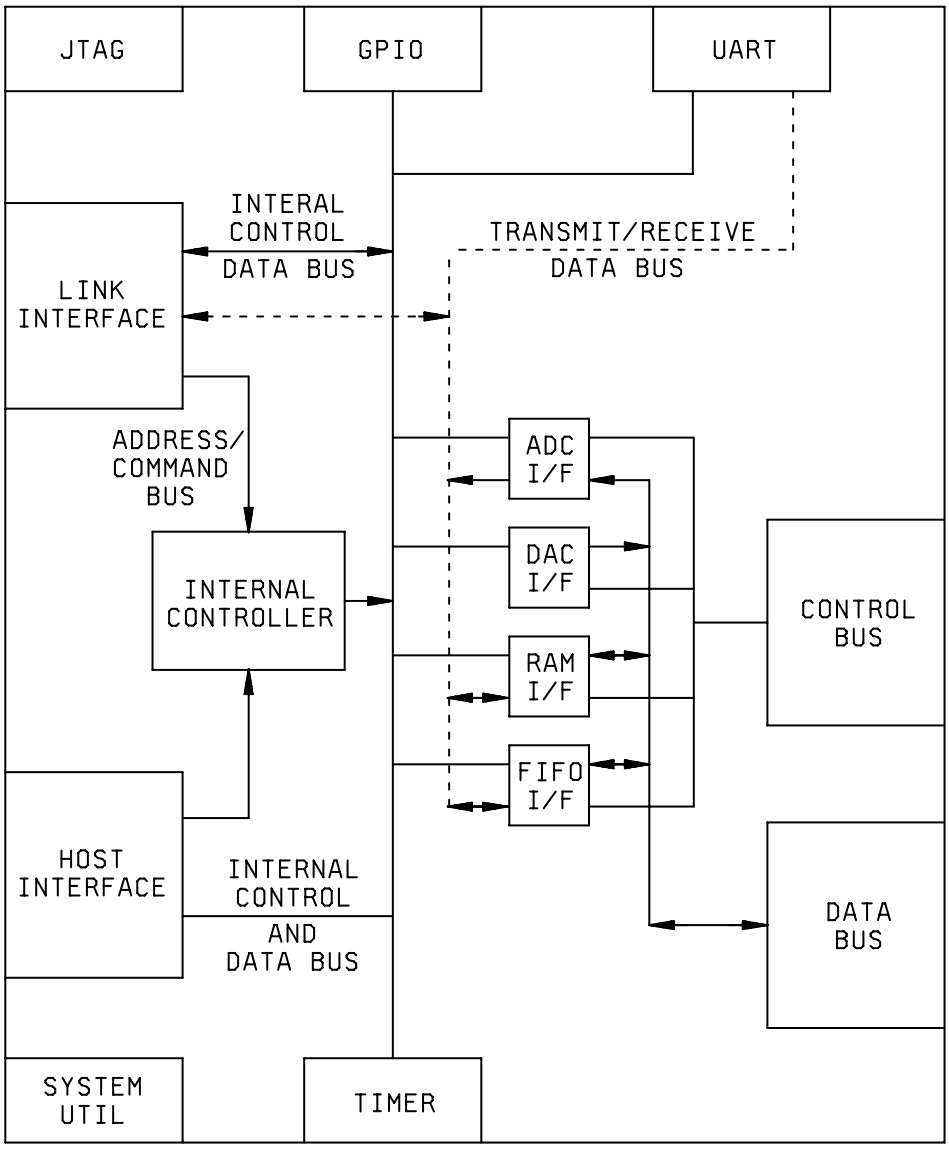


FIGURE 3. Block diagram.

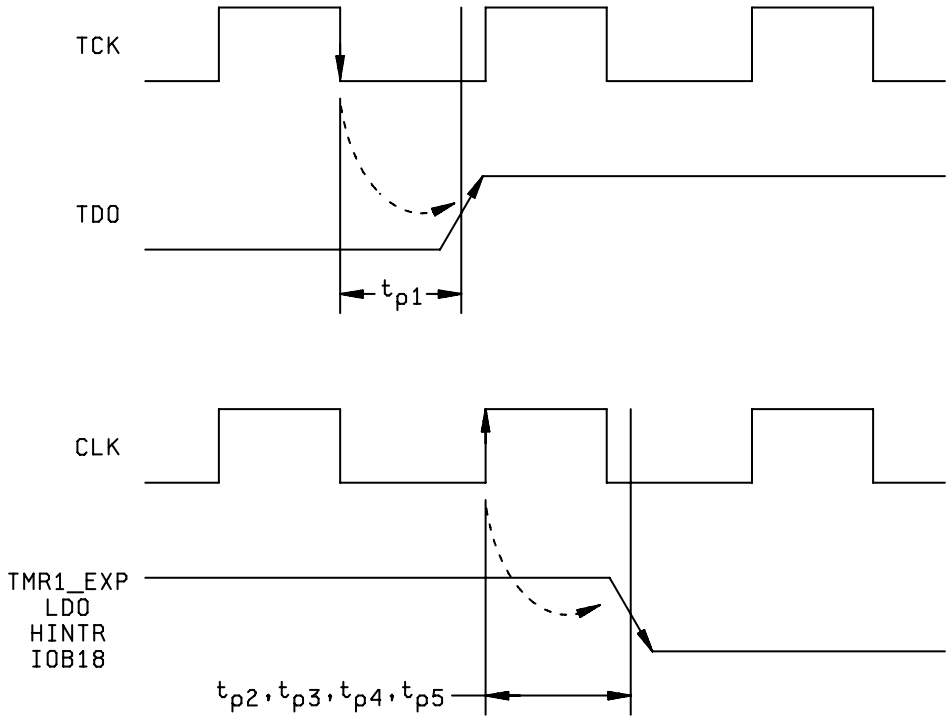


FIGURE 4. Timing waveforms.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, D or E . The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,7,9	1,7,9	1,7,9
Final electrical parameters (see 4.2)	1, 2, 3, 4, 7, 8, 9, 10, 11 1/	1, 2, 3, 4, 7, 8, 9, 10, 11 1/	1, 2, 3, 4, 7, 8, 9, 10, 11, 2/ 3/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9 3/
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.
3/ Delta limits, as specified in table IIB, shall be required where specified, and the delta values shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in delta parameters (25°C).

Parameter	Limit	Unit
IIL/IIH	+/- 10% of specificied value in table 1	µA
IOZL/IOZH	+/- 10% of specificied value in table 1	µA
ICCSB	+/- 10% of specificied value in table 1	mA

Note: The parameters shall be recorded before and after the required burn-in and lifetest to determine the delta limits.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition or . The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 08-06-18

Approved sources of supply for SMD 5962-08A02 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-08A0201QXC	3/	AT7912EKF-MQ
5962-08A0201VXC	3/	AT7912EKF-SV
5962-08A0202QXC	F7400	AT7912FKF-MQ
5962-08A0202VXC	F7400	AT7912FKF-SV

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ No longer available from an approved source of supplied.

Vendor CAGE number	Vendor name and address
F7400	ATMEL Nantes SA BP 70602 44306 Nantes Cedex 3, France