ARM-based Flash MCU

SAM4S Series

SUMMARY DATASHEET

Description

The Atmel SAM4S series is a member of a family of Flash microcontrollers based on the high performance 32-bit ARM Cortex-M4 RISC processor. It operates at a maximum speed of 120 MHz and features up to 2048 Kbytes of Flash, with optional dual bank implementation and cache memory, and up to 160 Kbytes of SRAM. The peripheral set includes a Full Speed USB Device port with embedded transceiver, a High Speed MCI for SDIO/SD/MMC, an External Bus Interface featuring a Static Memory Controller providing connection to SRAM, PSRAM, NOR Flash, LCD Module and NAND Flash, 2x USARTs, 2x UARTs, 2x TWIs, 3x SPI, an I2S, as well as 1 PWM timer, 2x three channel general-purpose 16-bit timers (with stepper motor and quadrature decoder logic support), an RTC, a 12-bit ADC, a 12-bit DAC and an analog comparator.

The SAM4S series is ready for capacitive touch thanks to the QTouch® library, offering an easy way to implement buttons, wheels and sliders.

The SAM4S device is a medium range general purpose microcontroller with the best ratio in terms of reduced power consumption, processing power and peripheral set. This enables the SAM4S to sustain a wide range of applications including consumer, industrial control, and PC peripherals.

It operates from 1.62V to 3.6V.

The SAM4S series is pin-to-pin compatible with the SAM3N, SAM3S series (64- and 100-pin versions) and SAM7S legacy series (64-pin versions).

1. Features

- Core
  - ARM® Cortex®-M4 with a 2Kbytes cache running at up to 120 MHz
  - Memory Protection Unit (MPU)
  - DSP Instruction Set
  - Thumb®-2 instruction set
- Pin-to-pin compatible with SAM3N, SAM3S products (64- and 100- pin versions) and SAM7S legacy products (64-pin version)
- Memories
  - Up to 2048 Kbytes embedded Flash with optional dual bank and cache memory
  - Up to 160 Kbytes embedded SRAM
  - 16 Kbytes ROM with embedded boot loader routines (UART, USB) and IAP routines
  - 8-bit Static Memory Controller (SMC): SRAM, PSRAM, NOR and NAND Flash support

- System
  - Embedded voltage regulator for single supply operation
  - Power-on-Reset (POR), Brown-out Detector (BOD) and Watchdog for safe operation
  - Quartz or ceramic resonator oscillators: 3 to 20 MHz main power with Failure Detection and optional low-power 32.768 kHz for RTC or device clock
  - RTC with Gregorian and Persian Calendar mode, waveform generation in low-power modes
  - RTC clock calibration circuitry for 32.768 kHz crystal frequency compensation
  - High precision 8/12 MHz factory trimmed internal RC oscillator with 4 MHz default frequency for device startup. In-application trimming access for frequency adjustment
  - Slow Clock Internal RC oscillator as permanent low-power mode device clock
  - Two PLLs up to 240 MHz for device clock and for USB
  - Temperature Sensor
  - Up to 22 Peripheral DMA (PDC) Channels
- Low Power Modes
  - Sleep and Backup Modes, down to 1 µA in Backup Mode
  - Ultra low-power RTC
- Peripherals
  - USB 2.0 Device: 12 Mbps, 2668 byte FIFO, up to 8 bidirectional Endpoints. On-Chip Transceiver
  - Up to 2 USARTs with ISO7816, IrDA®, RS-485, SPI, Manchester and Modem Mode
  - Two 2-wire UARTs
  - Up to 2 Two Wire Interface (I2C compatible), 1 SPI, 1 Serial Synchronous Controller (I2S), 1 High Speed Multimedia Card Interface (SDIO/SD Card/MMC)
  - 2 Three-Channel 16-bit Timer/Counter with capture, waveform, compare and PWM mode. Quadrature Decoder Logic and 2-bit Gray Up/Down Counter for Stepper Motor
  - 4-channel 16-bit PWM with Complementary Output, Fault Input, 12-bit Dead Time Generator Counter for Motor Control
  - 32-bit Real-time Timer and RTC with calendar, alarm and 32 kHz trimming features
  - Up to 16-channel, 1Msps ADC with differential input mode and programmable gain stage and auto calibration
  - One 2-channel 12-bit 1Msps DAC
  - One Analog Comparator with flexible input selection, Selectable input hysteresis
  - 32-bit Cyclic Redundancy Check Calculation Unit (CRCCU)
  - Write Protected Registers
- I/O
  - Up to 79 I/O lines with external interrupt capability (edge or level sensitivity), debouncing, glitch filtering and on-die Series Resistor Termination
  - Three 32-bit Parallel Input/Output Controllers, Peripheral DMA assisted Parallel Capture Mode
- Packages
  - 100-lead LQFP, 14 x 14 mm, pitch 0.5 mm/ 100-ball TFBGA, 9 x 9 mm, pitch 0.8 mm/ 100-ball VFBGA, 7 x 7 mm, pitch 0.65 mm
  - 64-lead LQFP, 10 x 10 mm, pitch 0.5 mm/ 64-pad QFN 9x9 mm, pitch 0.5 mm

1.1 Configuration Summary

The SAM4S series devices differ in memory size, package and features. Table 1-1 summarizes the configurations of the device family.

Table 1-1. Configuration Summary

Feature	SAM4SD32C	SAM4SD32B	SAM4SD16C	SAM4SD16B	SAM4SA16C	SAM4SA16B	SAM4S16C	SAM4S16B	SAM4S8C	SAM4S8B
Flash	2 x 1024 Kbytes	2 x 1024 Kbytes	2 x 512 Kbytes	2 x 512 Kbytes	1024 Kbytes	1024 Kbytes	1024 Kbytes	1024 Kbytes	512 Kbytes	512 Kbytes
SRAM	160 Kbytes	160 Kbytes	160 Kbytes	160 Kbytes	160 Kbytes	160 Kbytes	128 Kbytes	128 Kbytes	128 Kbytes	128 Kbytes
HCACHE	2Kbytes	2Kbytes	2Kbytes	2Kbytes	2Kbytes	2Kbytes	-	-	-	-
Package	LQFP 100 TFBGA 100 VFBGA 100	LQFP 64 QFN 64	LQFP 100 TFBGA 100 VFBGA 100	LQFP 64 QFN 64	LQFP 100 TFBGA 100 VFBGA 100	LQFP 64 QFN 64	LQFP 100 TFBGA 100 VFBGA 100	LQFP 64 LFBGA 64	LQFP 100 TFBGA 100 VFBGA 100	LQFP 64 QFN 64
Number of PIOs	79	47	79	47	79	47	79	47	79	47
External Bus Interface	8-bit data, 4chip selects, 24-bit address	-	8-bit data, 4chip selects, 24-bit address	-	8-bit data, 4chip selects, 24-bit address	-	8-bit data, 4chip selects, 24-bit address	-	8-bit data, 4chip selects, 24-bit address	-
Central DMA	6	4	6	4	6	4	6	4	6	6
12-bit ADC	16 ch.(1)	11 ch.(1)	16 ch.(1)	11 ch.(1)	16 ch.(1)	11 ch.(1)	16 ch.(1)	11 ch.(1)	16 ch.(1)	11 ch.(1)
12-bit DAC	2 ch.	2 ch.	2 ch.	2 ch.	2 ch.	2 ch.	2 ch.	2 ch.	2 ch.	2 ch.
Timer Counter Channels	6	3	6	3	6	3	6	3	6	3
PDC Channels	22	22	22	22	22	22	22	22	22	22
USART/ UART	2/2(2)	2/2(2)	2/2(2)	2/2(2)	2/2(2)	2/2(2)	2/2(2)	2/2(2)	2/2(2)	2/2(2)
HSMCI	1 port 4 bits	1 port 4 bits	1 port 4 bits	1 port 4 bits	1 port 4 bits	1 port 4 bits	1 port 4 bits	1 port 4 bits	1 port 4 bits	1 port 4 bits

Notes: 1. One channel is reserved for internal temperature sensor.
2. Full Modem support on USART1.

2. Block Diagram

Figure 2-1. SAM4S16/S8 Series 100-pin Version Block Diagram

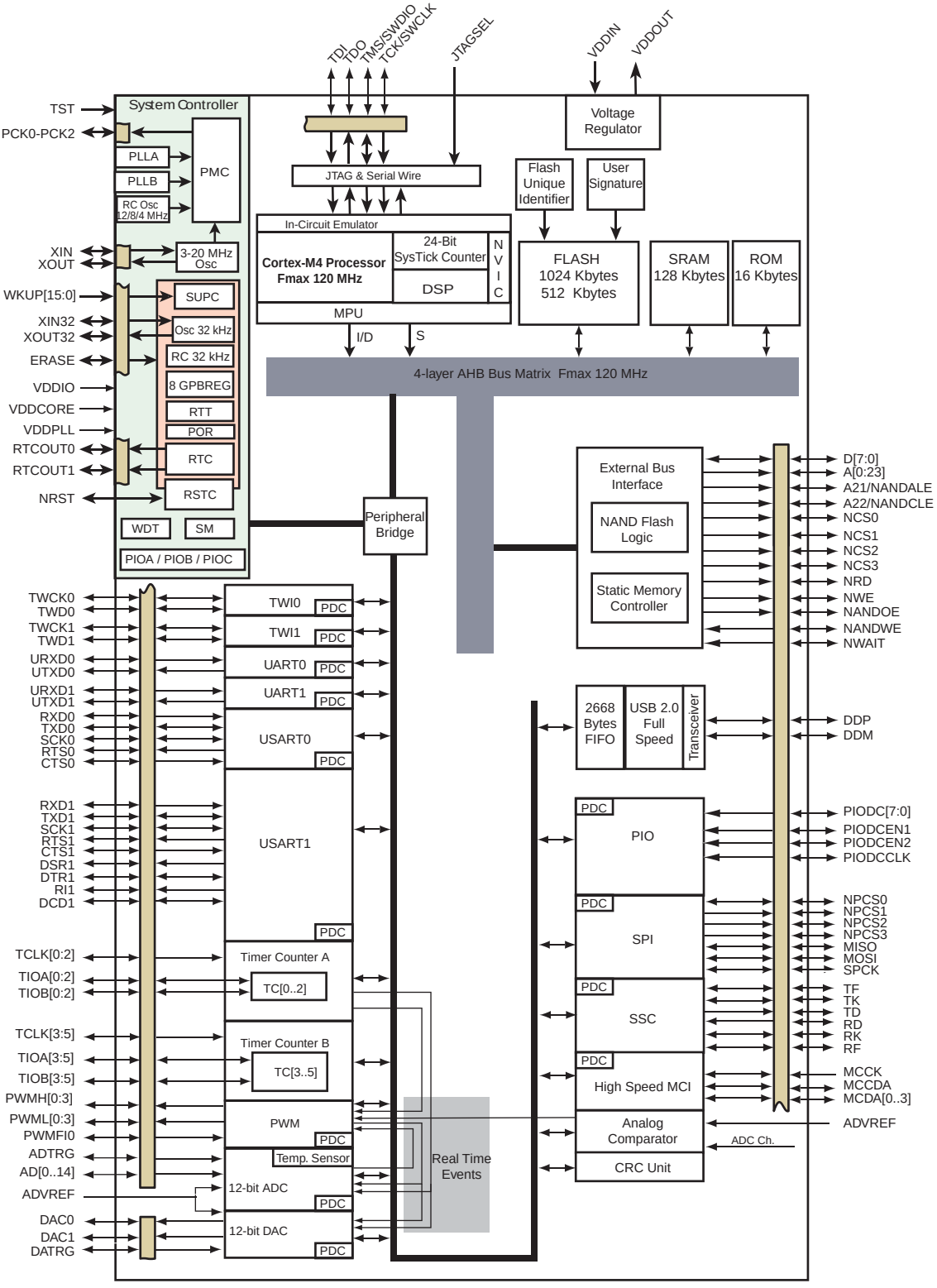


Figure 2-2. SAM4S16/S8 Series 64-pin Version Block Diagram

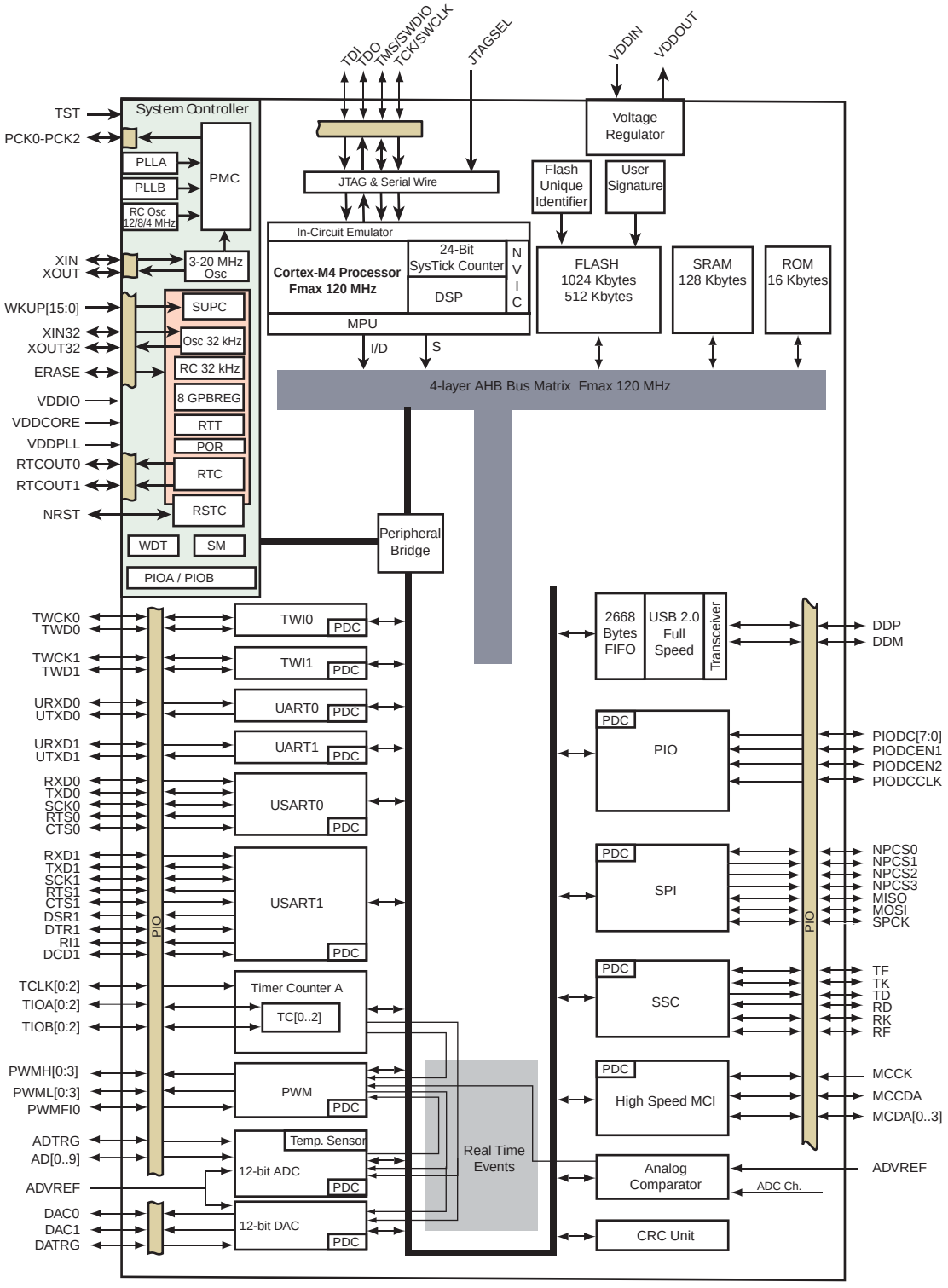


Figure 2-3. SAM4SD32/SD16/SA16 100-pin Version Block Diagram

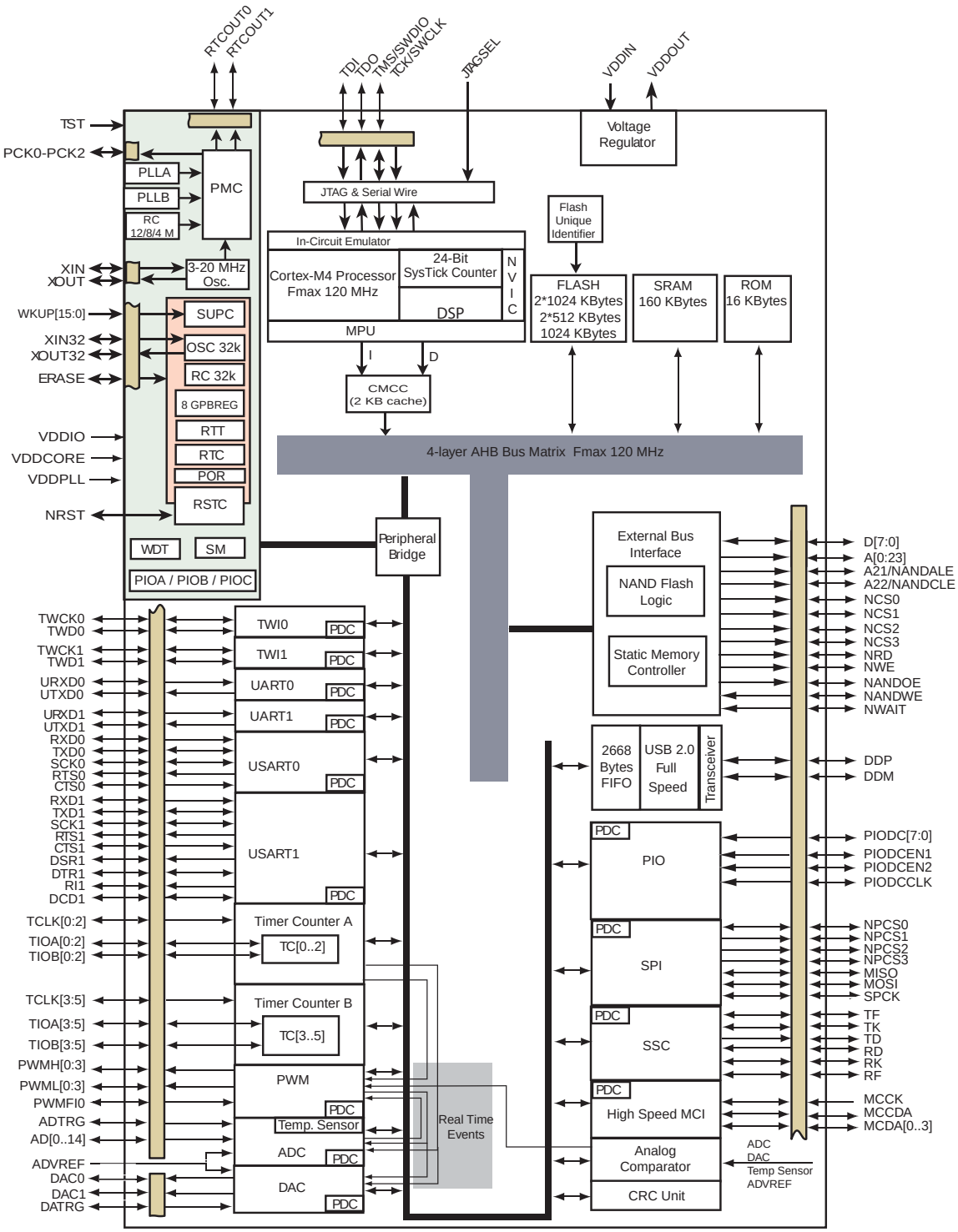
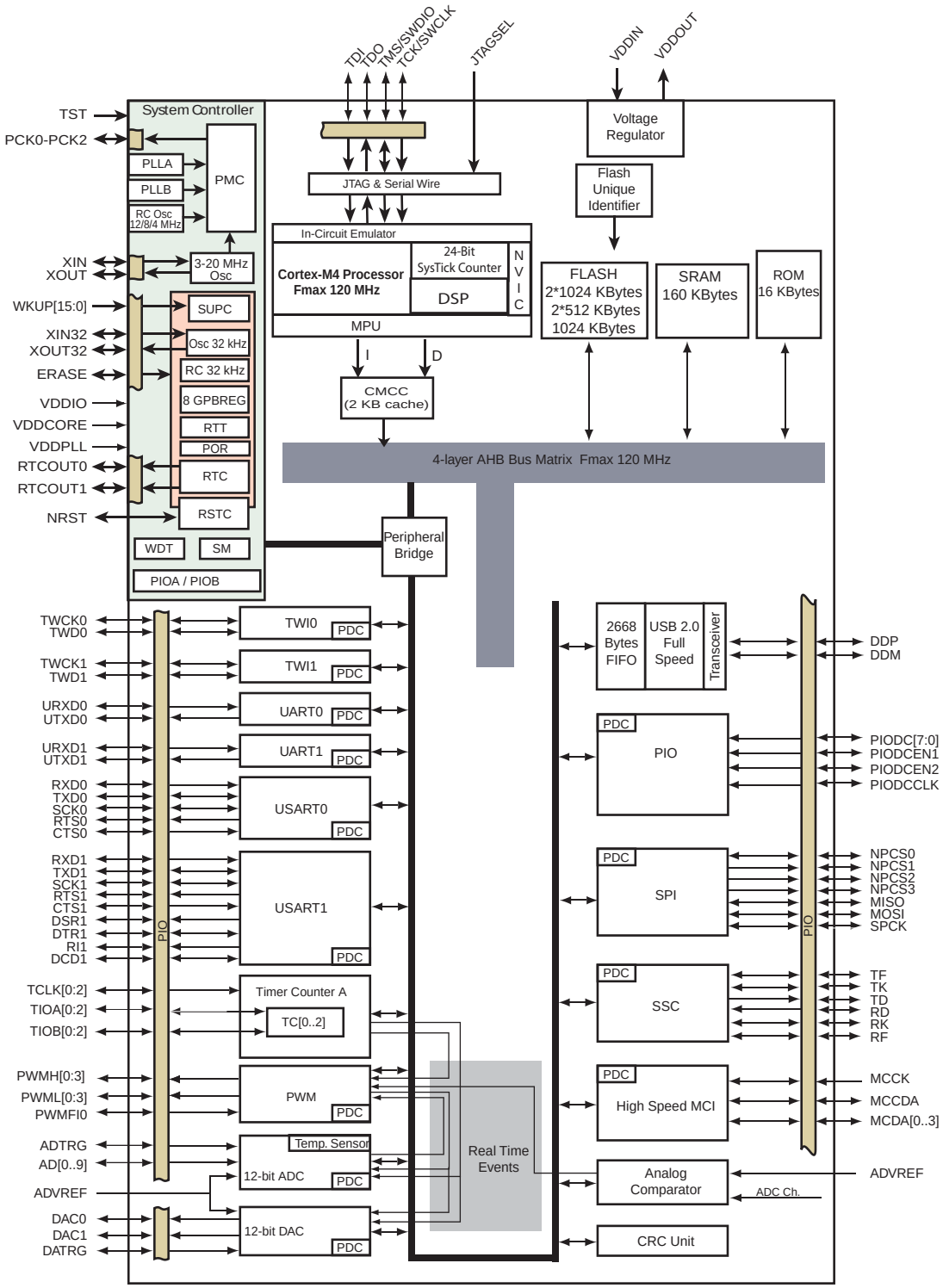


Figure 2-4. SAM4SD32/SD16/SA16 64-pin Version Block Diagram



3. Signal Description

Table 3-1 gives details on signal names classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Voltage reference	Comments
Power Supplies					
VDDIO	Peripherals I/O Lines and USB transceiver Power Supply	Power			1.62V to 3.6V
VDDIN	Voltage Regulator Input, ADC, DAC and Analog Comparator Power Supply	Power			1.62V to 3.6V[4]
VDDOUT	Voltage Regulator Output	Power			1.2V Output
VDDPLL	Oscillator and PLL Power Supply	Power			1.08 V to 1.32V
VDDCORE	Power the core, the embedded memories and the peripherals	Power			1.08V to 1.32V
GND	Ground	Ground			
Clocks, Oscillators and PLLs					
XIN	Main Oscillator Input	Input		VDDIO	Reset State: - PIO Input - Internal Pull-up disabled - Schmitt Trigger enabled[1]
XOUT	Main Oscillator Output	Output			
XIN32	Slow Clock Oscillator Input	Input			
XOUT32	Slow Clock Oscillator Output	Output			
PCK0 - PCK2	Programmable Clock Output	Output			Reset State: - PIO Input - Internal Pull-up enabled - Schmitt Trigger enabled[1]
Real Time Clock					
RTCOUT0	Programmable RTC waveform output	Output		VDDIO	Reset State: - PIO Input - Internal Pull-up disabled - Schmitt Trigger enabled[1]
RTCOUT1	Programmable RTC waveform output	Output			
Serial Wire/JTAG Debug Port - SWJ-DP					
TCK/SWCLK	Test Clock/Serial Wire Clock	Input		VDDIO	Reset State: - SWJ-DP Mode - Internal pull-up disabled[5] - Schmitt Trigger enabled[1]
TDI	Test Data In	Input			
TDO/TRACESWO	Test Data Out / Trace Asynchronous Data Out	Output			
TMS/SWDIO	Test Mode Select /Serial Wire Input/Output	Input / I/O			
JTAGSEL	JTAG Selection	Input	High		Permanent Internal pull-down

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage reference	Comments
Flash Memory					
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	VDDIO	Reset State: - Erase Input - Internal pull-down enabled - Schmitt Trigger enabled(1)
Reset/Test					
NRST	Synchronous Microcontroller Reset	I/O	Low	VDDIO	Permanent Internal pull-up
TST	Test Select	Input			Permanent Internal pull-down
Universal Asynchronous Receiver Transceiver - UARTx					
URXDx	UART Receive Data	Input			
UTXDx	UART Transmit Data	Output			
PIO Controller - PIOA - PIOB - PIOC					
PA0 - PA31	Parallel IO Controller A	I/O		VDDIO	Reset State: - PIO or System IOs(2) - Internal pull-up enabled - Schmitt Trigger enabled(1)
PB0 - PB14	Parallel IO Controller B	I/O			
PC0 - PC31	Parallel IO Controller C	I/O			
PIO Controller - Parallel Capture Mode					
PIODC0-PIODC7	Parallel Capture Mode Data	Input		VDDIO	
PIODCCLK	Parallel Capture Mode Clock	Input			
PIODCEN1-2	Parallel Capture Mode Enable	Input			
External Bus Interface					
D0 - D7	Data Bus	I/O			
A0 - A23	Address Bus	Output			
NWAIT	External Wait Signal	Input	Low		
Static Memory Controller - SMC					
NCS0 - NCS3	Chip Select Lines	Output	Low		
NRD	Read Signal	Output	Low		
NWE	Write Enable	Output	Low		
NAND Flash Logic					
NANDOE	NAND Flash Output Enable	Output	Low		
NANDWE	NAND Flash Write Enable	Output	Low		
High Speed Multimedia Card Interface - HSMCI					
MCCK	Multimedia Card Clock	I/O			
MCCDA	Multimedia Card Slot A Command	I/O			
MCDA0 - MCDA3	Multimedia Card Slot A Data	I/O			
Universal Synchronous Asynchronous Receiver Transmitter USARTx					

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage reference	Comments
SCKx	USARTx Serial Clock	I/O			
TXDx	USARTx Transmit Data	I/O			
RXDx	USARTx Receive Data	Input			
RTSx	USARTx Request To Send	Output			
CTSx	USARTx Clear To Send	Input			
DTR1	USART1 Data Terminal Ready	I/O			
DSR1	USART1 Data Set Ready	Input			
DCD1	USART1 Data Carrier Detect	Output			
RI1	USART1 Ring Indicator	Input			
Synchronous Serial Controller - SSC					
TD	SSC Transmit Data	Output			
RD	SSC Receive Data	Input			
TK	SSC Transmit Clock	I/O			
RK	SSC Receive Clock	I/O			
TF	SSC Transmit Frame Sync	I/O			
RF	SSC Receive Frame Sync	I/O			
Timer/Counter - TC					
TCLKx	TC Channel x External Clock Input	Input			
TIOAx	TC Channel x I/O Line A	I/O			
TIOBx	TC Channel x I/O Line B	I/O			
Pulse Width Modulation Controller- PWMC					
PWMHx	PWM Waveform Output High for channel x	Output			
PWMLx	PWM Waveform Output Low for channel x	Output			The only output in complementary mode when dead time insertion is enabled.
PWMFI0	PWM Fault Input	Input			
Serial Peripheral Interface - SPI					
MISO	Master In Slave Out	I/O			
MOSI	Master Out Slave In	I/O			
SPCK	SPI Serial Clock	I/O			
SPI_NPCS0	SPI Peripheral Chip Select 0	I/O	Low		
SPI_NPCS1 - SPI_NPCS3	SPI Peripheral Chip Select	Output	Low		

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage reference	Comments
Two-Wire Interface- TWI					
TWDx	TWIx Two-wire Serial Data	I/O			
TWCKx	TWIx Two-wire Serial Clock	I/O			
Analog					
ADVREF	ADC, DAC and Analog Comparator Reference	Analog			
12-bit Analog-to-Digital Converter - ADC					
AD0-AD14	Analog Inputs	Analog, Digital			
ADTRG	ADC Trigger	Input		VDDIO	
12-bit Digital-to-Analog Converter - DAC					
DAC0 - DAC1	Analog output	Analog, Digital			
DACTRG	DAC Trigger	Input		VDDIO	
Fast Flash Programming Interface - FFPI					
PGMEN0-PGMEN2	Programming Enabling	Input		VDDIO	
PGMM0-PGMM3	Programming Mode	Input		VDDIO	
PGMD0-PGMD15	Programming Data	I/O			
PGMRDY	Programming Ready	Output	High		
PGMNVALID	Data Direction	Output	Low		
PGMNOE	Programming Read	Input	Low		
PGMCK	Programming Clock	Input			
PGMNCMD	Programming Command	Input	Low		
USB Full Speed Device					
DDM	USB Full Speed Data -	Analog, Digital		VDDIO	Reset State: - USB Mode - Internal Pull-down(3)
DDP	USB Full Speed Data +				

Note:
1. Schmitt Triggers can be disabled through PIO registers.
2. Some PIO lines are shared with System I/Os.
3. Refer to USB Section of the product Electrical Characteristics for information on Pull-down value in USB Mode.
4. See “Typical Powering Schematics” Section for restrictions on voltage range of Analog Cells.
5. TDO pin is set in input mode when the Cortex-M4 Core is not in debug mode. Thus the internal pull-up corresponding to this PIO line must be enabled to avoid current consumption due to floating input.

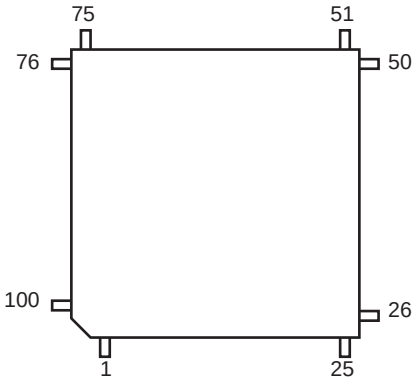
4. Package and Pinout

SAM4S devices are pin-to-pin compatible with SAM3N, SAM3S products in 64- and 100-pin versions, and AT91SAM7S legacy products in 64-pin versions.

4.1 SAM4SD32/SD16/SA16/S16/S8C Package and Pinout

4.1.1 100-Lead LQFP Package Outline

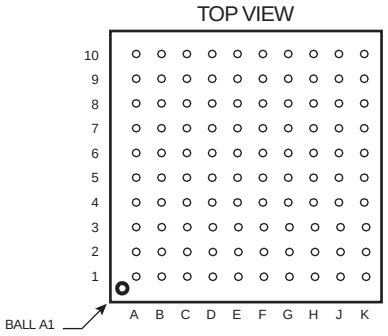
Figure 4-1. Orientation of the 100-lead LQFP Package



4.1.2 100-ball TFBGA Package Outline

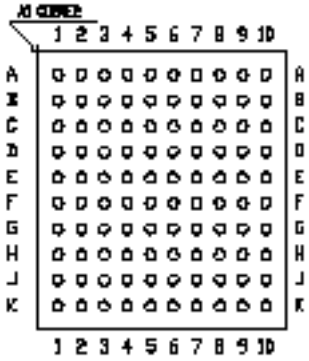
The 100-Ball TFBGA package has a 0.8 mm ball pitch and respects Green Standards. Its dimensions are 9 x 9 x 1.1 mm. Figure 4-2 shows the orientation of the 100-ball TFBGA Package.

Figure 4-2. Orientation of the 100-ball TFBGA Package



4.1.3 100-ball VFBGA Package Outline

Figure 4-3. Orientation of the 100-ball VFBGA Package



4.1.4 100-Lead LQFP Pinout

Table 4-1. SAM4SD32/SD16/SA16/S16/S8C 100-lead LQFP Pinout

1	ADVREF	26	GND	51	TDI/PB4	76	TDO/TRACESWO/ PB5
2	GND	27	VDDIO	52	PA6/PGMNOE	77	JTAGSEL
3	PB0/AD4	28	PA16/PGMD4	53	PA5/PGMRDY	78	PC18
4	PC29/AD13	29	PC7	54	PC28	79	TMS/SWDIO/PB6
5	PB1/AD5	30	PA15/PGMD3	55	PA4/PGMNCMD	80	PC19
6	PC30/AD14	31	PA14/PGMD2	56	VDDCORE	81	PA31
7	PB2/AD6	32	PC6	57	PA27/PGMD15	82	PC20
8	PC31	33	PA13/PGMD1	58	PC8	83	TCK/SWCLK/PB7
9	PB3/AD7	34	PA24/PGMD12	59	PA28	84	PC21
10	VDDIN	35	PC5	60	NRST	85	VDDCORE
11	VDDOUT	36	VDDCORE	61	TST	86	PC22
12	PA17/PGMD5/ AD0	37	PC4	62	PC9	87	ERASE/PB12
13	PC26	38	PA25/PGMD13	63	PA29	88	DDM/PB10
14	PA18/PGMD6/ AD1	39	PA26/PGMD14	64	PA30	89	DDP/PB11
15	PA21/PGMD9/ AD8	40	PC3	65	PC10	90	PC23
16	VDDCORE	41	PA12/PGMD0	66	PA3	91	VDDIO
17	PC27	42	PA11/PGMM3	67	PA2/PGMEN2	92	PC24
18	PA19/PGMD7/ AD12	43	PC2	68	PC11	93	PB13/DAC0
19	PC15/AD11	44	PA10/PGMM2	69	VDDIO	94	PC25
20	PA22/PGMD10/ AD9	45	GND	70	GND	95	GND
21	PC13/AD10	46	PA9/PGMM1	71	PC14	96	PB8/XOUT
22	PA23/PGMD11	47	PC1	72	PA1/PGMEN1	97	PB9/PGMCK/XIN
23	PC12/AD12	48	PA8/XOUT32/ PGMM0	73	PC16	98	VDDIO
24	PA20/PGMD8/ AD3	49	PA7/XIN32/ PGMNVALID	74	PA0/PGMEN0	99	PB14/DAC1
25	PC0	50	VDDIO	75	PC17	100	VDDPLL

4.1.5 100-Ball TFBGA Pinout

Table 4-2. SAM4SD32/SD16/SA16/S16/S8 100-ball TFBGA Pinout

A1	PB1/AD5	C6	TCK/SWCLK/PB7	F1	PA18/PGMD6/ AD1	H6	PC4
A2	PC29	C7	PC16	F2	PC26	H7	PA11/PGMM3
A3	VDDIO	C8	PA1/PGMEN1	F3	VDDOUT	H8	PC1
A4	PB9/PGMCK/XIN	C9	PC17	F4	GND	H9	PA6/PGMNOE
A5	PB8/XOUT	C10	PA0/PGMEN0	F5	VDDIO	H10	TDI/PB4
A6	PB13/DAC0	D1	PB3/AD7	F6	PA27/PGMD15	J1	PC15/AD11
A7	DDP/PB11	D2	PB0/AD4	F7	PC8	J2	PC0
A8	DDM/PB10	D3	PC24	F8	PA28	J3	PA16/PGMD4
A9	TMS/SWDIO/PB6	D4	PC22	F9	TST	J4	PC6
A10	JTAGSEL	D5	GND	F10	PC9	J5	PA24/PGMD12
B1	PC30	D6	GND	G1	PA21/PGMD9/AD8	J6	PA25/PGMD13
B2	ADVREF	D7	VDDCORE	G2	PC27	J7	PA10/PGMM2
B3	GNDANA	D8	PA2/PGMEN2	G3	PA15/PGMD3	J8	GND
B4	PB14/DAC1	D9	PC11	G4	VDDCORE	J9	VDDCORE
B5	PC21	D10	PC14	G5	VDDCORE	J10	VDDIO
B6	PC20	E1	PA17/PGMD5/ AD0	G6	PA26/PGMD14	K1	PA22/PGMD10/ AD9
B7	PA31	E2	PC31	G7	PA12/PGMD0	K2	PC13/AD10
B8	PC19	E3	VDDIN	G8	PC28	K3	PC12/AD12
B9	PC18	E4	GND	G9	PA4/PGMNCMD	K4	PA20/PGMD8/ AD3
B10	TDO/TRACESWO/ PB5	E5	GND	G10	PA5/PGMRDY	K5	PC5
C1	PB2/AD6	E6	NRST	H1	PA19/PGMD7/ AD2	K6	PC3
C2	VDDPLL	E7	PA29/AD13	H2	PA23/PGMD11	K7	PC2
C3	PC25	E8	PA30/AD14	H3	PC7	K8	PA9/PGMM1
C4	PC23	E9	PC10	H4	PA14/PGMD2	K9	PA8/XOUT32/ PGMM0
C5	ERASE/PB12	E10	PA3	H5	PA13/PGMD1	K10	PA7/XIN32/ PGMNVALID

4.1.6 100-Ball VFBGA Pinout

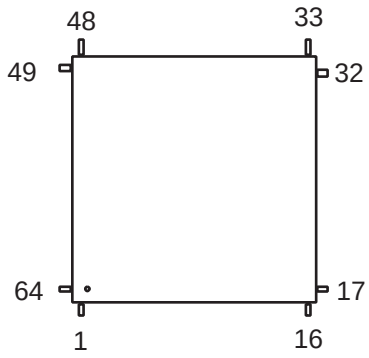
Table 4-3. SAM4SD32/SD16/SA16/S16/S8 100-ball VFBGA Pinout

A1	ADVREF	C6	PC9	F1	VDDOUT	H6	PA12/PGMD0
A2	VDDPLL	C7	TMS/SWDIO/PB6	F2	PA18/PGMD6/ AD1	H7	PA9/PGMM1
A3	PB9/PGMCK/XIN	C8	PA1/PGMEN1	F3	PA17/PGMD5/ AD0	H8	VDDCORE
A4	PB8/XOUT	C9	PA0/PGMEN0	F4	GND	H9	PA6/PGMNOE
A5	JTAGSEL	C10	PC16	F5	GND	H10	PA5/PGMRDY
A6	DDP/PB11	D1	PB1/AD5	F6	PC26	J1	PA20/AD3
A7	DDM/PB10	D2	PC30	F7	PA4/PGMNCMD	J2	PC12/AD12
A8	PC20	D3	PC31	F8	PA28	J3	PA16/PGMD4
A9	PC19	D4	PC22	F9	TST	J4	PC6
A10	TDO/TRACESWO/ PB5	D5	PC5	F10	PC8	J5	PA24
B1	GNDANA	D6	PA29/AD13	G1	PC15/AD11	J6	PA25
B2	PC25	D7	PA30/AD14	G2	PA19/PGMD7/ AD2	J7	PA11/PGMM3
B3	PB14/DAC1	D8	GND	G3	PA21/AD8	J8	VDDCORE
B4	PB13/DAC0	D9	PC14	G4	PA15/PGMD3	J9	VDDCORE
B5	PC23	D10	PC11	G5	PC3	J10	TDI/PB4
B6	PC21	E1	VDDIN	G6	PA10/PGMM2	K1	PA23
B7	TCK/SWCLK/PB7	E2	PB3/AD7	G7	PC1	K2	PC0
B8	PA31	E3	PB2/AD6	G8	PC28	K3	PC7
B9	PC18	E4	GND	G9	NRST	K4	PA13/PGMD1
B10	PC17	E5	GND	G10	PA27	K5	PA26
C1	PB0/AD4	E6	GND	H1	PC13/AD10	K6	PC2
C2	PC29	E7	VDDIO	H2	PA22/AD9	K7	VDDIO
C3	PC24	E8	PC10	H3	PC27	K8	VDDIO
C4	ERASE/PB12	E9	PA2/PGMEN2	H4	PA14/PGMD2	K9	PA8/XOUT32/ PGMM0
C5	VDDCORE	E10	PA3	H5	PC4	K10	PA7/XIN32/ PGMNVALID

4.2 SAM4SD32/SD16/SA16/S16/S8 Package and Pinout

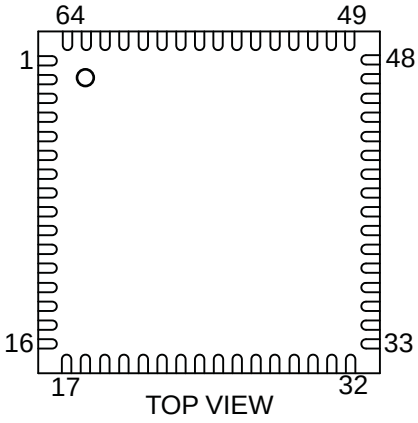
4.2.1 64-Lead LQFP Package Outline

Figure 4-4. Orientation of the 64-lead LQFP Package



4.2.2 64-lead QFN Package Outline

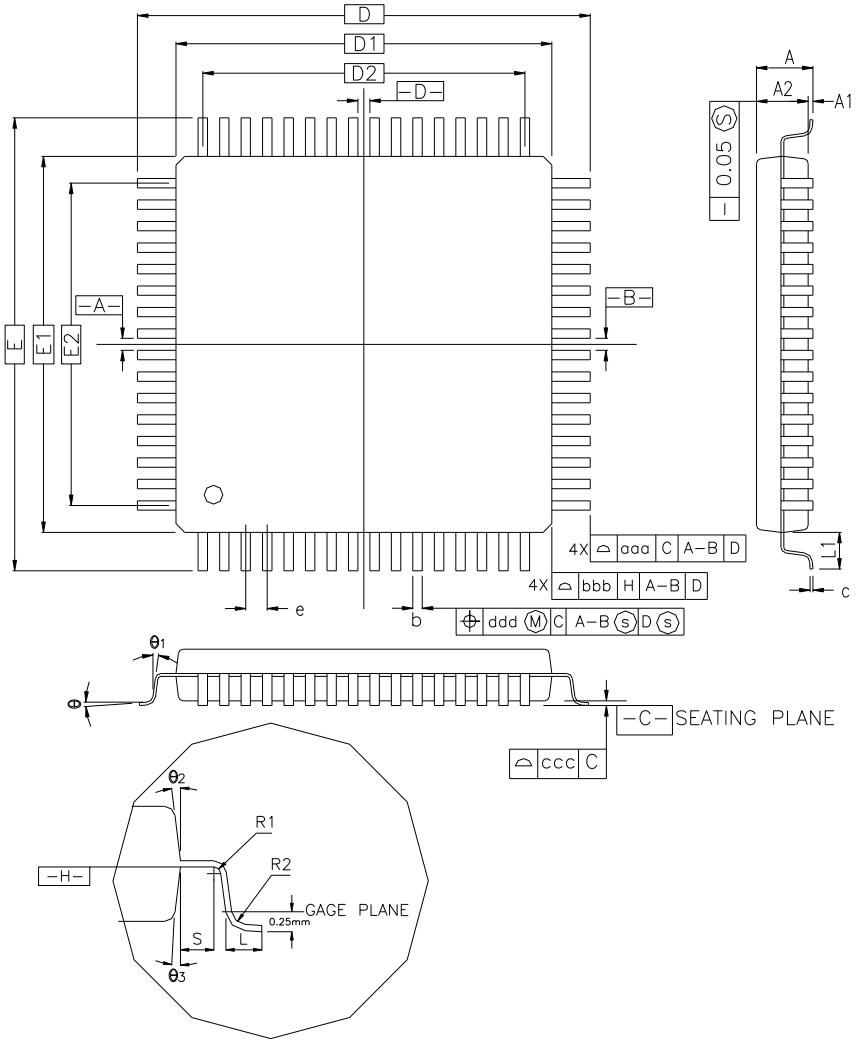
Figure 4-5. Orientation of the 64-lead QFN Package



5. Package Drawings

The SAM4S series devices are available in LQFP, QFN, TFBGA and VFBGA packages.

Figure 5-1. 100-lead LQFP Package Mechanical Drawing

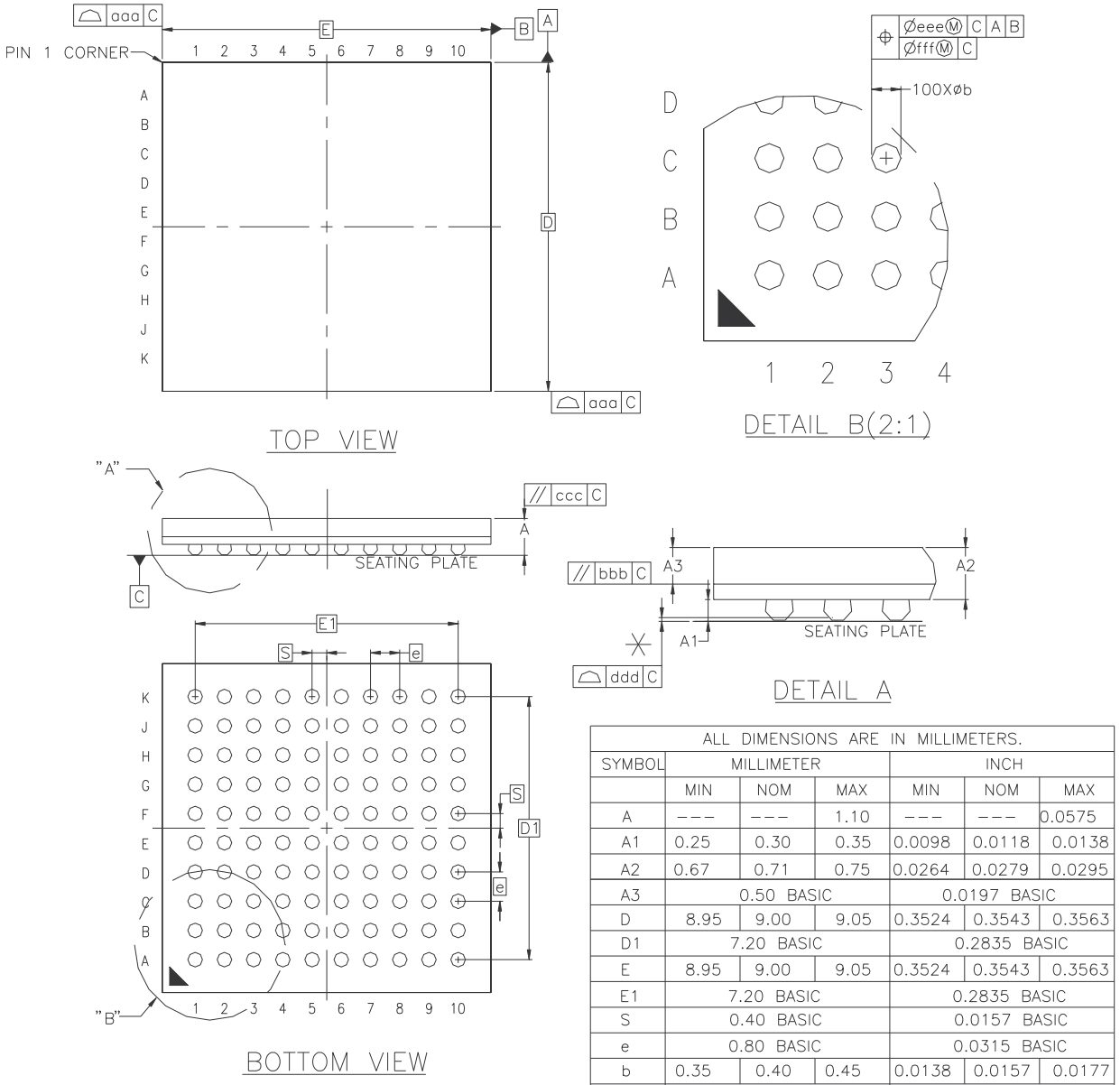


COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC.			0.630 BSC.		
D_1	14.00 BSC.			0.551 BSC.		
E	16.00 BSC.			0.630 BSC.		
E_1	14.00 BSC.			0.551 BSC.		
R_2	0.08	—	0.20	0.003	—	0.008
R_1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	12.00			0.472		
E2	12.00			0.472		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Note : 1. This drawing is for general information only. Refer to JEDEC Drawing MS-026 for additional information.

Figure 5-2. 100-ball TFBGA Package Mechanical Drawing



ALL DIMENSIONS ARE IN MILLIMETERS.						
SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.0575
A1	0.25	0.30	0.35	0.0098	0.0118	0.0138
A2	0.67	0.71	0.75	0.0264	0.0279	0.0295
A3	0.50 BASIC			0.0197 BASIC		
D	8.95	9.00	9.05	0.3524	0.3543	0.3563
D1	7.20 BASIC			0.2835 BASIC		
E	8.95	9.00	9.05	0.3524	0.3543	0.3563
E1	7.20 BASIC			0.2835 BASIC		
S	0.40 BASIC			0.0157 BASIC		
e	0.80 BASIC			0.0315 BASIC		
b	0.35	0.40	0.45	0.0138	0.0157	0.0177
aaa	0.15			0.0059		
bbb	0.20			0.0079		
ccc	0.20			0.0079		
ddd	0.12			0.0047		
eee	0.15			0.0059		
fff	0.08			0.0031		

Figure 5-3. 100-ball VFBGA Package Mechanical Drawing

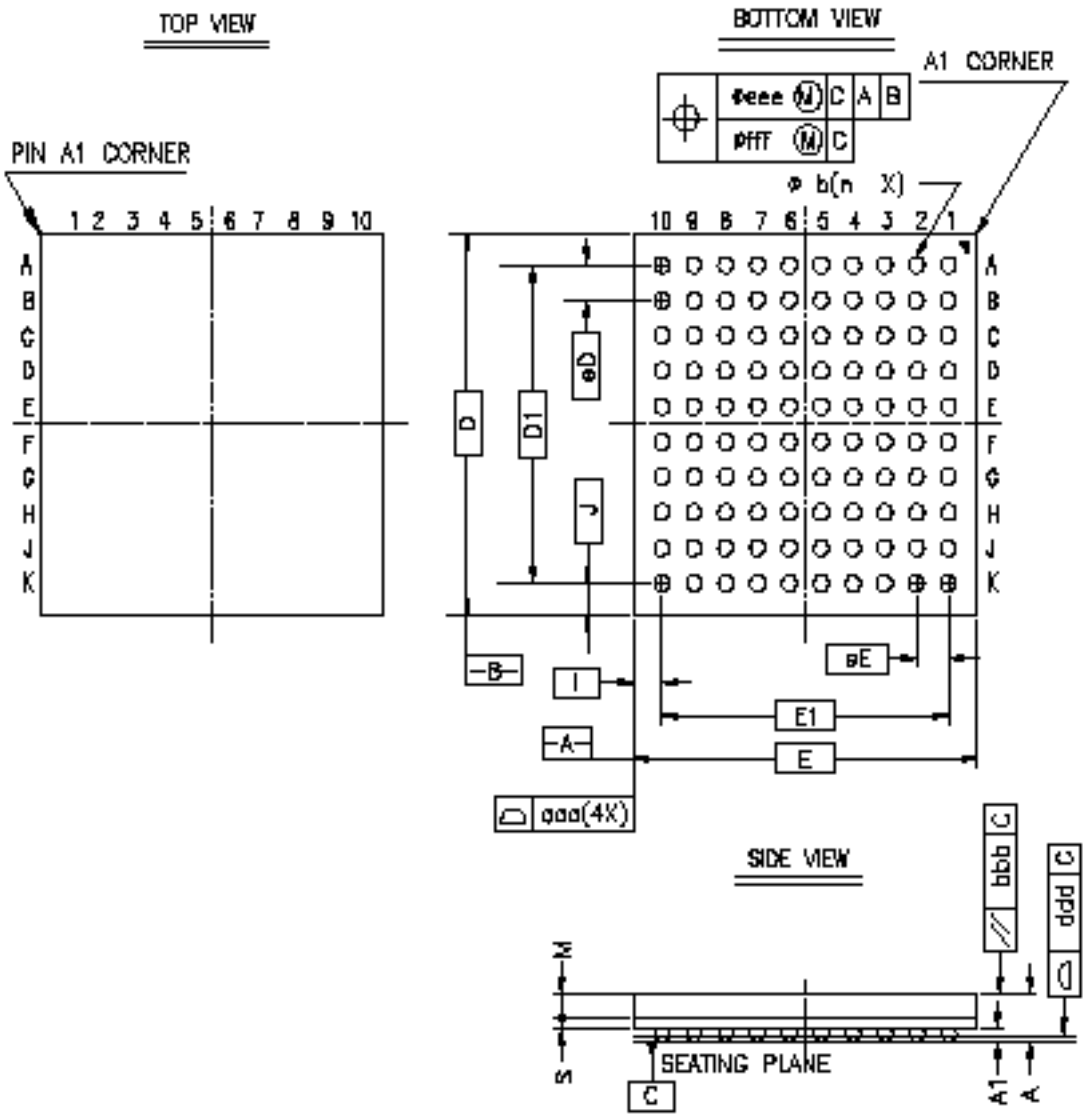
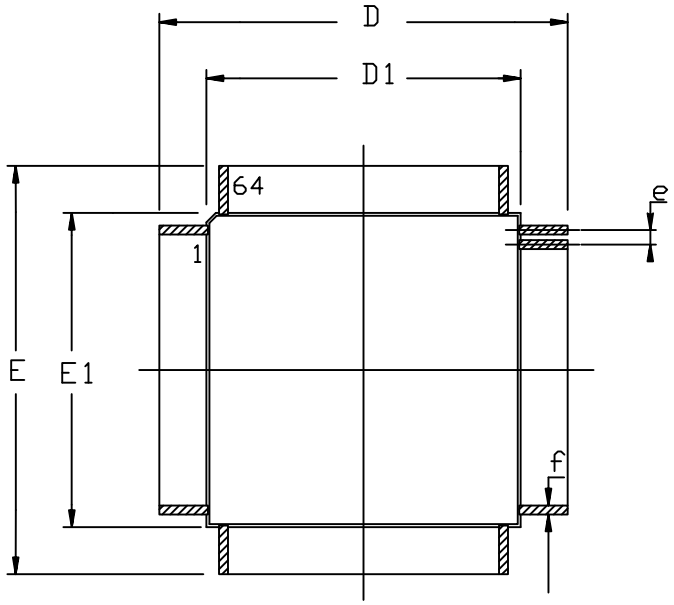
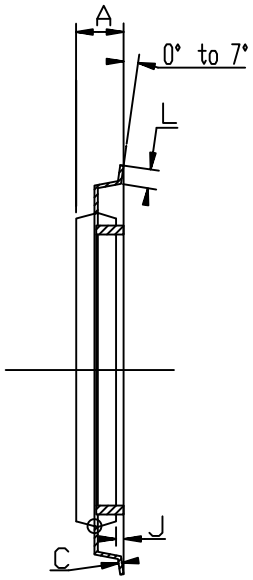


Table 5-1. VFBGA Package Dimensions

		Symbol	Common Dimensions (mm)
Package:			VFBGA
Body Size:	X	E	7.000 ± 0.100
	Y	D	7.000 ± 0.100
Ball Pitch:	X	eE	0.650
	Y	eD	0.650
Total Thickness:		A	1.000 max
Mold Thickness:		M	0.450 ref.
Substrate Thickness:		S	0.210 ref.
Ball Diameter:			0.300
Stand Off:		A1	0.160 ~ 0.260
Ball Width:		b	0.270 ~ 0.370
Package Edge Tolerance:		aaa	0.100
Mold Flatness:		bbb	0.100
Coplanarity:		ddd	0.080
Ball Offset (Package):		eee	0.150
Ball Offset (Ball):		fff	0.080
Ball Count:		n	100
Edge Ball Center to Center:	X	E1	5.850
	Y	D1	5.850
Corner Ball Center to Package Edge:	X	I	0.575
	Y	J	0.575

Figure 5-4. 64-lead LQFP Package Mechanical Drawing





COMMON DIMENSIONS IN MM

SYMBOL	Min	Max	NOTES
A	----	1.20	
A1	0.95	1.05	
C	0.09	0.20	
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
J	0.05	0.15	
L	0.45	0.75	
e	0.80 BSC		
f	0.30	0.45	

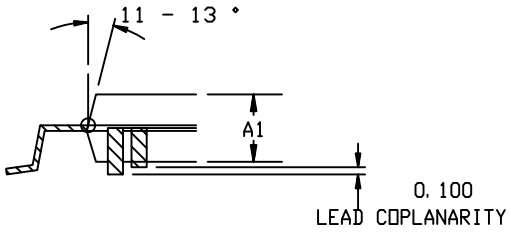
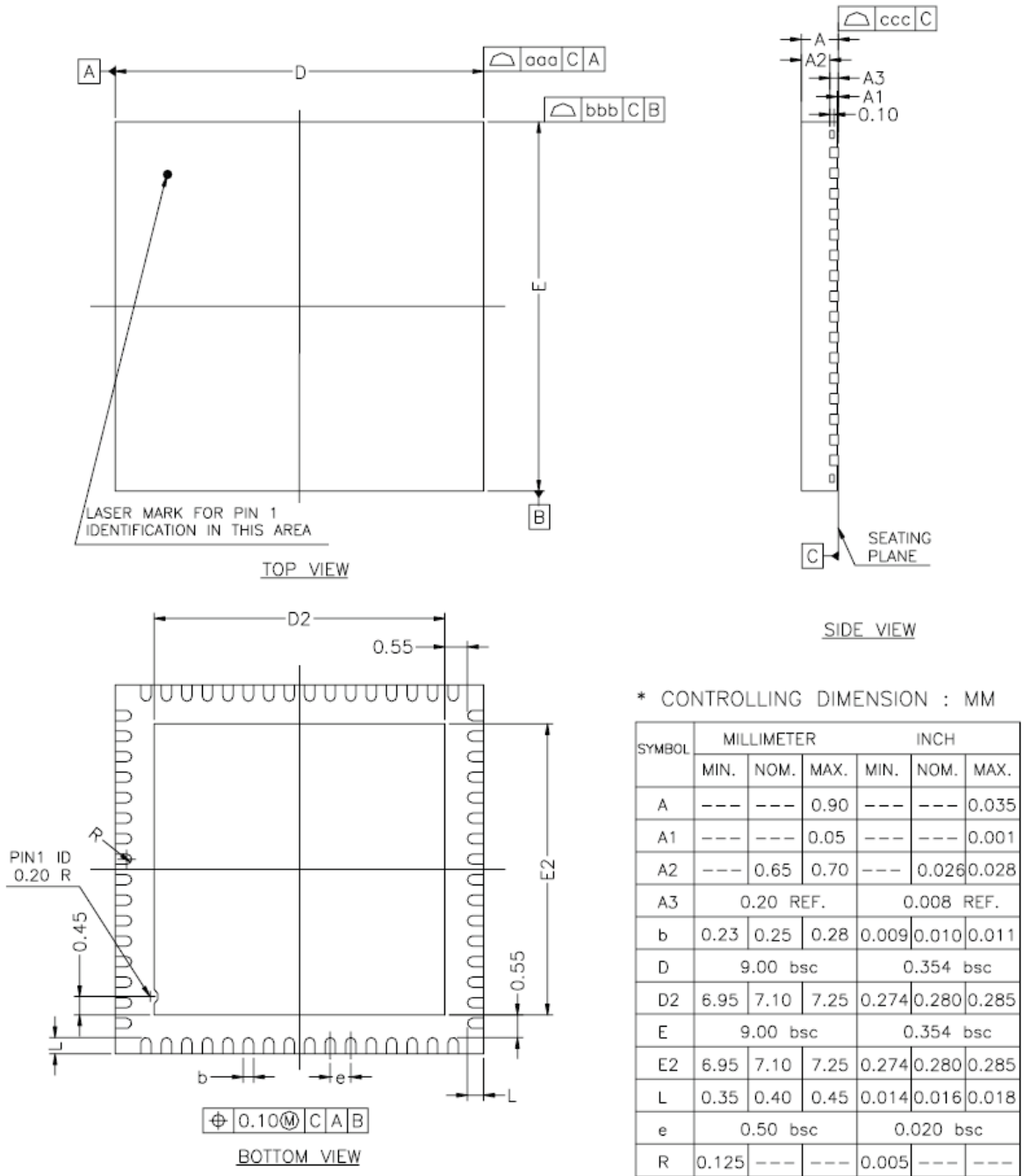


Figure 5-5. 64-lead QFN Package Mechanical Drawing



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.90	---	---	0.035
A1	---	---	0.05	---	---	0.001
A2	---	0.65	0.70	---	0.026	0.028
A3	0.20 REF.			0.008 REF.		
b	0.23	0.25	0.28	0.009	0.010	0.011
D	9.00 bsc			0.354 bsc		
D2	6.95	7.10	7.25	0.274	0.280	0.285
E	9.00 bsc			0.354 bsc		
E2	6.95	7.10	7.25	0.274	0.280	0.285
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.50 bsc			0.020 bsc		
R	0.125	---	---	0.005	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

6. Ordering Information

Table 6-1. Ordering Codes for SAM4S Devices

Ordering Code	MRL	Flash (Kbytes)	Package	Package Type	Temperature Operating Range
ATSAM4SD32CA-CU	A	2*1024	TFBGA100	Green	Industrial (-40°C to +85°C)
ATSAM4SD32CA-CFU	A	2*1024	VFBGA100	Green	Industrial (-40°C to +85°C)
ATSAM4SD32CA-AU	A	2*1024	LQFP100	Green	Industrial (-40°C to +85°C)
ATSAM4SD32BA-MU	A	2*1024	QFN64	Green	Industrial (-40°C to +85°C)
ATSAM4SD32BA-AU	A	2*1024	LQFP64	Green	Industrial (-40°C to +85°C)
ATSAM4SD16CA-CU	A	2*512	TFBGA100	Green	Industrial (-40°C to +85°C)
ATSAM4SD16CA-CFU	A	2*512	VFBGA100	Green	Industrial (-40°C to +85°C)
ATSAM4SD16CA-AU	A	2*512	LQFP100	Green	Industrial (-40°C to +85°C)
ATSAM4SD16BA-MU	A	2*512	QFN64	Green	Industrial (-40°C to +85°C)
ATSAM4SD16BA-AU	A	2*512	LQFP64	Green	Industrial (-40°C to +85°C)
ATSAM4SA16CA-CU	A	1024	TFBGA100	Green	Industrial (-40°C to +85°C)
ATSAM4SA16CA-CFU	A	1024	VFBGA100	Green	Industrial (-40°C to +85°C)
ATSAM4SA16CA-AU	A	1024	LQFP100	Green	Industrial (-40°C to +85°C)
ATSAM4SA16BA-MU	A	1024	QFN64	Green	Industrial (-40°C to +85°C)
ATSAM4SA16BA-AU	A	1024	LQFP64	Green	Industrial (-40°C to +85°C)
ATSAM4S16CA-CU	A	1024	TFBGA100	Green	Industrial (-40°C to +85°C)
ATSAM4S16CA-CFU	A	1024	VFBGA100	Green	Industrial (-40°C to +85°C)
ATSAM4S16CA-AU	A	1024	LQFP100	Green	Industrial (-40°C to +85°C)
ATSAM4S16BA-MU	A	1024	QFN64	Green	Industrial (-40°C to +85°C)
ATSAM4S16BA-AU	A	1024	LQFP64	Green	Industrial (-40°C to +85°C)

Table 6-1. Ordering Codes for SAM4S Devices

Ordering Code	MRL	Flash (Kbytes)	Package	Package Type	Temperature Operating Range
ATSAM4S8CA-CU	A	512	TFBGA100	Green	Industrial (-40°C to +85°C)
ATSAM4S8CA-CFU	A	512	VFBGA100	Green	Industrial (-40°C to +85°C)
ATSAM4S8CA-AU	A	512	LQFP100	Green	Industrial (-40°C to +85°C)
ATSAM4S8BA-MU	A	512	QFN64	Green	Industrial (-40°C to +85°C)
ATSAM4S8BA-AU	A	512	LQFP64	Green	Industrial (-40°C to +85°C)

Revision History

In the table that follows, the most recent version of the document appears first.

“rfo” indicates changes requested during document review and approval loop.

Doc. Rev 11100CS	Comments	Change Request Ref.
	In Section 2. “Block Diagram”, USB linked to Peripheral Bridge instead of AHB Bus Matrix in Figure 2-1, Figure 2-2, Figure 2-3 and Figure 2-4.	8386
	WKUP[15:0] pins added on each block diagram in Section 2. “Block Diagram” and in Table 3-1, “Signal Description List,”.	8459
	All diagrams updated with Real Time Events in Section 2. “Block Diagram”.	8484
	QFN64 package drawing and table updated in Figure 4-5, "Orientation of the 64-lead QFN Package".	8529
	In accordance with new Summary Datasheets template, deleted the following chapters: 5 Power Considerations, 6 Input/Output Lines, 7 Processor and Architecture, 8 Product Mapping, 9 Memories, 10 System Controller, 11 Embedded Peripherals Overview.	rfo
	Added 32 kHz trimming features in Section 1. “Features”.	
	ARMPowered® logo replaced with ARMConnected® logo in backpage, corresponding text updated.	

Doc. Rev 11100BS	Comments	Change Request Ref.
	48-pin package references removed from Section “Description”, Section 1. “Description”, Section 1.1 “Configuration Summary” (updated Table 1-1), Section 2. “Block Diagram” (deleted Fig. 2-3), Section 4. “Package and Pinout” (deleted the entire section 4.3 SAM4S16/S8A Package and Pinout), Section 10.13 “Chip Identification” (updated Table 10-1), Section 10.14 “PIO Controllers” (updated Table 10-2), Section 10.16 “Peripheral Signal Multiplexing on I/O Lines”, Section 5. “Package Drawings” (deleted Fig. 12-5 and Fig. 12-6).	8099
	VFBGA100 package information added to Section “Description”, Section 1.1 “Configuration Summary” (updated Table 1-1), and Section 4.1 “SAM4SD32/SD16/SA16/S16/S8C Package and Pinout” (added Figure 4-3 and Table 4-3).	rfo
	References to WFE instructions replaced by relevant bits precise descriptions in Section 5.5 “Low-Power Modes”.	
	SRAM upper address changed to 0x20400000 in Figure 8-1 on page 32.	
	New devices features added in Section 9.1.1 “Internal SRAM”Section 9.1.3.1 “Flash Overview”,Section 9.1.3.4 “Lock Regions”, Section 9.1.3.5 “Security Bit Feature”, Section 9.1.3.11 “GPNVM Bits”, and Table 10-1 on page 46.	
	Note added in Section 9.1.3.1 “Flash Overview”.	
	Table 10-3 updated in Section 10.15 “Peripheral Identifiers”.	
	Dual bank and cache memory references added to Section “Description” and Section 1. “Description”.	rfo
	Deleted LFBGA references from Section “Description” and Section 1. “Description” (updated Table 1-1).	rfo
	Section 2. “Block Diagram”: added references to SAM4S16/S8 and SAM4SD16/SA16 in the figure titles, updated Figure 2-3 for colors, and added Figure 2-4, "SAM4SD32/SD16/SA16 64-pin Version Block Diagram".	
	Section 5. “Package Drawings”: updated the introduction text and added Figure 5-3, "100-ball VFBGA Package Mechanical Drawing".	
	Section 6. “Ordering Information”: updated the headings row and added new rows with the SAM4SD32/SD16/A16/16/8 features in Table 6-1.	
	Consumption data updated in Section “Description”, Section 5.2 “Voltage Regulator”, Section 5.5.1 “Backup Mode”, Section 5.5.2 “Wait Mode”, and in Section 5.5.4 “Low Power Mode Summary Table”(Table 5-1 and the corresponding footnotes).	rfo
	Added 2 KB cache information in Figure 2-3, "SAM4SD32/SD16/SA16 100-pin Version Block Diagram" and Figure 2-4, "SAM4SD32/SD16/SA16 64-pin Version Block Diagram".	rfo
	Changed the temperature operating range (+105°C replaced with +85°C) in Section 6. “Ordering Information”.	
	Section 6.1 “General Purpose I/O Lines”, updated electrical characteristics for I/O lines.	rfo
	Section 9.1.3.1 “Flash Overview”, added Internal Flash addresses in the description of Flash size (Figure 9-3).	
	Section 9.1.3.11 “GPNVM Bits”, updated bits information (SAM4S16/SA16 and SAM4S8).	
	Deleted the entire section 10.14 UART.	
	Section 10.15 “Peripheral Identifiers”, updated information for EEFC0 and EEFC1 in Table 10-3 on page 47.	
	Section “Description”, added “Write Protected Registers” to the Peripherals list.	8213
	Section 2. “Block Diagram”, replaced “Time Counter B” by “Time Counter A” in Figure 2-1 on page 4.	rfo
	Specified the preliminary status of the datasheet.	rfo

Doc. Rev 11100AS	Comments	Change Request Ref.
	Initial release.	

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