

Errata

- Releasing Reset Condition without Clock
- Clearing Lockbits at High V_{CC} or Temperature
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7. Releasing Reset Condition without Clock

If an external reset or a watchdog reset occurs while the clock is stopped and the reset is released before the clock is restarted, the internal reset will time out after the start-up delay, which is independent of the external clock. If no external clock pulses are present in the period when internal reset is active, the reset does correctly causes tri-stating of the I/O while the reset is held. However, if the internal reset is released before the clock starts running, the part does not clear its I/O registers, nor sets PC to 0x00. Here, stopping the clock refers to gating the external clock input. Power-down mode does not have this issue.

Problem Fix/Workaround

Make sure the clock is running whenever an external reset can be expected. If the watchdog is used, never stop an external clock.

6. Clearing Lockbits at High V_{CC} or Temperature

If the temperature is too high, and/or the programming voltage is too high, the clearing of lockbits might fail.

Problem Fix/Workaround

Keep V_{CC} below 5.0 volts at room temperature when performing a chip erase.

5. Wrong Clearing of XTRF in MCUSR

The XTRF flag in MCUSR will be cleared when clearing the PORF flag. The flag does not get cleared by writing a "0" to it.

Problem Fix/Workaround

Finish the test of both flags before clearing any of them. Clear both flags simultaneously by writing 0 to both PORF and XTRF in MCUCR.

4. Reset during EEPROM Write

If reset is activated during EEPROM write, the result is not what should be expected. The EEPROM write cycle completes as normal, but the address registers are reset to 0. The result is that both the address written and address 0 in the EEPROM can be corrupted.

Problem Fix/Workaround

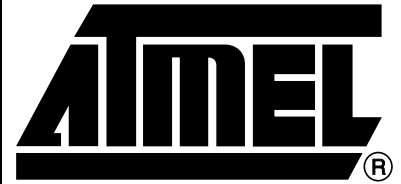
Avoid using address 0 for storage, unless you can guarantee that you will not get a reset during EEPROM write.

3. Serial Programming at Voltages below 3.0 Volts

At voltages below 3.0 volts, serial programming might fail.

Problem Fix/Workaround

Keep V_{CC} at 3.0 volts or higher during in-system programming.



8-bit **AVR**[®]
Microcontroller
with 2K Bytes of
In-System
Programmable
Flash

AT90S/LS2343
Rev. F
Errata Sheet

Rev. 1193D-09/01





2. High I_{CC} in Power-down with External Clock Running

When the external clock is running while the device is in power down, the power consumption will be higher than specified.

Problem Fix/Workaround

Stop the external clock while the device is in Power-down.

1. Wrong Latching of RCEN Fuse

If V_{CC} goes below GND and then up to the operating voltage, the RCEN fuse can be read as unprogrammed even if it is programmed. The result of this is that the device starts looking for a clock signal on the external clock input instead of from the internal RC oscillator, making it look as if it "hangs".

Problem Fix/Workaround

This issue has been resolved in Rev. G of the AT90S/LS2343.



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