#### **Features**

- Programmable 4,194,304 x 1 and 8,388,608 x 1-bit Serial Memories Designed to Store Configuration Programs for Field Programmable Gate Arrays (FPGAs)
- 3.3V Output Capability
- 5V Tolerant I/O Pins
- Program Support using the Atmel ATDH2200E System or Industry Third-party Programmers
- In-System Programmable (ISP) via 2-wire Bus
- Simple Interface to SRAM FPGAs
- Compatible with Atmel AT40K and AT94K Devices, Altera<sup>®</sup> FLEX<sup>®</sup>, APEX<sup>™</sup> Devices, Lucent<sup>®</sup> ORCA<sup>®</sup> FPGAs, Xilinx<sup>®</sup> XC3000, XC4000, XC5200, Spartan<sup>®</sup>, Virtex<sup>®</sup> FPGAs, Motorola<sup>®</sup> MPA1000 FPGAs
- Cascadable Read-back to Support Additional Configurations or Higher-density Arrays
- Low-power CMOS FLASH Process
- Available in 6 mm x 6 mm x 1 mm 8-lead LAP (Pin-compatible with 8-lead SOIC/VOIC Packages), 20-lead PLCC and 44-lead TQFP Packages
- Emulation of Atmel's AT24CXXX Serial EEPROMs
- Low-power Standby Mode
- Single Device Capable of Holding 4-bit Stream Files Allowing Simple System Reconfiguration
- Fast Serial Download Speeds up to 33 MHz
- Endurance: 5,000 Write Cycles Typical
- Green (Pb/Halide-free/RoHS Compliant) Package Options Available

### 1. Description

The AT17F Series of In-System Programmable Configuration PROMs (Configurators) provide an easy-to-use, cost-effective configuration memory for Field Programmable Gate Arrays. The AT17F Series device is packaged in the 8-lead LAP, 20-lead PLCC, and 44-lead TQFP, see Table 1-1. The AT17F Series Configurator uses a simple serial-access procedure to configure one or more FPGA devices.

The AT17F Series Configurators can be programmed with industry-standard programmers, Atmel's ATDH2200E Programming Kit or Atmel's ATDH2225 ISP Cable.

Table 1-1. AT17F Series Packages

Package	AT17F040	AT17F080
8-lead LAP	Yes	Yes
20-lead PLCC	Yes	Yes
44-lead TQFP	-	Yes



# FPGA Configuration Flash Memory

AT17F040 AT17F080

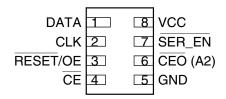




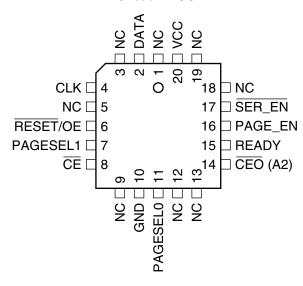


## 2. Pin Configuration

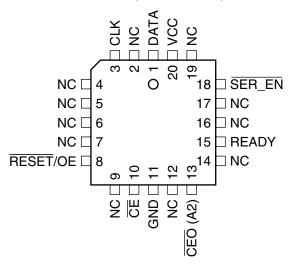
#### 8-lead LAP



#### 20-lead PLCC

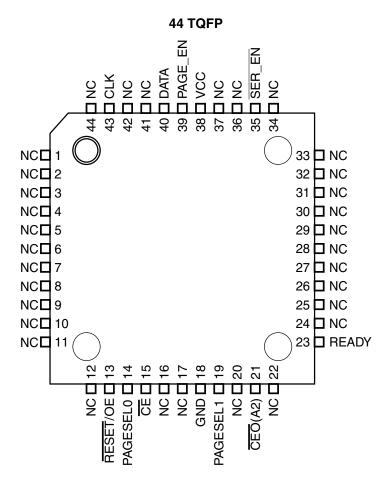


#### 20-lead PLCC (Virtex Pinout)(1)(2)



Notes: 1. 20-lead PLCC (Virtex pinout) is only available in the AT17F040.

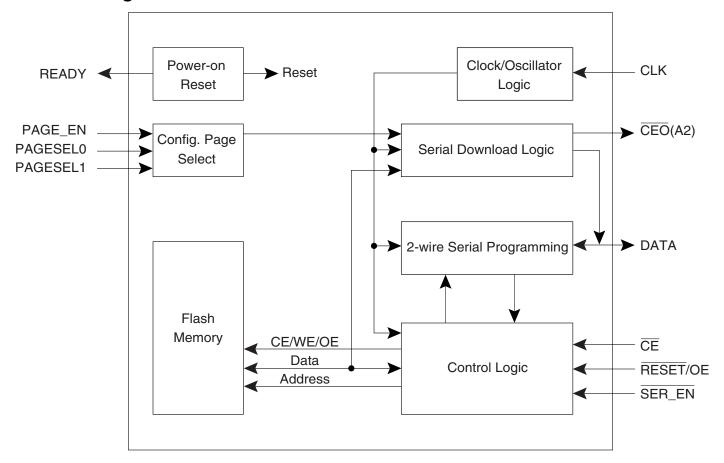
2. Virtex pinout is compatible with the XC17V and XC18V Series PROM.







### 3. Block Diagram



### 4. Device Description

The control signals for the configuration memory device ( $\overline{\text{CE}}$ ,  $\overline{\text{RESET}}/\text{OE}$  and CLK) interface directly with the FPGA device control signals. All FPGA devices can control the entire configuration process and retrieve data from the configuration device without requiring an external intelligent controller.

The  $\overline{\text{RESET}}/\text{OE}$  and  $\overline{\text{CE}}$  pins control the tri-state buffer on the DATA output pin and enable the address counter. When  $\overline{\text{RESET}}/\text{OE}$  is driven Low, the configuration device resets its address counter and tri-states its DATA pin. The  $\overline{\text{CE}}$  pin also controls the output of the AT17F Series Configurator. If  $\overline{\text{CE}}$  is held High after the  $\overline{\text{RESET}}/\text{OE}$  reset pulse, the counter is disabled and the DATA output pin is tri-stated. When  $\overline{\text{NESET}}/\text{OE}$  is driven Low again, the address counter is reset and the DATA output pin is tri-stated, regardless of the state of  $\overline{\text{CE}}$ .

When the configurator has driven out all of its data and  $\overline{\text{CEO}}$  is driven Low, the device tri-states the DATA pin to avoid contention with other configurators. Upon power-up, the address counter is automatically reset.

### 5. Pin Description

Table 5-1. Pin Description

			AT17F040			AT17F080	
Name	I/O	8 LAP	20 PLCC	20 PLCC (Virtex)	8 LAP	20 PLCC	44 TQFP
DATA	I/O	1	2	1	1	2	40
CLK	I	2	4	3	2	4	43
PAGE_EN	ı	_	16	_	_	16	39
PAGESEL0	1	_	11	_	_	11	14
PAGESEL1	I	_	7	_	_	7	19
RESET/OE	ı	3	6	8	3	6	13
CE	1	4	8	10	4	8	15
GND	_	5	10	11	5	10	18
CEO	0	0	4.4	10	0	4.4	0.4
A2	1	6	14	13	6	14	21
READY	0	_	15	15	_	15	23
SER_EN	1	7	17	18	7	17	35
V <sub>CC</sub>	_	8	20	20	8	20	38

### 5.1 DATA<sup>(1)</sup>

Three-state DATA output for configuration. Open-collector bi-directional pin for programming.

#### 5.2 CLK<sup>(1)</sup>

Clock input. Used to increment the internal address and bit counter for reading and programming.

### 5.3 **PAGE\_EN**<sup>(2)</sup>

Input used to enable page download mode. When PAGE\_EN is high the configuration download address space is partitioned into 4 equal pages. This gives users the ability to easily store and retrieve multiple configuration bitstreams from a single configuration device. This input works in conjunction with the PAGESEL inputs. PAGE\_EN must be remain low if paging is not desired. When \$\overline{\text{SER}\_EN}\$ is Low (ISP mode) this pin has no effect.

Notes: 1. This pin has an internal 20  $K\Omega$  pull-up resistor.

2. This pin has an internal 30 K $\Omega$  pull-down resistor.





### 5.4 PAGESEL[1:0]<sup>(2)</sup>

Page select inputs. Used to determine which of the 4 memory pages are targeted during a serial configuration download. The address space for each of the pages is shown in Table 5-2. When SER EN is Low (ISP mode) these pins have no effect.

Table 5-2.Address Space

Paging Decodes	AT17F040 (4 Mbits)	AT17F080 (8 Mbits)
PAGESEL = 00, PAGE_EN = 1	00000 – 0FFFFh	00000 – 1FFFFh
PAGESEL = 01, PAGE_EN = 1	10000 – 1FFFFh	20000 – 3FFFFh
PAGESEL = 10, PAGE_EN = 1	20000 – 2FFFFh	40000 – 5FFFFh
PAGESEL = 11, PAGE_EN = 1	30000 – 3FFFFh	60000 – 7FFFFh
PAGESEL = XX, PAGE_EN = 0	00000 – 3FFFFh	00000 – 7FFFFh

### $\overline{RESET}/OE^{(1)}$

Output Enable (active High) and RESET (active Low) when SER\_EN is High. A Low level on RESET/OE resets both the address and bit counters. A High level (with  $\overline{\text{CE}}$  Low) enables the data output driver.

#### $5.6 \quad \overline{CE}^{(1)}$

Chip Enable input (active Low). A Low level (with OE High) allows CLK to increment the address counter and enables the data output driver. A High level on  $\overline{\text{CE}}$  disables both the address and bit counters and forces the device into a low-power standby mode. Note that this pin will *not* enable/disable the device in the 2-wire Serial Programming mode ( $\overline{\text{SER}}_{-}\overline{\text{EN}}$  Low).

#### 5.7 **GND**

Ground pin. A 0.2  $\mu$ F decoupling capacitor between  $V_{CC}$  and GND is recommended.

#### 5.8 **CEO**

Chip Enable Output (when  $\overline{SER}_{\overline{EN}}$  is High). This output goes Low when the internal address counter has reached its maximum value. If the PAGE\_EN input is set High, the maximum value is the highest address in the selected partition. The PAGESEL[1:0] inputs are used to make the 4 partition selections. If the PAGE\_EN input is set Low, the device is not partitioned and the address maximum value is the highest address in the device, see Table 5-2 on page 6. In a daisy chain of AT17F Series devices, the  $\overline{CEO}$  pin of one device must be connected to the  $\overline{CE}$  input of the next device in the chain. It will stay Low as long as  $\overline{CE}$  is Low and OE is High. It will then follow  $\overline{CE}$  until OE goes Low; thereafter,  $\overline{CEO}$  will stay High until the entire EEPROM is read again.

Notes: 1. This pin has an internal 20  $k\Omega$  pull-up resistor.

2. This pin has an internal 30 k $\Omega$  pull-down resistor.

### 5.9 A2<sup>(1)</sup>

Device selection input, (when  $\overline{SER\_EN}$  Low). The input is used to enable (or chip select) the device during programming (i.e., when  $\overline{SER\_EN}$  is Low). Refer to the AT17F Programming Specification available on the Atmel web site for additional details.

#### **5.10 READY**

Open collector reset state indicator. Driven Low during power-up reset, released when power-up is complete. (recommended 4.7 k $\Omega$  pull-up on this pin if used).

### 5.11 **SER\_EN**<sup>(1)</sup>

The serial enable input must remain High during FPGA configuration operations. Bringing  $\overline{SER\_EN}$  Low enables the 2-Wire Serial Programming Mode. For non-ISP applications,  $\overline{SER\_EN}$  should be tied to  $V_{CC}$ .

### 5.12 V<sub>CC</sub>

+3.3V (±10%).

Notes: 1. This pin has an internal 20  $k\Omega$  pull-up resistor.

2. This pin has an internal 30 k $\Omega$  pull-down resistor.





### 6. FPGA Master Serial Mode Summary

The I/O and logic functions of any SRAM-based FPGA are established by a configuration program. The program is loaded either automatically upon power-up, or on command, depending on the state of the FPGA mode pins. In Master mode, the FPGA automatically loads the configuration program from an external memory. The AT17F Serial Configuration PROM has been designed for compatibility with the Master Serial mode.

This document discusses the Atmel AT40K, AT40KAL and AT94KAL applications as well as Xilinx applications.

## 7. Control of Configuration

Most connections between the FPGA device and the AT17F Serial Configurator PROM are simple and self-explanatory.

- The DATA output of the AT17F Series Configurator drives DIN of the FPGA devices.
- The master FPGA CCLK output drives the CLK input of the AT17F Series Configurator.
- The  $\overline{\text{CEO}}$  output of any AT17F Series Configurator drives the  $\overline{\text{CE}}$  input of the next Configurator in a cascade chain of configurator devices.
- SER\_EN must be connected to V<sub>CC</sub> (except during ISP).
- The READY pin is available as an open-collector indicator of the device's reset status; it is driven Low while the device is in its power-on reset cycle and released (tri-stated) when the cycle is complete.
- PAGE\_EN must be held Low if download paging is not desired. The PAGESEL[1:0] inputs
  must be tied off High or Low. If paging is desired, PAGE\_EN must be High and the PAGESEL
  pins must be set to High or Low such that the desired page is selected, see Table 5-2 on
  page 6.

## 8. Cascading Serial Configuration Devices

For multiple FPGAs configured as a daisy-chain, or for FPGAs requiring larger configuration memories, cascaded configurators provide additional memory.

After the last bit from the first configurator is read, the clock signal to the configurator asserts its  $\overline{\text{CEO}}$  output Low and disables its DATA line driver. The second configurator recognizes the Low level on its  $\overline{\text{CE}}$  input and enables its DATA output.

After configuration is complete, the address counters of all cascaded configurators are reset if the RESET/OE on each configurator is driven to its active (Low) level.

If the address counters are not to be reset upon completion, then the RESET/OE input can be tied to its inactive (High) level.

## 9. Programming Mode

8

The programming mode is entered by bringing  $\overline{SER}_{EN}$  Low. In this mode the chip can be programmed by the 2-wire serial bus. The programming is done at  $V_{CC}$  supply only. Programming super voltages are generated inside the chip. The AT17F parts are read/write at 3.3V nominal. Refer to the AT17F Programming Specification available on the Atmel web site (www.atmel.com) for more programming details. AT17F devices are supported by the Atmel ATDH2200 programming system along with many third party programmers.

### 10. Standby Mode

The AT17F Series Configurators enter a low-power standby mode whenever SER\_EN is High and CE is asserted High. In this mode, the AT17F Configurator consumes less than 1 mA of current at 3.3V. The output remains in a high-impedance state regardless of the state of the OE input.

## 11. Absolute Maximum Ratings\*

Operating Temperature40° C to +85° C
Storage Temperature65 ° C to +150 ° C
Voltage on Any Pin with Respect to Ground0.1V to V <sub>CC</sub> +0.5V
Supply Voltage (V <sub>CC</sub> )0.5V to +4.0V
Maximum Soldering Temp. (10 sec. @ 1/16 in.) 260° C
ESD (R <sub>ZAP</sub> = 1.5K, C <sub>ZAP</sub> = 100 pF)2000V

\*NOTICE:

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

## 12. Operating Conditions

			AT17F Series		
Symbol	Description		Min	Max	Units
V	Commercial	Supply voltage relative to GND -0°C to +70°C	2.97	3.63	V
V <sub>cc</sub>	Industrial	Supply voltage relative to GND -40°C to +85°C	2.97	3.63	V

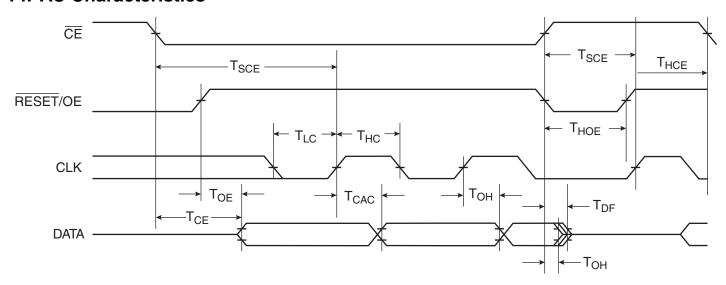
### 13. DC Characteristics

			AT17	7F040	AT17	'F080	
Symbol	Description		Min	Max	Min	Max	Units
V <sub>IH</sub>	High-level Input Voltage		2.0	V <sub>CC</sub>	2.0	V <sub>CC</sub>	V
V <sub>IL</sub>	Low-level Input Voltage		0	0.8	0	0.8	V
V <sub>OH</sub>	High-level Output Voltage (I <sub>OH</sub> = -2.5 mA)	Comerce	2.4		2.4		V
V <sub>OL</sub>	Low-level Output Voltage (I <sub>OL</sub> = +3 mA)	Commercial		0.4		0.4	V
V <sub>OH</sub>	High-level Output Voltage (I <sub>OH</sub> = -2 mA)	La di catalal	2.4		2.4		V
V <sub>OL</sub>	Low-level Output Voltage (I <sub>OL</sub> = +3 mA)	Industrial		0.4		0.4	V
I <sub>CCA</sub>	Supply Current, Active Mode			20		20	mA
IL	Input or Output Leakage Current ( $V_{IN} = V_{CC}$	or GND)	-10	10	-10	10	μA
Constant Comment Other discounts	Commercial		1		1	mA	
<sup>I</sup> CCS	I <sub>CCS</sub> Supply Current, Standby Mode Ind			1		1	mA

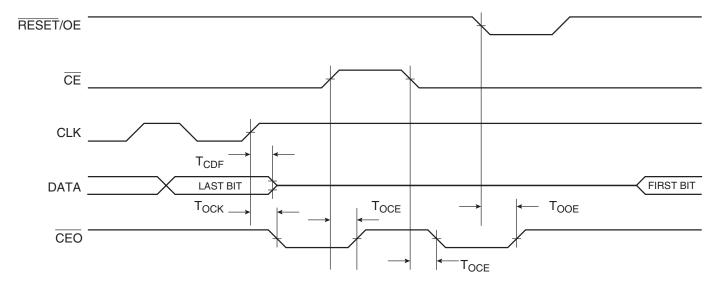




### 14. AC Characteristics



## 15. AC Characteristics when Cascading



## 16. AC Characteristics

				AT17F040/080		
Symbol	Description		Min		Max	Units
<b>T</b> (2)	OF to Data Data.	Commercial			50	ns
T <sub>OE</sub> <sup>(2)</sup>	OE to Data Delay	Industrial <sup>(1)</sup>			55	ns
<b>T</b> (2)	CE to Data Delay	Commercial			55	ns
T <sub>CE</sub> <sup>(2)</sup>	CE to Data Delay	Industrial <sup>(1)</sup>			60	ns
<b>T</b> (2)	CLK to Doto Dolov	Commercial	3		30	ns
T <sub>CAC</sub> <sup>(2)</sup>	CLK to Data Delay	Industrial <sup>(1)</sup>			30	ns
_	5	Commercial	0			ns
T <sub>OH</sub>	Data Hold from $\overline{CE}$ , OE, or CLK	Industrial <sup>(1)</sup>	0			ns
<b>T</b> (3)	OF or OF to Data Float Dalay	Commercial			15	ns
T <sub>DF</sub> <sup>(3)</sup>	CE or OE to Data Float Delay	Industrial <sup>(1)</sup>			15	ns
_	CLK Low Time	Commercial	15			ns
T <sub>LC</sub>	CLK Low Time	Industrial <sup>(1)</sup>	15			ns
_	OLK High Times	Commercial	15			ns
T <sub>HC</sub>	CLK High Time	Industrial <sup>(1)</sup>	15			ns
т	CE Setup Time to CLK	Commercial	20			ns
T <sub>SCE</sub>	(to guarantee proper counting)	Industrial <sup>(1)</sup>	25			ns
т	CE Hold Time from CLK	Commercial	0			ns
T <sub>HCE</sub>	(to guarantee proper counting)	Industrial <sup>(1)</sup>	0			ns
_	RESET/OE Low Time	Commercial	20			ns
T <sub>HOE</sub>	(guarantees counter is reset)	Industrial <sup>(1)</sup>	20			ns
_	Maximum Input Clock Frequency	Commercial			10	MHz
$F_{MAX}$	SEREN = 0	Industrial <sup>(1)</sup>			10	MHz
_	Maximum Input Clock Frequency	Commercial			33	MHz
F <sub>MAX</sub>	SEREN = 1	Industrial <sup>(1)</sup>			33	MHz
т	Write Cycle Time <sup>(4)</sup>	Commercial		12		μs
$T_{WR}$	write Cycle Time."	Industrial <sup>(1)</sup>		12		μs
т	From Cycle Time <sup>(4)</sup>	Commercial		13		S
T <sub>EC</sub>	Erase Cycle Time <sup>(4)</sup>	Industrial <sup>(1)</sup>		13		s

- Notes: 1. Preliminary specifications for military operating range only.
  - 2. AC test lead = 50 pF.
  - 3. Float delays are measured with 5 pF AC loads. Transition is measured  $\pm$  200 mV from steady-state active levels.
  - 4. See the AT17F Programming Specfication for procedural information.





## 16.1 AC Characteristics When Cascading

			AT17F040		AT17F080		
Symbol	Description		Min	Max	Min	Max	Units
<b>-</b> (3)	CLK to Data Float Daloy	Commercial		60		50	ns
T <sub>CDF</sub> <sup>(3)</sup>	CLK to Data Float Delay	Industrial		60		50	ns
<b>T</b> (2)	CLK to CEO Delay	Commercial		55		50	ns
T <sub>OCK</sub> <sup>(2)</sup>		Industrial		60		55	ns
<b>T</b> (2)	T <sub>OCE</sub> <sup>(2)</sup>	Commercial		55		35	ns
OCE		Industrial		60		40	ns
<b>T</b> (2)	DECETION to CEO Delay	Commercial		40		35	ns
T <sub>OOE</sub> <sup>(2)</sup>	RESET/OE to CEO Delay	Industrial		45		35	ns
_	Mariana Iran A Olaska Francisco	Commercial		33		33	MHz
F <sub>MAX</sub>	Maximum Input Clock Frequency	Industrial		33		33	MHz

Notes: 1. AC test lead = 50 pF.

<sup>2.</sup> Float delays are measured with 5 pF AC loads. Transition is measured  $\pm$  200 mV from steady-state active levels.

## 17. Thermal Resistance Coefficients

Package	Package Type		AT17F040	AT17F080
8CN4 Leadless Arrav Package (LAP)	θ <sub>JC</sub> [° C/W]		_	
OCIN4	Leadless Array Package (LAP)	θ <sub>JA</sub> [° C/W] <sup>(1)</sup>		-
00.1	Plactic Looded Chin Comics (PLCC)	θ <sub>JC</sub> [° C/W]		-
20J	Plastic Leaded Chip Carrier (PLCC)	θ <sub>JA</sub> [° C/W] <sup>(1)</sup>		-
444	This Plantic Ound Flat Parks as /TOFP	θ <sub>JC</sub> [° C/W]	_	17
44A	Thin Plastic Quad Flat Package (TQFP)		_	62

Note: 1. Airflow = 0 ft/min.





## 18. Ordering Information

Memory Size	Ordering Code	Package <sup>(1)(2)</sup>	Operation Range
4-Mbit	AT17F040-30VJC	20J - 20 PLCC	Commercial (0° C to 70° C)
4-IVIDIL	AT17F040-30VJI	20J - 20 PLCC	Industrial (-40° C to 85° C)
8-Mbit	AT17F080-30TQC	44A - 44 TQFP	Commercial (0° C to 70° C)
	AT17F080-30TQI	44A - 44 TQFP	Industrial (-40° C to 85° C)

Notes: 1. For the -30BJC and -30BJI packages, customers may migrate to the AT17F32-30BJU.

## 19. Green Package Options (Pb/Halide-free/RoHS Compliant)

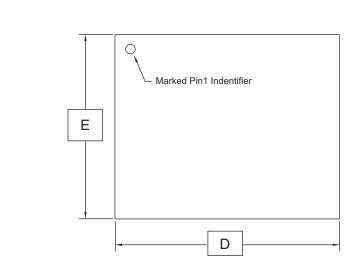
Memory Size	Ordering Code	Package	Operation Range
4-Mbit	AT17F040-30CU	8CN4 - 8 LAP	
	AT17F040-30JU	20J - 20 PLCC	Industrial
8-Mbit	AT17F080-30CU	8CN4 - 8 LAP	(-40° C to 85° C)
	AT17F080-30JU	20J - 20 PLCC	

	Package Type		
8CN4	8-lead, 6 mm x 6 mm x 1.04 mm, Leadless Array Package (LAP) – Pin-compatible with 8-lead SOIC/VOIC Packages		
20J	20-lead, Plastic J-leaded Chip Carrier (PLCC)		
44A	44-lead, Thin (1.0 mm) Plastic Quad Flat Package Carrier (TQFP)		

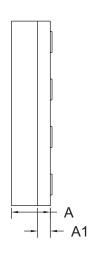
<sup>2.</sup> For the -30JC and -30JI packages, customers may migrate to the AT17Fxxx-30JU.

## 20. Packaging Information

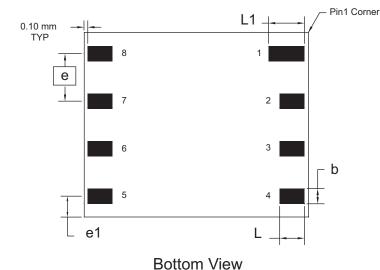
#### 20.1 8CN4 - LAP



Top View



Side View



Note: 1. Metal Pad Dimensions.

All exposed metal area shall have the following finished platings.
 Ni: 0.0005 to 0.015 mm
 Au: 0.0005 to 0.001 mm

COMMON DIMENSIONS (Unit of Measure = mm)

MIN	NOM	MAX	NOTE
0.94	1.04	1.14	
0.30	0.34	0.38	
0.45	0.50	0.55	1
5.89	5.99	6.09	
5.89	5.99	6.09	
	1.27 BSC		
1.10 REF			
0.95	1.00	1.05	1
1.25	1.30	1.35	1
	0.94 0.30 0.45 5.89 5.89	0.94 1.04 0.30 0.34 0.45 0.50 5.89 5.99 5.89 5.99 1.27 BSC 1.10 REF	0.94     1.04     1.14       0.30     0.34     0.38       0.45     0.50     0.55       5.89     5.99     6.09       5.89     5.99     6.09       1.27 BSC       1.10 REF       0.95     1.00     1.05

2/15/08



Package Drawing Contact: packagedrawings@atmel.com

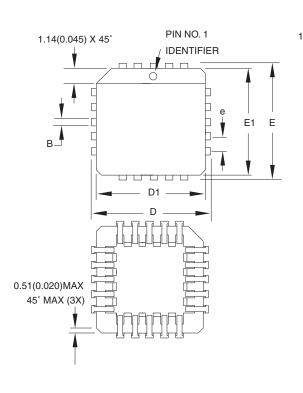
**TITLE 8CN4**, 8-lead (6 x 6 x 1.04 mm Body),
Lead Pitch 1.27mm,
Leadless Array Package (LAP)

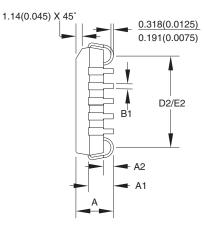
GPC	DRAWING NO.	REV.
DMH	8CN4	D





#### 20.2 20J - PLCC





## COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
Α	4.191	_	4.572	
A1	2.286	_	3.048	
A2	0.508	_	_	
D	9.779	_	10.033	
D1	8.890	_	9.042	Note 2
E	9.779	_	10.033	
E1	8.890	_	9.042	Note 2
D2/E2	7.366	_	8.382	
В	0.660	_	0.813	
B1	0.330	_	0.533	
е		1.270 TYF	)	

Notes:

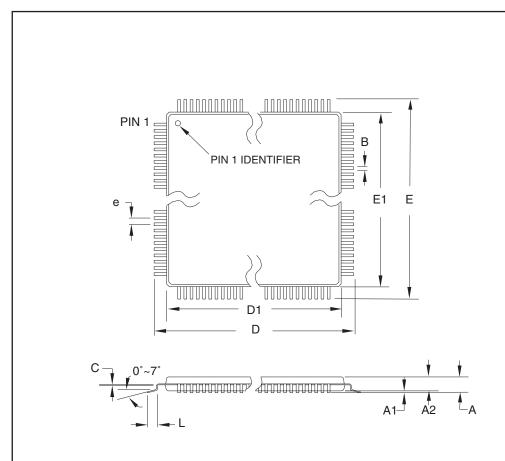
- 1. This package conforms to JEDEC reference MS-018, Variation AA.
- Dimensions D1 and E1 do not include mold protrusion.
   Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
- 3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

<u>AIMEL</u>	2325 Orchard Parkway		
	San Jose, CA 95131		

TITLE	DRAWING NO.	REV.
20J, 20-lead, Plastic J-leaded Chip Carrier (PLCC)	20J	В

#### 20.3 44A - TQFP



#### **COMMON DIMENSIONS**

(Unit of Measure = mm)

	,		· · ·	
SYMBOL	MIN	NOM	MAX	NOTE
Α	_	_	1.20	
A1	0.05	_	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
В	0.30	_	0.45	
С	0.09	_	0.20	
L	0.45	_	0.75	
е		0.80 TYP		

Notes:

- 1. This package conforms to JEDEC reference MS-026, Variation ACB.
- Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
- 3. Lead coplanarity is 0.10 mm maximum.

10/5/2001



2325 Orchard Parkway San Jose, CA 95131 TITLE

 $\textbf{44A,} \ \, \textbf{44-lead}, \ \, \textbf{10 x 10 mm Body Size}, \ \, \textbf{1.0 mm Body Thickness}, \\ \textbf{0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)}$ 

DRAWING NO.	REV.
44A	В





## 21. Revision History

Revision Level – Release Date	History
J – March 2006	Added last-time buy for AT17FXXX-30CC and AT17FXXX-30Cl.
K – February 2008	Removed -30JC, -30JI, -30BJC and -30BJI devices from ordering information.



#### Headquarters

Atmel Corporation

2325 Orchard Parkway San Jose, CA 95131 USA

Tel: 1(408) 441-0311 Fax: 1(408) 487-2600

#### International

Atmel Asia

Room 1219 Chinachem Golden Plaza 77 Mody Road Tsimshatsui East Kowloon Hong Kong

Tel: (852) 2721-9778 Fax: (852) 2722-1369 Atmel Europe

Le Krebs 8, Rue Jean-Pierre Timbaud BP 309 78054 Saint-Quentin-en-Yvelines Cedex

France Tel: (33) 1-30-60-70-00

Fax: (33) 1-30-60-71-11

Atmel Japan

9F, Tonetsu Shinkawa Bldg. 1-24-8 Shinkawa Chuo-ku, Tokyo 104-0033 Japan

Tel: (81) 3-3523-3551 Fax: (81) 3-3523-7581

#### **Product Contact**

Web Site

as components in applications intended to support or sustain life.

www.atmel.com

Technical Support

configurator@atmel.com

Sales Contact

www.atmel.com/contacts

Literature Requests www.atmel.com/literature

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