

Active Errata List

- During UART Reception, Clearing REN May Generate Unexpected IT
- Internal Resistor on Reset Pin
- SPI – SPI SS Pin Limitation on Master/Slave
- SPI – SPI Slave Responding in a Multislave Configuration When Not Selected by the Master and its SPDAT Register is Loaded
- SPI – SPI Slave Does Not Respond When Selected and Not Loaded
- ALE Disabled Toggles During Internal MOVX
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- Timer 2 – Baud Rate Generator – Long Start Time
- EEPROM Read After Write
- SPI Slave Mode/Data Corrupted

Errata History

Lot Number	Errata List
00635 and Below	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Above 00635	1, 2, 3, 4, 5, 6, 7, 8, 9, 10

Errata Description

1. During UART Reception, Clearing REN may Generate Unexpected IT

During UART reception, if the REN bit is cleared between start bit detection and the end of reception, the UART will not discard the data (RI is set).

Workaround

Test REN at the beginning of an Interrupt routine just after CLR RI, and run the Interrupt routine code only if REN is set.

2. Internal Resistor on Reset Pin

Deviation from electrical specification. Typical value for internal resistor on Reset pin: 20 kΩ.

Workaround

None.

3. SPI – SPI SS Pin Limitation on Master/Slave

The SS pin of the SPI does not get back to I/O when a One-to-One Master/Slave intercommunication is performed.

Workaround

None.

4. SPI – SPI Slave Responding in a Multislave Configuration When Not Selected by the Master and its SPDAT Register is Loaded

In a multislave configuration, if the master is sending the Sck and the Tx data to all the slaves, and only one slave is selected, the non-selected slaves respond and generate the end of the transmission interruption (SPIF) if their SPDAT registers are loaded before the transmission.

Workaround

None.



80C51 MCUs

T89C51RB2

T89C51RC2

Errata Sheet

Rev. 4100B-8051-05/02



5. SPI – SPI Slave Does Not Respond when Selected and not Loaded

SPI Slave does not respond when selected by a Master and no Data is loaded to be transmitted. No Rx data is registered and no SPIF interruption is generated at the end of the Transmission.

Workaround

None.

6. ALE Disabled Toggles During Internal MOVX

When ALE is disabled, internal MOVX instruction shows toggle of ALE.

Workaround

None.

7. Timer 2 – Baud Rate Generator – No IT when TF2 is Set by Software

When Timer 2 is used in baud rate generator mode, setting TF2 by software does not generate an interrupt.

Workaround

Use Timer 1 instead of Timer 2 to generate baud rate and interrupt.

8. Timer 2 – Baud Rate Generator – Long Start Time

When Timer 2 is used as a baud rate generator, TH2 is not loaded with RCAP2H at the beginning, then UART is not operational before 10000 machine cycles.

Workaround

Add the initialization of TH2 and TL2 in the initialization of Timer 2.

9. EEPROM Read After Write

The first read access on EEPROM just after a write command is disturbed.

Workaround

Do not load more than 16 bytes at a time.

10. SPI Slave Mode/Data Corrupted

When SPI macro is configured in slave reception mode, the SPI block does not handle the correct data on the SPI bus.

Workaround

None.

11. RB8 Lost with JBC on SCON

On C51, when using JBC instruction on any bit of SCON register, if RB8 bit changes from "1" to "0" during JBC the "0" is lost and RB8 keeps "1".

Workaround

In a polling algorithm, clear RB8 at the beginning of the code and after each time it goes to "1".

In interrupt, RB8 must be cleared at the beginning of the code and after each time it goes to "1".



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