Errata Sheet

TS80C51U2/TS87C51U2/TS83C51U2

This errata sheet describes the functional deviations known at the release date of this document.

Errata History

TS87C51U2

Lot Number	Trouble list	Status
All	T01, T02, T03, T04, T05, T06, T08, T09	Not Fixed

TS80C51U2-TS83C51U2

Lot Number	Trouble list	Status
All	T01, T02, T03, T04, T05, T06, T07, T08, T09	Not Fixed

Trouble descriptions

T01	Baud Rate Generator clock
Description:	In idle mode, the baud rate generator clock is off
Workaround:	Use Timer1 or Timer 2 to generate baud rate when idle mode is required.

T02	Port/level/read at 0 after reset vs External pull-down
Description:	After Reset, if the External pull-down connected to the port is too low, the Port is read at 0 level.
Workaround:	The external pull-down connected during Reset must be larger than (90Kohm if Medium pull-up=300Kohm @Vcc=5V)

T03	UART / Reception in modes 1, 2 and 3 / UART false start bits detection
Description:	When a false start bit occurs on the UART, some UART internal signals are not reset. Than when a real start bit occurs, the sampling is shifted.
Workaround:	No

T04	During UART reception, clearing REN may generate unexpected IT.
Description:	During UART reception, if the REN bit is clear between a start bit detection and the end of reception, the UART will not discard the data (RI is set).
Workaround:	Test REN at the beginning of Interrupt routine just after CLR RI, and to run the Interrupt routine code only if REN is set.

T05	JBC / Double IT when external Interrupt occurs during JBC instruction
Description:	On polling algorithm in ISR on IE1 or IE0 bit, when external IT appears during JBC instruction , flag is not cleared and next JBC sees another IT, then the same IT is seen twice.
Workaround:	Use JB Instruction instead of JBC instruction to test bit and CLR instruction to clear it.

T06	Timer2 / Downcounter mode / Double IT with slow ext. clock
Description:	Double IT with slow external clock in down-count mode.Timer 2 in 16 bit auto-reload in count down mode with external clock input 2 interrupts are generated successively with low frequency on clock input (typ 10-40KHz).
Workaround:	Reload FFFE into TH2-TL2 in ISR and count down to RCAP-1 (to recover cycle lost in ISR) Caution : does not work if initially RCAP = 0x0000

T07	Static Consumption EAVPP - ROM Only
Description:	In ROM process, EAVPP in not used and grounded by metal . When entering in power-down mode, a conflict occurs because an internal pull-up is connected to pad. Consumption is about 16µA in ROM process
Workaround:	No

T08	Input Trigger Consumption / All C51 type I/O ports
Description:	Some static consumption in input triggers of I/O ports may occur when entries are driven close to the trigger threshold (1mA to 2mA for each I/O at Vin = 2.4V for Vcc = 5V)
Workaround:	No

T09	Movx / Port0 / Read mode
Description:	When reading External Ram using Movx instruction, Port0's SFR may contain '0's whereas any access to external memories (data or program) should be by writing '1' into them .
Workaround:	No