



Rad-Hard 32-bit SPARC v8 Processor

ERRATA SHEET

Active Errata List

 Odd-numbered FPU register dependency not properly checked in some doubleprecision FPU operations

Table 1. Errata History

Product Release	Errata List
All AT697F part-numbers	1

Errata Description

Odd-numbered FPU register dependency not properly checked in some double-precision FPU operations

Data dependency is not properly checked between a load singleword floating-point instruction (LDF) involving an odd-numbered floating-point register as a destination of the load and an immediately following double-precision floating-point instruction (FADDd, FSUBd, FMULd, FDIVd or FSQRTd) that satisfies all of the following conditions:

- the odd-numbered floating-point register is used as (part of) a source operand
- the destination floating-point register is also a source operand
- in an FSUBd or FDIVd, the two source operands are different registers

In this case, the final result of the double-precision floating-point instruction will be wrong.

Other double-precision floating-point instructions (FCMPd, FCMPEd, FdTOi and FdTOs) are not affected by this issue and will operate as expected.

The error case appears when any of the six following sequences of instructions is present (n in [0:31], x and y as different even numbers in [0:30]):

Case 1:

$$\begin{array}{l} \text{LD [\$r]} \text{, } \$f_{\text{\tiny x+1}} \\ \textit{FPOPd}^{\text{(1)}} \ \$f_{\text{\tiny x}}, \ \$f_{\text{\tiny y}}, \ \$f_{\text{\tiny x}} \end{array}$$

Case 2:

LD [%r_n], %f_{x+1}

$$FPOPd^{(1)}$$
 %f_y, %f_x, %f_x

Case 3:

LD [%r], %f_{x+1}

$$FPOPd^{(1)}$$
 %f_x, %f_y, %f_y

Case 4:

$$\begin{array}{l} \text{LD [\$r_n], \$f_{x+1}} \\ \textit{FPOPd}^{(1)} \ \$f_y, \ \$f_x, \ \$f_y \end{array}$$

Case 5:

LD [%r_n], %f_{x+1}
$$FPOPd^{(2)}$$
 %f_x, %f_x, %f_x

Case 6:

LD [
$$\mbox{\$r}_{\mbox{\tiny n}}$$
], $\mbox{\$f}_{\mbox{\tiny x+1}}$
SQRTd $\mbox{\$f}_{\mbox{\tiny x}}$, $\mbox{\$f}_{\mbox{\tiny x}}$

Notes: 1. FPOPd is one of FADDd, FSUBd, FMULd or FDIVd.

2. FPOPd is one of FADDd or FMULd (FSUBd and FDIVd operate as expected).

Workarounds

If direct control over assembly language is possible, simply insert a NOP before the double-precision floating-point instruction (case 1 to 6):



LD [%r_n], %f_{x+1} NOP FPOPd <same registers set as described above>

If direct control over assembly language is not possible (high-level programming language such as C), checking the SPARC binary code against any of the six above mentioned faulty sequences of instructions shall be done using the code-checker program provided by Atmel (search for doc7787 on Atmel web site).

Although there is a very low likelihood of occurrence with high-level programming languages, customers facing this problem should contact the SPARC hotline (sparc-applab.hotline@nto.atmel.com).





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