

Active Errata List

- Reading Errors
- Empty Flag Parasitic Pulse

Errata History

Lot Number	Errata List
M67206H, M672061H, M67204H all lot numbers	1, 2

Errata Description

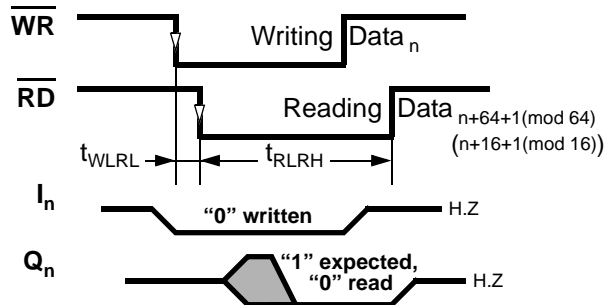
1. Reading errors.

Description

Sometimes a bit that has been written "1" is read "0".

Failure Conditions

1. Read and write commands fall down almost at the same time, t_{WLRL} parameter in the hereunder table.
2. Write bit "0" on input port while a bit "1" is expected on output port.
3. Reading the $64^{th}+1 \pmod{64}$ location ($16^{th} + 1 \pmod{16}$) for 4Kx9 FIFO) vs. the writing location.
4. Read pulse (t_{RLRH}) less than the one specified in the hereunder table.



Root Cause

The memory array of the 16Kx9 FIFO contains 64 columns, the 4Kx9 contains 16 columns. To reduce the read access time, a pipe line has been implemented on the data path. When the data_n is going out of the FIFO, the data_{n+1} is pre-fetched for the next read access. When the internal writing and reading are different from $64 \pmod{64}$ ($16 \pmod{16}$), a write and a read access are made on the same column. Coupling between the read bit-line and the write bit-line only disturbs the pre-fetch operation, forcing the sense amplifier to output "0". Then, the next external reading may be wrong.

Characterization

Worst case condition: 125°C / 4.5V

	t_{WLRL}		t_{RLRH}
	minimum	maximum	
67206H / 672061H	≥ 0 ns	≤ 8 ns	≤ 30 ns
67204H	≥ -2 ns	≤ 8 ns	≤ 25 ns



Radiation Tolerant FIFOs

M67206H M672061H M67204H Errata Sheet



Workaround

The workaround depends of the available means to implement it. Any of the following workarounds can be used:

1. No read sequence while write sequence.
2. Control the distance between the read and write locations.
3. Control the t_{WLRH} parameter in accordance with the above table.
4. Apply a read pulse t_{RLRH} greater than the value given in the above table.

2. Empty Flag Parasitic Pulse.

Description

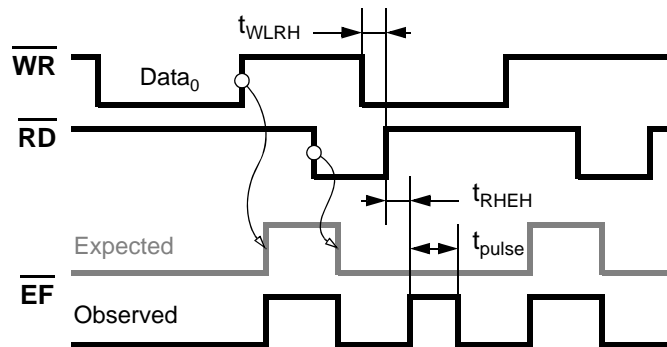
A parasitic positive pulse can be observed during a FIFO write if it is applied during the read of first data of the FIFO buffer (c.f. hereunder chronograms).

Side Effect

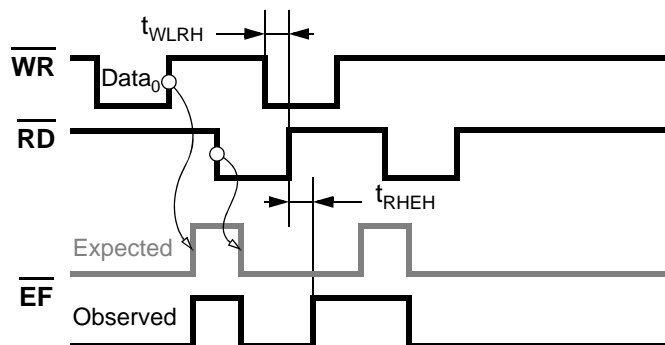
No side effect on flags computation, internal FIFO control and data integrity.

Behavior

1. \overline{WR} wide pulse width:



2. \overline{WR} short pulse width:



In this case, the falling edge of the parasitic pulse is masked by the beginning of the regular high level of \overline{EF} flag.

Root Cause

Un-controlled delays on input signals of a flags logic decoder generate an internal glitch. This glitch is re-formatted by the on-chip ETD system (Edge Transition Detection) and a parasitic pulse is output on \overline{EF} pin.

Work Around

Any of the following workarounds can be used:

1. No write sequence while read sequence.
2. \overline{EF} evaluation according to the following characterization.

Characterization

- Un-functioning window - t_{WLRH} :

	from	up to	Condition
t_{WLRH}	0 ns	10 ns	Vcc min, +125°C
	0 ns	6 ns	Vcc Max, -55°C

- Parasitic pulse delay - t_{RHEH} :

	delay	Condition
t_{RHEH}	15 ns	Vcc min, +125°C
	8 ns	Vcc Max, -55°C

- Parasitic pulse width- t_{pulse} :

	width	Comment
t_{pulse}	20 ns	Maximum



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