Features

- **Low Voltage and Standard Voltage Operation: 2.7 (V_{CC} = 2.7V to 5.5V)**
- **Internally Organized 128 x 8**
- **Two-wire Serial Interface**
- **Bidirectional Data Transfer Protocol**
- **1 MHz Compatibility**
- **4-Byte Page Write Mode**
- **Self-Timed Write Cycle (5 ms max)**
- **High Reliability**
  - **Endurance: 1 Million Write Cycles**
  - **Data Retention: 100 Years**
- **Automotive Grade and Lead-Free/Halogen-Free Devices Available**
- **8-lead JEDEC SOIC and 8-lead TSSOP Packages**

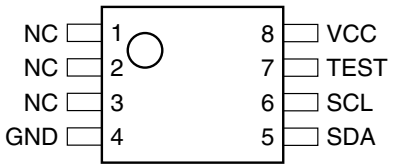
Description

The AT24C11 provides 1024 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 128 words of 8 bits each. The device is optimized for use in many automotive applications where low power and low voltage operation are essential. The AT24C11 is available in space saving 8-lead JEDEC SOIC and 8-lead TSSOP packages and is accessed via a Two-wire serial interface. In addition, the entire family is available in 2.7V (2.7V to 5.5V).

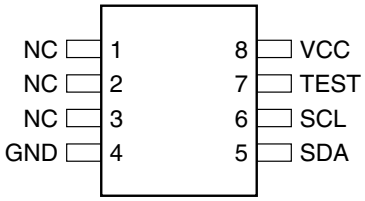
Table 0-1. Pin Configuration

Pin Name	Function
NC	No Connect
SDA	Serial Data
SCL	Serial Clock Input
TEST	Test Input (GND or VCC)

8-lead TSSOP



8-lead SOIC



Two-wire Automotive Temperature Serial EEPROM

1K (128 x 8)

AT24C11

Note: Not recommended for new design; please refer to AT24C01B Automotive datasheet.

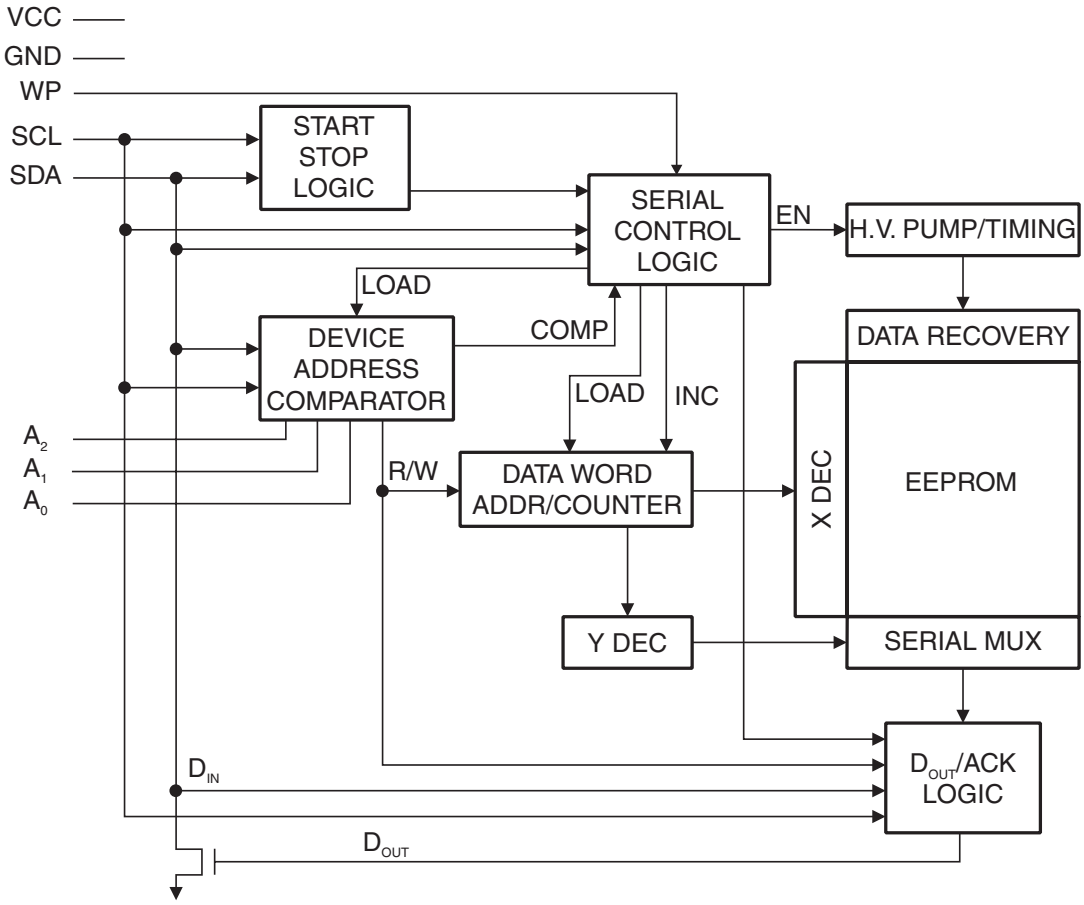
Rev. 5093E–SEEPR–8/07

Absolute Maximum Ratings*

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 0-1. Block Diagram



1. Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

2. Memory Organization

AT24C11, 1K SERIAL EEPROM: Internally organized with 32 pages of 4 bytes each. The 1K requires a 7-bit data word address for random word addressing.

Table 2-1. Pin Capacitance

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +2.7V to +5.5V

Symbol	Test Condition	Max	Units	Condition
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	6	pF	V_{IN} = 0V

Table 2-2. DC Characteristics

Applicable over recommended operating range from: T_{AE} = –40°C to +125°C, V_{CC} = +2.7V to +5.5V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		2.7		5.5	V
V_{CC2}	Supply Voltage		4.5		5.5	V
I_{CC}	Supply Current V_{CC} = 5.0V	READ at 100 kHz		0.4	1.0	mA
I_{CC}	Supply Current V_{CC} = 5.0V	WRITE at 100 kHz		2.0	3.0	mA
I_{SB1}	Standby Current V_{CC} = 1.8V	V_{IN} = V_{CC} or V_{SS}		0.6	3.0	µA
I_{SB2}	Standby Current V_{CC} = 2.5V	V_{IN} = V_{CC} or V_{SS}		1.4	4.0	µA
I_{SB3}	Standby Current V_{CC} = 2.7V	V_{IN} = V_{CC} or V_{SS}		1.6	4.0	µA
I_{SB4}	Standby Current V_{CC} = 5.0V	V_{IN} = V_{CC} or V_{SS}		8.0	18.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}		0.10	3.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}		0.05	3.0	µA
V_{IL}	Input Low Level(1)		–0.6		V_{CC} × 0.3	V
V_{IH}	Input High Level(1)		V_{CC} × 0.7		V_{CC} + 0.5	V
V_{OL2}	Output Low Level V_{CC} = 3.0V	I_{OL} = 2.1 mA			0.4	V
V_{OL1}	Output Low Level V_{CC} = 1.8V	I_{OL} = 0.15 mA			0.2	V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

Table 2-3. AC Characteristics

Applicable over recommended operating range from T_A = –40°C to +125°C, V_{CC} = +2.7V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	2.7V, 5.0V		Units
		Min	Max	
f_{SCL}	Clock Frequency, SCL		1000	kHz
t_{LOW}	Clock Pulse Width Low	0.4		µs
t_{HIGH}	Clock Pulse Width High	0.4		µs
t_{AA}	Clock Low to Data Out Valid	0.05	0.55	µs
t_{BUF}	Time the bus must be free before a new transmission can start(1)	0.5		µs
$t_{HD.STA}$	Start Hold Time	0.25		µs
$t_{SU.STA}$	Start Set-up Time	0.6		µs
$t_{HD.DAT}$	Data In Hold Time	0		µs
$t_{SU.DAT}$	Data In Set-up Time	100		ns
t_R	Inputs Rise Time(1)		0.3	µs
t_F	Inputs Fall Time(1)		100	ns
$t_{SU.STO}$	Stop Set-up Time	0.25		µs
t_{DH}	Data Out Hold Time	50		ns
t_{WR}	Write Cycle Time		5	ms
Endurance(1)	5.0V, 25°C, Page Mode	1M		Write Cycles

Note: 1. This parameter is ensured by characterization only.

3. Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 3-3 on page 6). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see Figure 3-4 on page 6).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition which terminates all communications. After a read sequence, the stop command will place the EEPROM in a standby power mode (see Figure 3-4 on page 6).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. Any device on the system bus receiving data (when communicating with the EEPROM) must pull the SDA bus low to acknowledge that it has successfully received each word. This must happen during the ninth clock cycle after each word received and after all other system devices have freed the SDA bus. The EEPROM will likewise acknowledge by pulling SDA low after receiving each address or data word (see Figure 3-5 on page 6).

STANDBY MODE: The AT24C11 features a low power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

MEMORY RESET: After an interruption in protocol, power loss or system reset, any 2-wire part can be reset by following these steps:

(a) Clock up to 9 cycles, (b) look for SDA high in each cycle while SCL is high and then (c) create a start condition as SDA is high.

Figure 3-1. Bus Timing
SCL: Serial Clock, SDA: Serial Data I/O

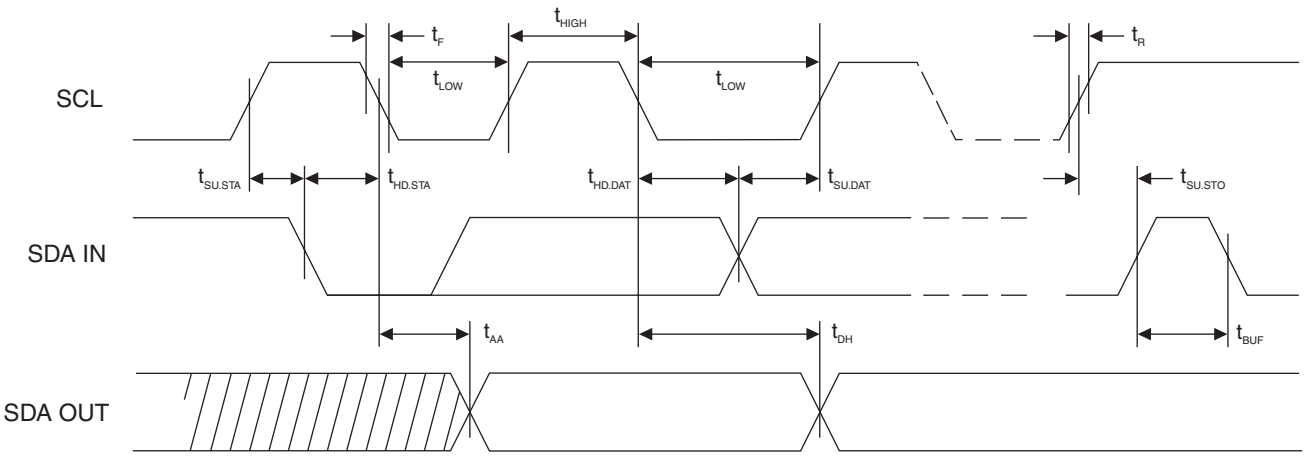
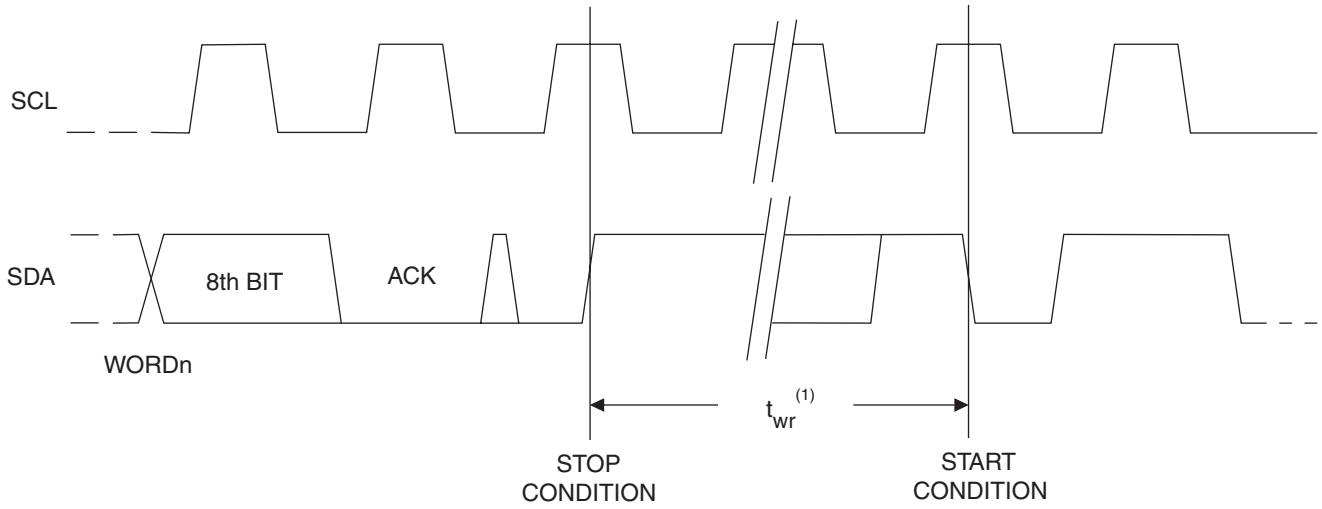


Figure 3-2. Write Cycle Timing
SCL: Serial Clock, SDA: Serial Data I/O



Note: 1. The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

Figure 3-3. Data Validity

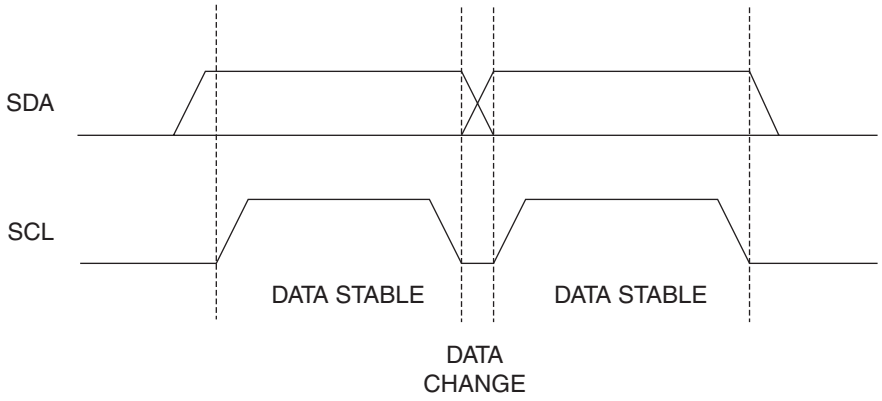


Figure 3-4. Start and Stop Definition

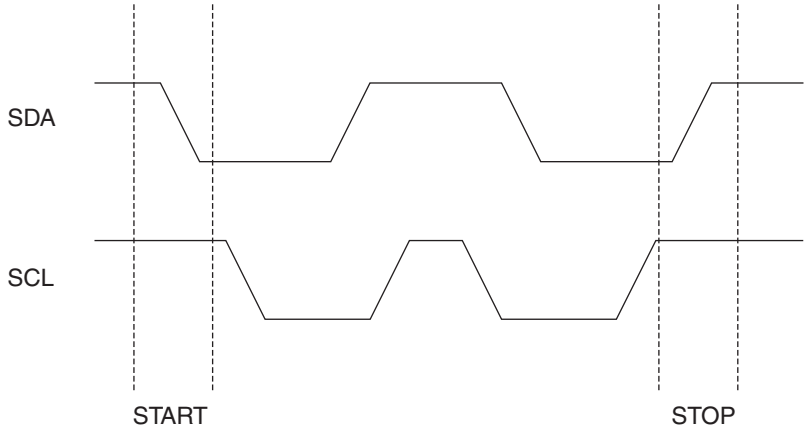
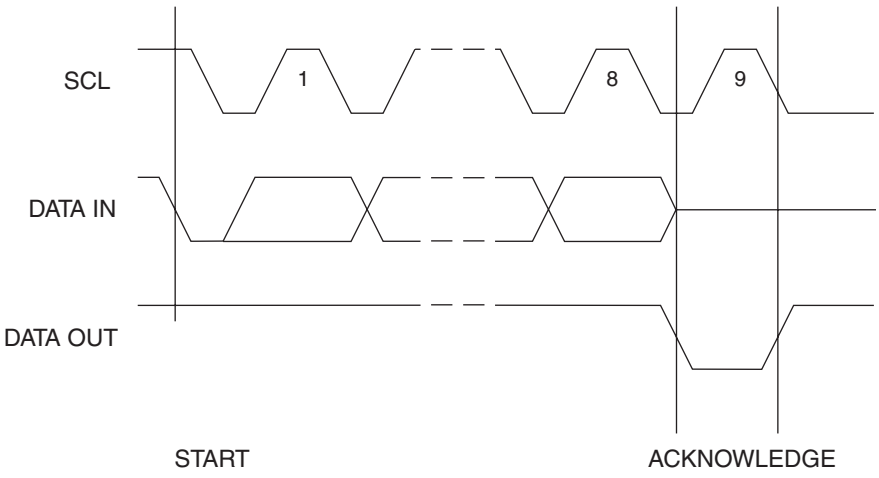


Figure 3-5. Output Acknowledge



4. Write Operations

BYTE WRITE: Following a start condition, a write operation requires a 7-bit data word address and a low write bit. Upon receipt of this address, the EEPROM will again respond with a zero and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally-timed write cycle to the nonvolatile memory. All inputs are disabled during this write cycle, t_{WR}, and the EEPROM will not respond until the write is complete (see refer to Figure 5-1 on page 8).

PAGE WRITE: The AT24C11 is capable of a 4-byte page write.

A page write is initiated the same as a byte write but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to three more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 5-2 on page 8).

The data word address lower 2 bits are internally incremented following the receipt of each data word. The higher five data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than four data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten. Access to 1 additional page is available upon request.

ACKNOWLEDGE POLLING: Once the internally-timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

5. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are two read operations: byte read and sequential read.

BYTE READ: A byte read is initiated with a start condition followed by a 7-bit data word address and a high read bit. The AT24C11 will respond with an acknowledge and then serially output 8 data bits. The microcontroller does not respond with a zero but does generate a following stop condition (see Figure 5-3 on page 8).

SEQUENTIAL READ: Sequential reads are initiated the same as a byte read. After the microcontroller receives an 8-bit data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will “roll over” and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with an input zero but does generate a following stop condition (see Figure 5-4 on page 8).

Figure 5-1. Byte Write

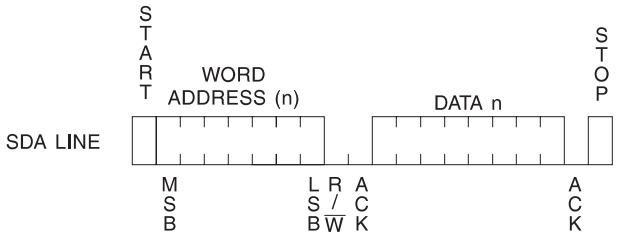


Figure 5-2. Page Write

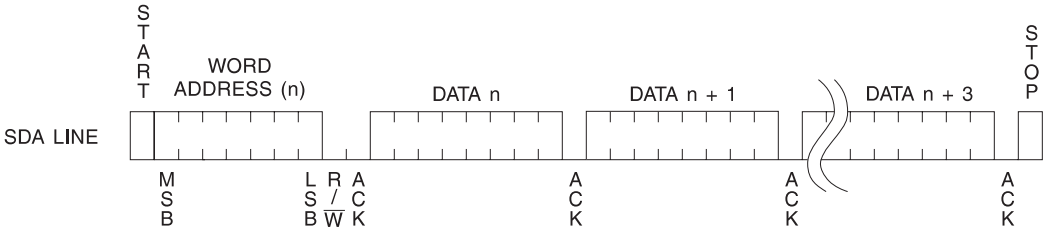


Figure 5-3. Byte Read

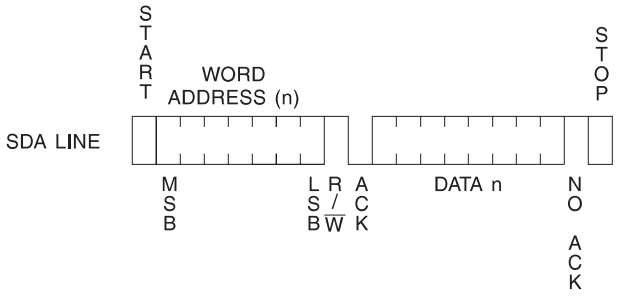
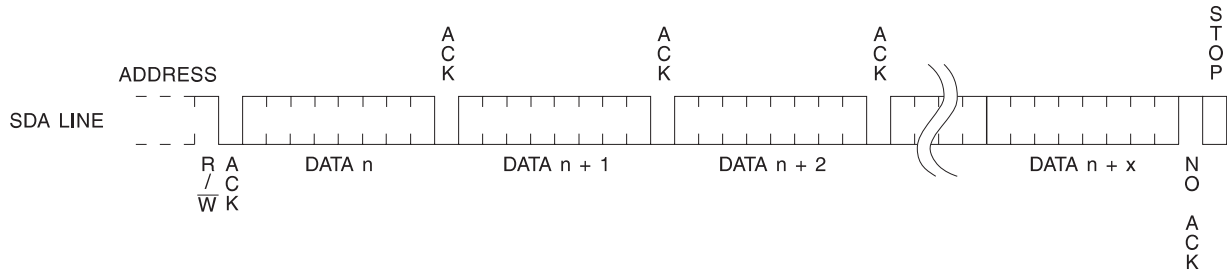


Figure 5-4. Sequential Read



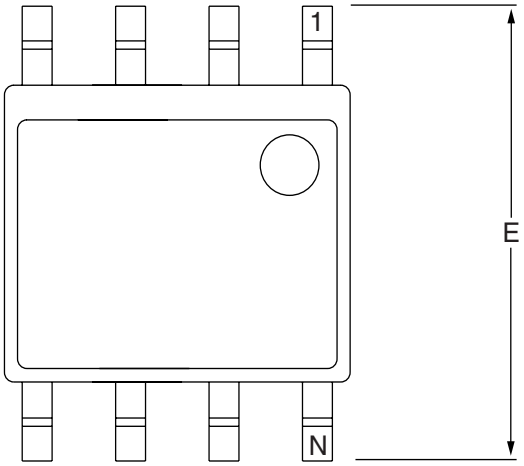
AT24C11 Ordering Information

Ordering Code	Package	Operation Range
AT24C11N-10SQ-2.7 AT24C11-10TQ-2.7	8S1 8A2	Lead-free/Halogen-free/ Automotive Temperature (–40°C to 85°C)

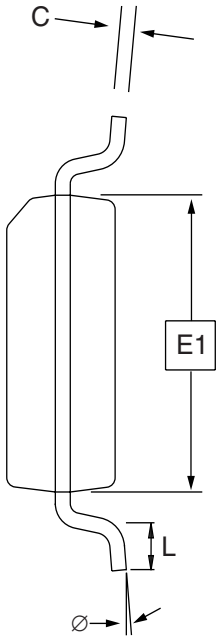
Package Type	
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8A2	8-lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP)
Options	
–2.7	Low-Voltage (2.7V to 5.5V)

Packaging Information

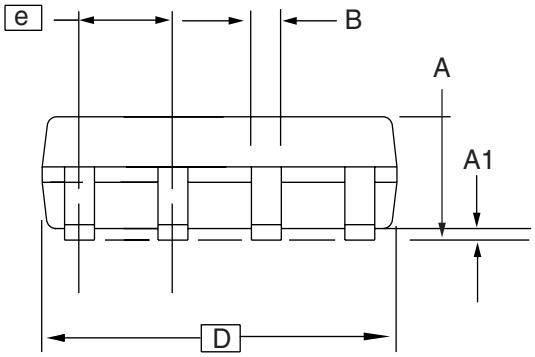
8S1 – JEDEC SOIC



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

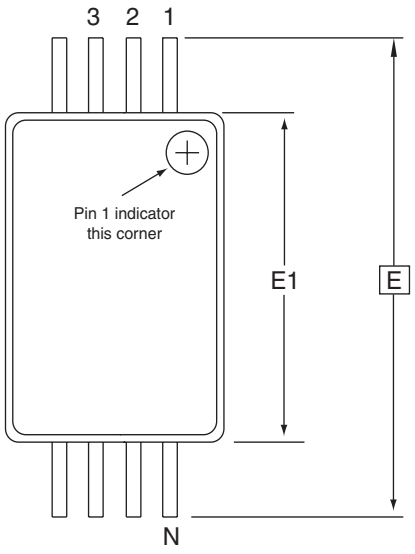
SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.00	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
∅	0°	–	8°	

Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

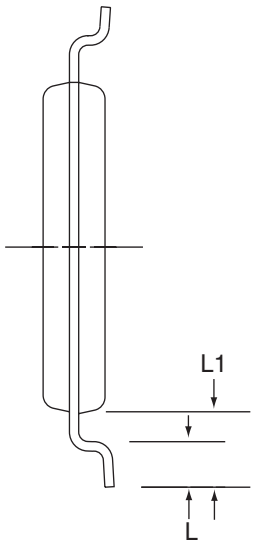
10/7/03

1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906	**TITLE** **8S1**, 8-lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**DRAWING NO.** 8S1	**REV.** B

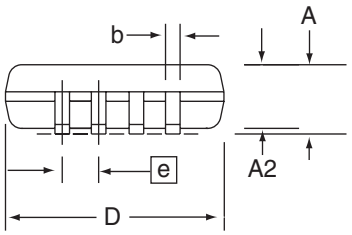
8A2 – TSSOP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
A	–	–	1.20	
A2	0.80	1.00	1.05	
b	0.19	–	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
5. Dimension D and E1 to be determined at Datum Plane H.

5/30/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8A2**, 8-lead, 4.4 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	8A2	B

Revision History

Doc. Rev.	Date	Comments
5093E	8/2007	Updated to new Template Updated common figures Added Note to first page
5093D	1/2007	Removed PDIP package offering Removed PB parts
5093C	9/2006	Revision history implemented; Removed ‘Preliminary’ status from datasheet.

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