

## Features

- Operating Voltage: 3.3V, 5V tolerant
- Access Time:
  - 17 ns
  - 15 ns
- Very Low Power Consumption
  - Active: 610 mW (Max) @ 17 ns<sup>(1)</sup>, 540 mW (Max) @ 25 ns
  - Standby: 3.3 mW (Typ)
- Wide Temperature Range: -55 to +125°C
- TTL-Compatible Inputs and Outputs
- Asynchronous
- Designed on 0.25 µm Radiation Hardened Process
- No Single Event Latch Up below LET Threshold of 80 MeV/mg/cm<sup>2</sup>@125°C
- Tested up to a Total Dose of 300 krad (Si) according to MIL-STD-883 Method 1019
- 500 Mils Wide FP36 Package
- ESD better than 2000V
- Quality Grades:
  - QML-Q or V
  - ESCC

Note: 1. 650 mW (Max) @ 15 ns

## Description

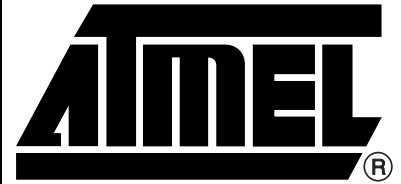
The AT60142HT is a very low power CMOS static RAM organized as 512K x 8 bits.

Atmel brings the solution to applications where fast computing is as mandatory as low consumption, such as aerospace electronics, portable instruments, or embarked systems.

Utilizing an array of six transistors (6T) memory cells, the AT60142HT combines an extremely low standby supply current (Typical value = 1 mA) with a fast access time at 15 ns over the full military temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

The AT60142HT is processed according to the methods of the latest revision of the MIL PRF 38535 or ESCC 9000.

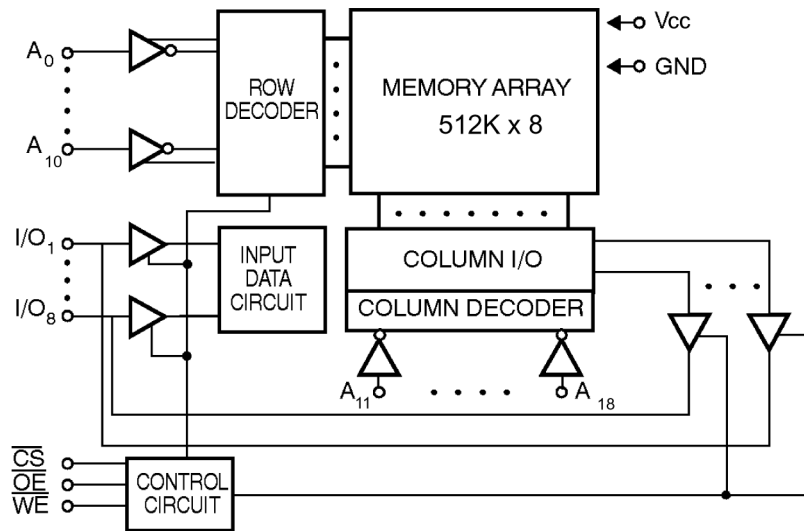
It is produced on a radiation hardened 0.25 µm CMOS process.



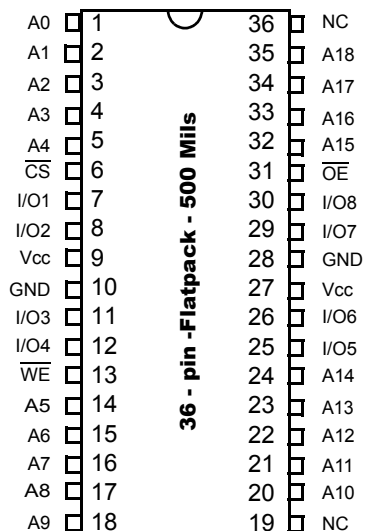
**Rad Hard**  
**512K x 8**  
**5V Tolerant**  
**Very Low Power**  
**CMOS SRAM**

**AT60142HT**

## Block Diagram



## Pin Configuration



Note: NC pins are not bonded internally. So, they can be connected to GND or Vcc.

## Pin Description

**Table 1.** Pin Names

Name	Description
A0 - A18	Address Inputs
I/O1 - I/O8	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground

**Table 2.** Truth Table<sup>(1)</sup>

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode
H	X	X	Z	Deselect / Power-down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	Z	Output Disable

Note: 1. L=low, H=high, X= L or H, Z=high impedance.

## Electrical Characteristics

### Absolute Maximum Ratings\*

Supply Voltage to GND Potential: ..... -0.5V + 4.6V  
 Voltage range on any input: ..... GND -0.5V to 7.0V  
 Voltage range on any output: ..... GND -0.5V to 7.0V  
 Storage Temperature: ..... -65°C to + 150°C  
 Output Current from Output Pins: ..... 20 mA  
 Electro Statics Discharge Voltage: ..... > 2000V  
 (MIL STD 883D Method 3015)

\*NOTE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. **Exposure between recommended DC operating and absolute maximum rating conditions for extended periods may affect device reliability.**

### Military Operating Range

Operating Voltage	Operating Temperature
3.3 ± 0.3V	-55°C to + 125°C

### Recommended DC Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply voltage	3.0	3.3	3.6	V
GND	Ground	0.0	0.0	0.0	V
V <sub>IL</sub>	Input low voltage	GND - 0.3	0.0	0.8	V
V <sub>IH</sub>	Input high voltage	2.2	—	5.5 <sup>(1)</sup>	V

Note: 1. 5.8V in transient conditions.

### Capacitance

Parameter	Description	Min	Typ	Max	Unit
C <sub>in</sub> <sup>(1)</sup>	Input capacitance	—	—	12	pF
C <sub>out</sub> <sup>(1)</sup>	Output capacitance	—	—	12	pF

Note: 1. Guaranteed but not tested.

## DC Parameters

### DC Test Conditions

TA = -55°C to + 125°C; Vss = 0V; VCC = 3.0V to 3.6V

Parameter	Description	Minimum	Typical	Maximum	Unit
IIX <sup>(1)</sup>	Input leakage current	-1	—	1	μA
IOZ <sup>(1)</sup>	Output leakage current	-1	—	1	μA
IIH <sup>(2)</sup> at 5.5V	Input Leakage Current	—	—	2	μA
IOZH <sup>(2)</sup> at 5.5V	Output Leakage Current	—	—	1.5	μA
VOL <sup>(3)</sup>	Output low voltage	—	—	0.4	V
VOH <sup>(4)</sup>	Output high voltage	2.4	—	—	V

1. GND < V<sub>IN</sub> < V<sub>CC</sub>, GND < V<sub>OUT</sub> < V<sub>CC</sub> Output Disabled.
2. V<sub>IN</sub> = 5.5V, V<sub>OUT</sub> = 5.5V, Output Disabled.
3. V<sub>CC</sub> min. I<sub>OL</sub> = 6 mA
4. V<sub>CC</sub> min. I<sub>OH</sub> = -4 mA.

### Consumption

Symbol	Description	TAVAV/TAVAW Test Condition	AT60142HT-17	AT60142HT-15	Unit	Value
I <sub>CCSB</sub> <sup>(1)</sup>	Standby Supply Current	—	2.5	2.5	mA	max
I <sub>CCSB1</sub> <sup>(2)</sup>	Standby Supply Current	—	2	2	mA	max
I <sub>CCOP</sub> <sup>(3)</sup> Read	Dynamic Operating Current	15 ns 17 ns 25 ns 50 ns 1 μs	- 170 150 75 10	180 170 150 75 10	mA	max
I <sub>CCOP</sub> <sup>(4)</sup> Write	Dynamic Operating Current	15 ns 17 ns 25 ns 50 ns 1 μs	- 145 130 120 100	150 145 130 120 100	mA	max

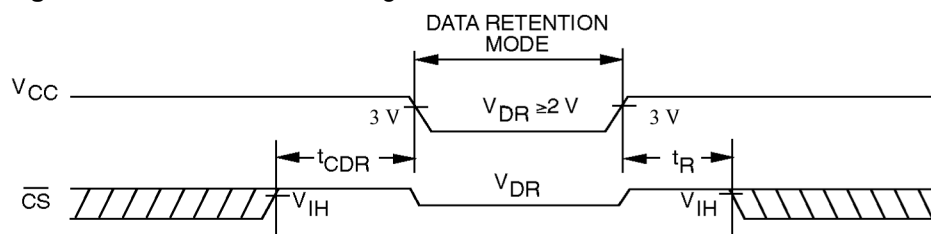
1.  $\overline{CS} \geq V_{IH}$
2.  $\overline{CS} \geq V_{CC} - 0.3V$
3.  $F = 1/T_{AVAV}$ , I<sub>out</sub> = 0 mA,  $\overline{WE} = \overline{OE} = V_{IH}$ , V<sub>IN</sub> = GND/V<sub>CC</sub>, V<sub>CC</sub> max.
4.  $F = 1/T_{AVAW}$ , I<sub>out</sub> = 0 mA,  $\overline{WE} = V_{IL}$ ,  $\overline{OE} = V_{IH}$ , V<sub>IN</sub> = GND/V<sub>CC</sub>, V<sub>CC</sub> max.

## Data Retention Mode

Atmel CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. During data retention chip select  $\overline{CS}$  must be held high within  $V_{CC}$  to  $V_{CC} - 0.2V$ .
2. Output Enable ( $\overline{OE}$ ) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3. During power-up and power-down transitions  $\overline{CS}$  and  $\overline{OE}$  must be kept between  $V_{CC} + 0.3V$  and 70% of  $V_{CC}$ .
4. The RAM can begin operation  $> t_R$  ns after  $V_{CC}$  reaches the minimum operation voltages (3V).

**Figure 1.** Data Retention Timing



## Data Retention Characteristics

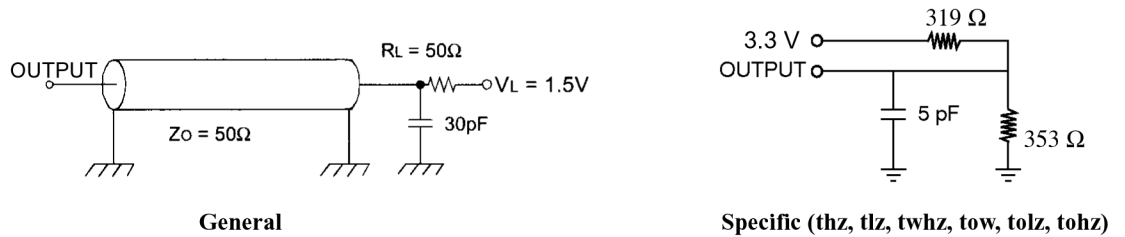
Parameter	Description	Min	Typ $T_A = 25^\circ C$	Max	Unit
$V_{CCDR}$	$V_{CC}$ for data retention	2.0	—	—	V
$t_{CDR}$	Chip deselect to data retention time	0.0	—	—	ns
$t_R$	Operation recovery time	$t_{AVAV}^{(1)}$	—	—	ns
$I_{CCDR}^{(2)}$	Data retention current	—	0.700	1.5 (AT60142HT-15)	mA
				1.5 (AT60142HT-17)	

1.  $T_{AVAV}$  = Read cycle time.
2.  $\overline{CS} = V_{CC}$ ,  $V_{IN} = GND/V_{CC}$ .

## AC Characteristics

Temperature Range:.....-55 +125°C  
 Supply Voltage:.....3.3 ±0.3V  
 Input Pulse Levels: ..... GND to 3.0V  
 Input Rise and Fall Times: .....3ns (10 - 90%)  
 Input and Output Timing Reference Levels: ..... 1.5V  
 Output Loading  $I_{OL}/I_{OH}$ :.....See Figure 2

**Figure 2.** AC Test Loads Waveforms



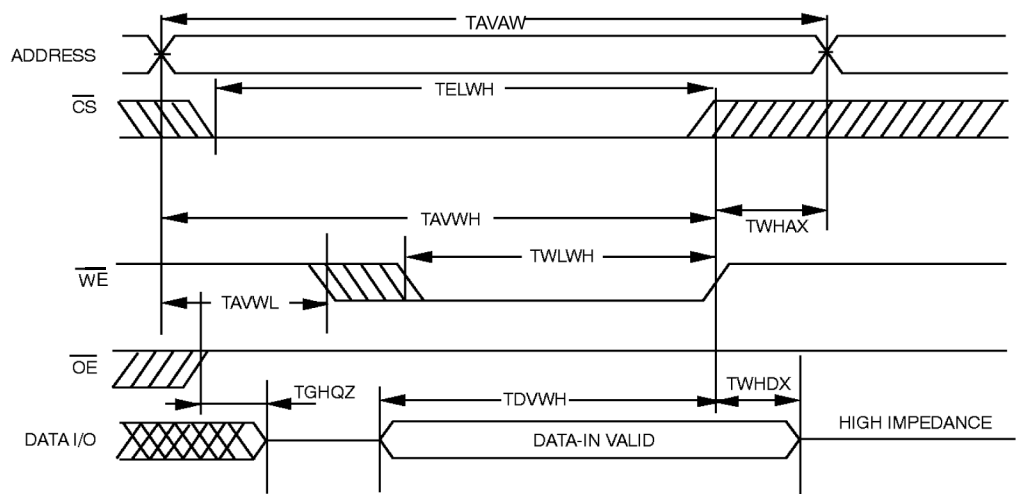
## Write Cycle

Symbol	Parameter	AT60142HT-17	AT60142HT-15	Unit	Value
TAVAW	Write cycle time	17	15	ns	min
TAVWL	Address set-up time	0	0	ns	min
TAVWH	Address valid to end of write	8	8	ns	min
TDVWH	Data set-up time	7	7	ns	min
TELWH	$\overline{CS}$ low to write end	12	10	ns	min
TWLQZ	Write low to high $Z^{(1)}$	7	6	ns	max
TWLWH	Write pulse width	8	8	ns	min
TWHAX	Address hold from end of write	0	0	ns	min
TWHDX	Data hold time	0	0	ns	min
TWHQX	Write high to low $Z^{(1)}$	3	3	ns	min

Notes: 1. Parameters guaranteed, not tested, with output loading 5 pF. (See "AC Test Loads Waveforms" on page 7.)

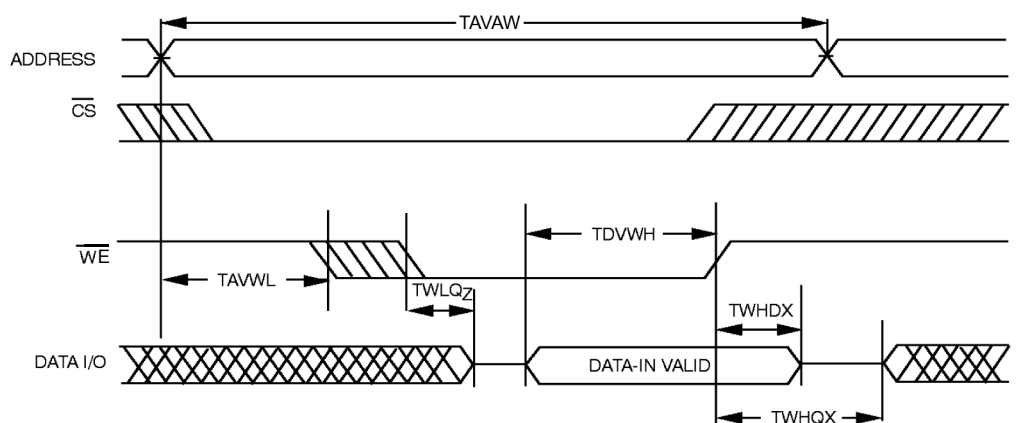
Write Cycle 1.

$\overline{WE}$  Controlled,  $\overline{OE}$  High During Write



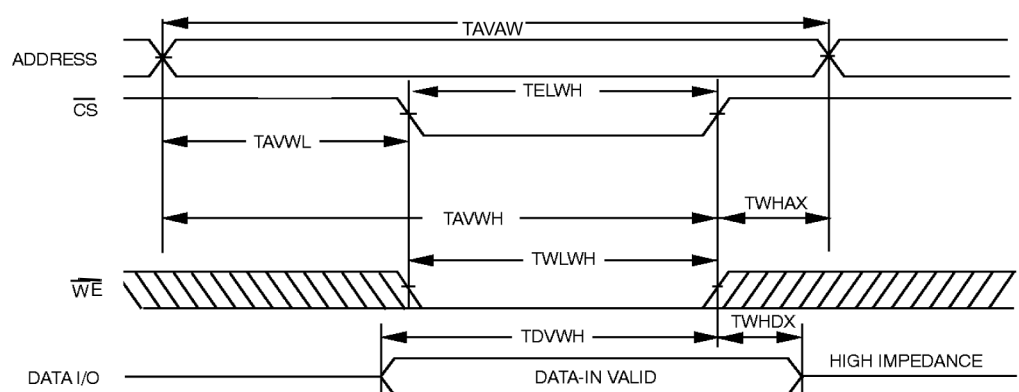
Write Cycle 2.

$\overline{WE}$  Controlled,  $\overline{OE}$  Low



Write Cycle 3.

$\overline{CS}$  Controlled



Note: The internal write time of the memory is defined by the overlap of CS Low and W LOW. Both signals must be activated to initiate a write and either signal can terminate a write by going in active mode. The data input setup and hold timing should be referenced to the active edge of the signal that terminates the write. Data out is high impedance if  $\overline{OE} = V_{IH}$ .



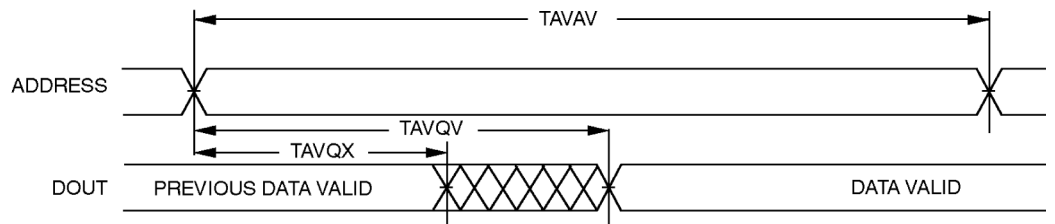
## Read Cycle

Symbol	Parameter	AT60142HT-17	AT60142HT-15	Unit	Value
TAVAV	Read cycle time	17	15	ns	min
TAVQV	Address access time	17	15	ns	max
TAVQX	Address valid to low Z	5	5	ns	min
TELQV	Chip-select access time	17	15	ns	max
TELQX	$\overline{CS}$ low to low Z <sup>(1)</sup>	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z <sup>(1)</sup>	7	6	ns	max
TGLQV	Output Enable access time	8	6	ns	max
TGLQX	$\overline{OE}$ low to low Z <sup>(1)</sup>	2	2	ns	min
TGHQZ	$\overline{OE}$ high to high Z <sup>(1)</sup>	6	5	ns	max

Note: 1. Parameters guaranteed, not tested, with output loading 5 pF. (See "AC Test Loads Waveforms" on page 7.)

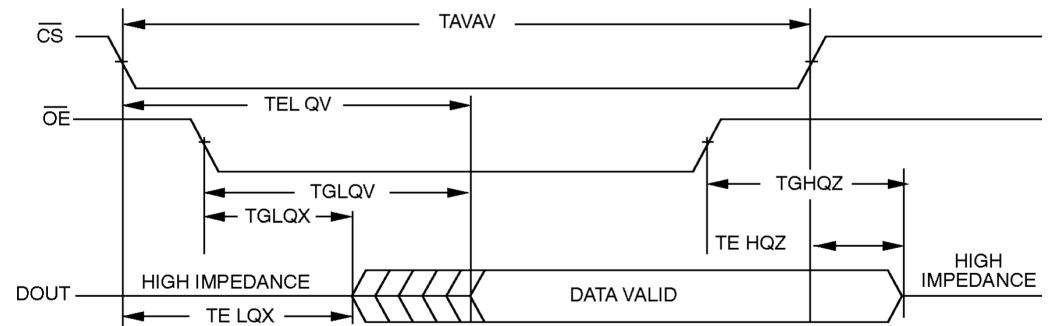
### Read Cycle nb 1

Address Controlled ( $\overline{CS} = \overline{OE} = V_{IL}$ ,  $\overline{WE} = V_{IH}$ )



### Read Cycle nb 2

Chip Select Controlled ( $\overline{WE} = V_{IH}$ )



## Ordering Information

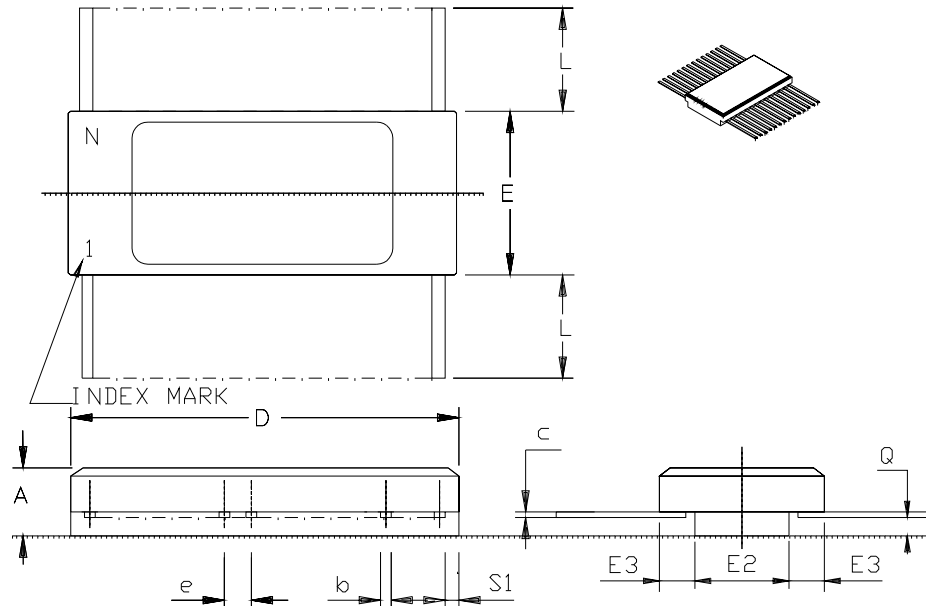
Part Number	Temperature Range	Speed	Package	Flow
AT60142HT-DS17M-E	25°C	17 ns/5V tol.	FP36.5 grounded lid	Engineering Samples
5962-0520803QYC	-55° to +125°C	17 ns/5V tol.	FP36.5 grounded lid	QML Q
5962-0520803VYC	-55° to +125°C	17 ns/5V tol.	FP36.5 grounded lid	QML V
5962R0520803VYC	-55° to +125°C	17 ns/5V tol.	FP36.5 grounded lid	QML V RHA
AT60142HT-DS17ESCC <sup>(3)</sup>	-55° to +125°C	17 ns/5V tol.	FP36.5 grounded lid	ESCC
AT60142HT-DD17M-E <sup>(1)</sup>	25°C	17 ns/5V tol.	Die	Engineering Samples
AT60142HT-DD17MSV <sup>(1)</sup>	-55° to +125°C	17 ns/5V tol.	Die	Space Level B
AT60142HT-DS15M-E <sup>(1)</sup>	25°C	15 ns/5V tol.	FP36.5 grounded lid	Engineering Samples
AT60142HT-DS15MMQ <sup>(1) (2)</sup>	-55° to +125°C	15 ns/5V tol.	FP36.5 grounded lid	Mil Level B
AT60142HT-DS15MSV <sup>(1) (2)</sup>	-55° to +125°C	15 ns/5V tol.	FP36.5 grounded lid	Space Level B
AT60142HT-DS15MSR <sup>(1) (2)</sup>	-55° to +125°C	15 ns/5V tol.	FP36.5 grounded lid	Space Level B RHA
AT60142HT-DS15ESCC <sup>(1) (3)</sup>	-55° to +125°C	15 ns/5V tol.	FP36.5 grounded lid	ESCC
AT60142HT-DD15M-E <sup>(1)</sup>	25°C	15 ns/5V tol.	Die	Engineering Samples
AT60142HT-DD15MSV <sup>(1)</sup>	-55° to +125°C	15 ns/5V tol.	Die	Space Level B

Note:

1. Contact Atmel for availability.
2. Will be replaced by SMD part number when available.
3. Will be replaced by ESCC part number when available.

## Package Drawing

### 36-lead Flat Pack (500 Mils)



	MM		INCH	
	Min	Max	Min	Max
A	2.29	3.05	.090	.120
b	0.38	0.51	.015	.020
c	0.10	0.18	.004	.007
D	---	23.62	---	.930
E	11.99	12.40	.472	.488
E2	8.89	---	.350	---
E3	0.76	---	.030	---
e	1.27	BSC	.050	BSC
L	7.75	8.26	.305	.325
Q	0.66	1.14	.026	.045
S1	0.13	---	.005	---
N	36		36	

## Document Revision History

Creation from AT60142FT with the following changes :

- Package DC removed
- Update of parameters  $I_{CCSB}$ ,  $I_{CCSB1}$ ,  $I_{CCDR}$

### Changes from Rev. A to Rev. B

1. In "Ordering Information" section page 10 :
  - Atmel P/N of 17ns/5V version replaced by SMD P/N



## Headquarters

---

**Atmel Corporation**  
2325 Orchard Parkway  
San Jose, CA 95131  
USA  
Tel: 1(408) 441-0311  
Fax: 1(408) 487-2600

## International

---

**Atmel Asia**  
Room 1219  
Chinachem Golden Plaza  
77 Mody Road Tsimshatsui  
East Kowloon  
Hong Kong  
Tel: (852) 2721-9778  
Fax: (852) 2722-1369

**Atmel Europe**  
Le Krebs  
8, Rue Jean-Pierre Timbaud  
BP 309  
78054 Saint-Quentin-en-  
Yvelines Cedex  
France  
Tel: (33) 1-30-60-70-00  
Fax: (33) 1-30-60-71-11

**Atmel Japan**  
9F, Tonetsu Shinkawa Bldg.  
1-24-8 Shinkawa  
Chuo-ku, Tokyo 104-0033  
Japan  
Tel: (81) 3-3523-3551  
Fax: (81) 3-3523-7581

## Product Contact

---

**Web Site**  
[www.atmel.com](http://www.atmel.com)

**Technical Support**  
Enter Product Line E-mail

**Sales Contact**  
[www.atmel.com/contacts](http://www.atmel.com/contacts)

**Literature Requests**  
[www.atmel.com/literature](http://www.atmel.com/literature)

---

**Disclaimer:** The information in this document is provided in connection with Atmel products. No license, express or implied, by estoppel or otherwise, to any intellectual property right is granted by this document or in connection with the sale of Atmel products. **EXCEPT AS SET FORTH IN ATMEL'S TERMS AND CONDITIONS OF SALE LOCATED ON ATMEL'S WEB SITE, ATMEL ASSUMES NO LIABILITY WHATSOEVER AND DISCLAIMS ANY EXPRESS, IMPLIED OR STATUTORY WARRANTY RELATING TO ITS PRODUCTS INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT. IN NO EVENT SHALL ATMEL BE LIABLE FOR ANY DIRECT, INDIRECT, CONSEQUENTIAL, PUNITIVE, SPECIAL OR INCIDENTAL DAMAGES (INCLUDING, WITHOUT LIMITATION, DAMAGES FOR LOSS OF PROFITS, BUSINESS INTERRUPTION, OR LOSS OF INFORMATION) ARISING OUT OF THE USE OR INABILITY TO USE THIS DOCUMENT, EVEN IF ATMEL HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.** Atmel makes no representations or warranties with respect to the accuracy or completeness of the contents of this document and reserves the right to make changes to specifications and product descriptions at any time without notice. Atmel does not make any commitment to update the information contained herein. Unless specifically provided otherwise, Atmel products are not suitable for, and shall not be used in, automotive applications. Atmel's products are not intended, authorized, or warranted for use as components in applications intended to support or sustain life.

©2009 Atmel Corporation. All rights reserved. Atmel® and combinations thereof are the registered trademarks of Atmel Corporation or its subsidiaries. Other terms and product names may be the trademarks of others.



Printed on recycled paper.