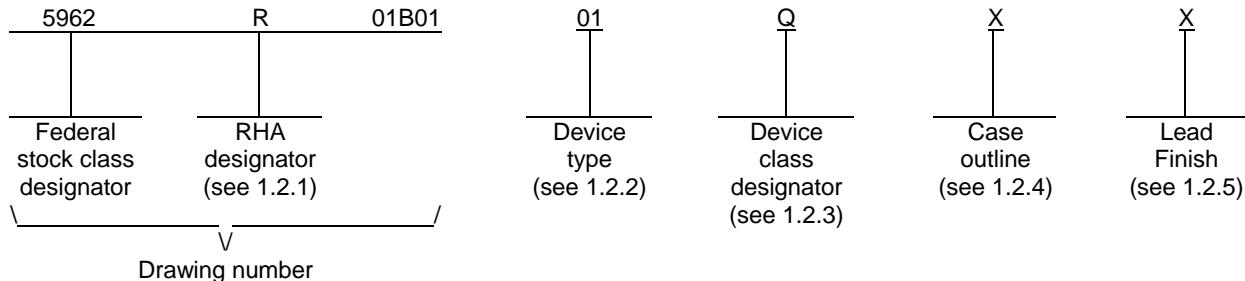


1. SCOPE

1.1 **Scope.** This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN) in the applicable Altered Item Drawing (AID). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

Customizations (personalizations) for each design, including circuit organization, electrical performance characteristics, and test conditions, shall be specified in an Altered Item Drawing (AID) (see 3.3 herein).

1.2 **PIN.** The PIN is as shown in the following example:



1.2.1 **RHA designator.** Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 **Device type(s).** The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	TH1099ER	1/ 3/ 988,000 sites available MH1RT
02	TH1156ER	1/ 3/ 1,558,000 sites available MH1RT
03	TH1242ER	1/ 3/ 2,422,000 sites available MH1RT
04	TH1332ER	1/ 3/ 3,319,000 sites available MH1RT
05	TH1099ES	2/ 3/ 988,000 sites available MH1RT
06	TH1156ES	2/ 3/ 1,558,000 sites available MH1RT
07	TH1242ES	2/ 3/ 2,422,000 sites available MH1RT
08	TH1332ES	2/ 3/ 3,319,000 sites available MH1RT
09	TH1M099ER	1/ 4/ composite 988,000 sites MH1RT
10	TH1M156ER	1/ 4/ composite 1,558,000 sites MH1RT
11	TH1M242ER	1/ 4/ composite 2,422,000 sites MH1RT
12	TH1M332ER	1/ 4/ composite 3,319,000 sites MH1RT
13	TH1M099ES	2/ 4/ composite 988,000 sites MH1RT
14	TH1M156ES	2/ 4/ composite 1,558,000 sites MH1RT
15	TH1M242ES	2/ 4/ composite 2,422,000 sites MH1RT
16	TH1M332ES	2/ 4/ composite 3,319,000 sites MH1RT

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<u>Device type</u>	<u>Generic number</u>			<u>Circuit function</u>
17	TH1099R	1/	3/	988,000 sites available MH1
18	TH1156R	1/	3/	1,558,000 sites available MH1
19	TH1242R	1/	3/	2,422,000 sites available MH1
20	TH1332R	1/	3/	3,319,000 sites available MH1
21	TH1099S	2/	3/	988,000 sites available MH1
22	TH1156S	2/	3/	1,558,000 sites available MH1
23	TH1242S	2/	3/	2,422,000 sites available MH1
24	TH1332S	2/	3/	3,319,000 sites available MH1
25	TH1M099R	1/	4/	composite 988,000 sites MH1
26	TH1M156R	1/	4/	composite 1,558,000 sites MH1
27	TH1M242R	1/	4/	composite 2,422,000 sites MH1
28	TH1M332R	1/	4/	composite 3,319,000 sites MH1
29	TH1M099S	2/	4/	composite 988,000 sites MH1
30	TH1M156S	2/	4/	composite 1,558,000 sites MH1
31	TH1M242S	2/	4/	composite 2,422,000 sites MH1
32	TH1M332S	2/	4/	composite 3,319,000 sites MH1
33	TH1256A			FPGA conversion

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835, and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	See figure 1	196	Quad flatpack unformed leads
Y	See figure 1	256	Quad flatpack unformed leads
Z	See figure 1	352	Quad flatpack with non conductive tie bar
U	See figure 1	349	Column grid array + interposer SCI
T	See figure 1	472	Column grid array + interposer SCI
M	See figure 1	196	Quad flatpack unformed leads – grounded lid
N	See figure 1	256	Quad flatpack unformed leads – grounded lid
4	See figure 1	352	Quad flatpack with non conductive tie bar – grounded lid
5	See figure 1	349	Column grid array + interposer SCI – grounded lid
6	See figure 1	472	Column grid array + interposer SCI – grounded lid
7	See figure 1	256	Unformed leads quad flat pack with tie bar – grounded lid
8	See figure 1	208	Unformed leads quad flat pack with tie bar – grounded lid

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ These devices are capable of operating at 2.5, 3.0, 3.3 V. See table I for limits.
 2/ These devices are capable of operating at 2.5, 3.0, 3.3 V and I/O are Tolerant/Compliant 5.0 V. See table I for limits.
 3/ Device will be customized at metal levels.
 4/ Device will be customized at base wafer and metal levels.

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1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range (V_{DD})	-0.5 V to 4.0 V
Supply voltage range (V_{CC})	-0.5 V to 6.0 V 3/
Input voltage range	
Low voltage range (V_{IN})	-0.5 V to V_{DD} + 0.5 V
5 V compliant (V_{IN}).....	-0.5 V to V_{CC} + 0.5 V
5 V tolerance (V_{IN})	-0.5 V to 6.0 V
Input pin current (I_{IN})	
Signal pin.....	-10.0 mA to 10.0 mA
Power pin.....	-60 mA to 60 mA
Lead temperature (soldering 10 sec)	+300°C 4/
Storage temperature range (T_s)	-65°C to +150°C
Maximum junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range 1(V_{DD})	2.7 V to 3.3 V
Supply voltage range 2(V_{DD})	2.3 V to 2.7 V
Supply voltage range 3(V_{DD})	3.0 V to 3.6 V
Supply voltage range – interface I_o (V_{CC})	4.5 V to 5.5 V 3/
Ambient temperature (T_A)	-55°C to 125°C

1.5 Radiation features.

Maximum total dose available	100 Krads 5/
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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. . Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

-
- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
 - 2/ All voltages referenced to ground unless otherwise specified.
 - 3/ V_{CC} range is applicable to the inner peripheral interface when compliant buffers are used.
 - 4/ Duration 10 sec maximum at a distance not less than 1.6 mm.
 - 5/ Unless otherwise specified in the AID.

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2.2 Non Government Publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents(s) which are DOD adopted are those listed in the DODISS cited in the solicitation

JEDEC PUB 95-1 – Design Requirements for Generic matrix Trays.

(Applications for copies should be addressed to the Electronic Industry Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or at <http://www.jedec.org>)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.3 AID requirements. All AIDs written against this SMD shall be sent to DSCC-VA. The following items shall be provided to the device manufacturer by the customer as part of an AID. Items 3.3.3 through 3.3.9 form a part of the manufacturer's design database/database archive. These items shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. As such, these items will not appear in the AID in the traditional sense.

3.3.1 Terminal connections and pin assignments.

3.3.2 Package type (see 1.2.4).

3.3.3 Functional block diagram (or equivalent VHDL behavioral description).

3.3.4 Logic diagram (or equivalent structural VHDL description).

3.3.5 Pin function description.

3.3.6 Design tape # or design document name (i.e., net list).

3.3.7 Design functional tape # or name.

3.3.8 Test functional tape # or name.

3.3.9 Switching waveform(s).

3.3.10 Fault coverage. The extent of fault coverage is controlled by the quality of the customers design input, therefore fault coverage shall be specified by the customer.

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3.3.11 Device electrical performance characteristics. Device electrical performance characteristics shall include dc parametric (see table I herein for minimum requirements), functional, input to output ac parameters and any other data which would be considered required by a design engineer. All electrical performance characteristics apply over the full recommended case operating temperature range and specified test load conditions.

3.3.12 Maximum power dissipation. Maximum power dissipation shall be in accordance with the application specific design.

3.3.13 RHA post-irradiated electoricals. For RHA devices supplied to this drawing, the RHA post irradiated electoricals shall be specified in the AID.

3.4 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.5 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.6 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q, and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A. The AID number shall be added to the marking by the manufacturer.

3.6.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.7 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCL-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.8 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change for device class M. For device class M, notification to DSCL-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.10 Verification and review for device class M. For device class M, DSCL, DSCL's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.11 Microcircuit group assignment for device class M. Device classes M devices covered by this drawing shall be in microcircuit group number 123 (see MIL-PRF-38535, appendix A).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions ^{1/} -55°C ≤ T _C ≤ 125°C 2.3 V ≤ V _{DD} ≤ 2.7 V unless otherwise specified for device operate at V _{DD} = 2.5 V	Group A Subgroups	Device type	Limits		Units
					Min	Max	
Low level input current (w/o pull-up or pull-down resistor)	I _{IL}	V _{IN} = V _{SS} , CMOS buffers	1,2,3	All	-1	1	μA
Low level input current Pull-up resistor PRU1 ^{2/}	I _{ILPU}	V _{IN} = V _{SS} , CMOS buffers	1,2,3	All	70	230	μA
Low level input current Pull-down resistor PRD1	I _{ILPD}	V _{IN} = V _{SS} , CMOS buffers	1,2,3	All	-5	5	μA
High level input current (w/o pull-up or pull-down resistor)	I _{IH}	V _{IN} = V _{DD} , CMOS buffers	1,2,3	All	-1	1	μA
High level input current Pull-up resistor PRU1	I _{IHPU}	V _{IN} = V _{DD} , CMOS buffers	1,2,3	All	-5	5	μA
High level input current Pull-down resistor PRD1 ^{3/}	I _{IHPD}	V _{IN} = V _{DD} , CMOS buffers	1,2,3	All	70	540	μA
High impedance state output current	I _{OZ}	V _{IN} = V _{DD} or V _{SS} , V _{DD} = V _{DD} max, All buffers	1,2,3	All	-1	1	μA
Low level input voltage	V _{IL}	CMOS buffers	1,2,3	All		0.3 V _{DD}	V
High level input voltage	V _{IH}	CMOS buffers	1,2,3	All	0.7 V _{DD}		V
Input leakage current cold sparing	I _{ICs}	V _{DD} = V _{SS} = 0 V, V _{IN} = 0 to V _{DD} max, PICZ buffers	1,2,3	All	-2	2	μA
Output leakage current cold sparing	I _{OCs}	V _{DD} = V _{SS} = 0 V, V _{OUT} = 0 to V _{DD} max, PO11Z buffers	1,2,3	All	-2	2	μA
Output low voltage ^{4/}	V _{OL}	I _{OL} = 0.8 mA, V _{DD} = V _{DD} min, PO11 buffers	1,2,3	All		0.4	V
Output high voltage ^{5/}	V _{OH}	I _{OH} = -0.6 mA, V _{DD} = V _{DD} min, PO11 buffers	1,2,3	All	2.0		V
Output short circuit current ^{6/}	I _{OSN}	PO11 output at low level shortened to V _{DD}	1,2,3	All		15	mA
Output short circuit current ^{6/}	I _{OSP}	PO11 output at high level shortened to V _{SS}	1,2,3	All		8	mA
Input capacitance ^{6/}	C _{IN}		4	All		2.4	pF
Output capacitance ^{6/}	C _{OUT}		4	All		5.6	pF
I/O capacitance ^{6/}	C _{I/O}		4	All		6.6	pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T _C ≤ 125°C 2.7 V ≤ V _{DD} ≤ 3.3 V unless otherwise specified for device operate at V _{DD} = 3.0 V	Group A Subgroups	Device type	Limits		Units
					Min	Max	
Low level input current (w/o pull-up or pull-down resistor)	I _{IL}	V _{IN} = V _{SS} , CMOS buffers	1,2,3	All	-1	1	μA
Low level input current Pull-up resistor PRU1 2/	I _{ILPU}	V _{IN} = V _{SS} , CMOS buffers	1,2,3	All	108	330	μA
Low level input current Pull-down resistor PRD1	I _{ILPD}	V _{IN} = V _{SS} , CMOS buffers	1,2,3	All	-5	5	μA
High level input current (w/o pull-up or pull-down resistor)	I _{IH}	V _{IN} = V _{DD} , CMOS buffers	1,2,3	All	-1	1	μA
High level input current Pull-up resistor PRU1	I _{IHPU}	V _{IN} = V _{DD} , CMOS buffers	1,2,3	All	-5	5	μA
High level input current Pull-down resistor PRD1 3/	I _{IHPD}	V _{IN} = V _{DD} , CMOS buffers	1,2,3	All	108	825	μA
High impedance state output current	I _{OZ}	V _{IN} = V _{DD} or V _{SS} , V _{DD} = V _{DD} max, All buffers, no pull resistor	1,2,3	All	-1	1	μA
Low level input voltage	V _{IL}	CMOS buffers	1,2,3	All		0.8	V
High level input voltage	V _{IH}	CMOS buffers	1,2,3	All	2.0		V
Input leakage current cold sparing	I _{I_{CS}}	V _{DD} = V _{SS} = 0 V, V _{IN} = 0 to V _{DD} max, PICZ buffers	1,2,3	All	-2	2	μA
Output leakage current cold sparing	I _{O_{CS}}	V _{DD} = V _{SS} = 0 V, V _{OUT} = 0 to V _{DD} max, PO11Z buffers	1,2,3	All	-2	2	μA
Output low voltage 4/	V _{OL}	I _{OL} = 1 mA, V _{DD} = V _{DD} min, PO11 buffers	1,2,3	All		0.4	V
Output high voltage 5/	V _{OH}	I _{OH} = -0.8 mA, V _{DD} = V _{DD} min, PO11 buffers	1,2,3	All	2.4		V
Output short circuit current 6/	I _{OSN}	PO11 output at low level shortened to V _{DD}	1,2,3	All		21	mA
Output short circuit current 6/	I _{OSP}	PO11 output at high level shortened to V _{SS}	1,2,3	All		12	mA
Input capacitance 6/	C _{IN}		4	All		2.4	pF
Output capacitance 6/	C _{OUT}		4	All		5.6	pF
I/O capacitance 6/	C _{I/O}		4	All		6.6	pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T _C ≤ 125°C 3.0 V ≤ V _{DD} ≤ 3.6 V unless otherwise specified for device operate at V _{DD} = 3.3 V	Group A Subgroups	Device type	Limits		Units
					Min	Max	
Low level input current (w/o pull-up or pull-down resistor)	I _{IL}	V _{IN} = V _{SS} , CMOS buffers	1,2,3	All	-1	1	μA
Low level input current Pull-up resistor PRU1 2/	I _{ILPU}	V _{IN} = V _{SS} , CMOS buffers	1,2,3	All	120	400	μA
Low level input current Pull-down resistor PRD1	I _{ILPD}	V _{IN} = V _{SS} , CMOS buffers	1,2,3	All	-5	5	μA
High level input current (w/o pull-up or pull-down resistor)	I _{IH}	V _{IN} = V _{DD} , CMOS buffers	1,2,3	All	-1	1	μA
High level input current Pull-up resistor PRU1	I _{IHPU}	V _{IN} = V _{DD} , CMOS buffers	1,2,3	All	-5	5	μA
High level input current Pull-down resistor PRD1 3/	I _{IHPD}	V _{IN} = V _{DD} , CMOS buffers	1,2,3	All	150	900	μA
High impedance state output current	I _{OZ}	V _{IN} = V _{DD} or V _{SS} , V _{DD} = V _{DD} max, All buffers	1,2,3	All	-1	1	μA
Low level input voltage	V _{IL}	CMOS buffers	1,2,3	All		0.8	V
High level input voltage	V _{IH}	CMOS buffers	1,2,3	All	2.0		V
Input leakage current cold sparing	I _{ICS}	V _{DD} = V _{SS} = 0 V, V _{IN} = 0 to V _{DD} max, PICZ buffers	1,2,3	All	-2	2	μA
Output leakage current cold sparing	I _{OCs}	V _{DD} = V _{SS} = 0 V, V _{OUT} = 0 to V _{DD} max, PO11Z buffers	1,2,3	All	-2	2	μA
Output low voltage 4/	V _{OL}	I _{OL} = 2 mA, V _{DD} = V _{DD} min, PO11 buffers	1,2,3	All		0.4	V
Output high voltage 5/	V _{OH}	I _{OH} = -1.8 mA, V _{DD} = V _{DD} min, PO11 buffers	1,2,3	All	2.4		V
Output short circuit current 6/	I _{OSN}	PO11 output at low level shortened to V _{DD}	1,2,3	All		23	mA
Output short circuit current 6/	I _{OSP}	PO11 output at high level shortened to V _{SS}	1,2,3	All		13	mA
Input capacitance 6/	C _{IN}		4	All		2.4	pF
Output capacitance 6/	C _{OUT}		4	All		5.6	pF
I/O capacitance 6/	C _{I/O}		4	All		6.6	pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T _C ≤ 125°C 2.3 V ≤ V _{DD} ≤ 3.6 V 7/ 4.5 V ≤ V _{CC} ≤ 5.5 V 8/ unless otherwise specified for bi-voltage operating devices	Group A Subgroups	Device type	Limits		Units
					Min	Max	
Low level input current (w/o pull-up or pull-down resistor)	I _{IL}	V _{IN} = V _{SS} , CMOS buffers	1,2,3	9/	-1	1	μA
Low level input current Pull-up resistor PRU1 2/	I _{ILPU}	V _{IN} = V _{SS} , CMOS buffers	1,2,3	9/	180	690	μA
Low level input current Pull-down resistor PRD1	I _{ILPD}	V _{IN} = V _{SS} , CMOS buffers	1,2,3	9/	-5	5	μA
High level input current (w/o pull-up or pull-down resistor)	I _{IH}	V _{IN} = V _{CC} , V _{DD} = V _{DD} max, V _{CC} = V _{CC} max, CMOS buffers	1,2,3	9/	-1	1	μA
High level input current Pull-up resistor PRU1	I _{IHPU}	V _{IN} = V _{CC} , V _{DD} = V _{DD} max, V _{CC} = V _{CC} max, CMOS buffers	1,2,3	9/	-5	5	μA
High level input current Pull-down resistor PRD1 3/	I _{IHPD}	V _{IN} = V _{CC} , V _{DD} = V _{DD} max, V _{CC} = V _{CC} max, CMOS buffers	1,2,3	9/	30	400	μA
High impedance state output current	I _{OZ}	V _{IN} = V _{CC} or V _{SS} , V _{DD} = V _{DD} max, V _{CC} = V _{CC} max, All buffers	1,2,3	9/	-1	1	μA
Low level input voltage	V _{IL}	CMOS buffers	1,2,3	9/		0.8	V
High level input voltage	V _{IH}	CMOS buffers	1,2,3	9/		2.0	V
Input leakage current cold sparing	I _{ICS}	V _{CC} = V _{SS} = 0 V, V _{IN} = 0 to V _{DD} max, PICZ buffers	1,2,3	9/	-2	2	μA
Output leakage current cold sparing	I _{OCs}	V _{DD} = V _{SS} = 0 V, V _{OUT} = 0 to V _{DD} max, PO11Z buffers	1,2,3	9/	-2	2	μA
Output low voltage 4/	V _{OL}	V _{DD} = V _{DD} min, V _{CC} = V _{CC} min,	1,2,3	9/		0.4	V
Output high voltage 5/	V _{OH}	V _{DD} = V _{DD} min (3.0 V / 3.3 V), V _{CC} = V _{CC} min	1,2,3	9/	2.4		V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _A ≤ 125°C 2.3 V ≤ V _{DD} ≤ 3.6 V <u>7/</u> 4.5 V ≤ V _{CC} ≤ 5.5 V <u>8/</u> unless otherwise specified for bi-voltage operating devices	Group A Subgroups	Device type	Limits		Units
					Min	Max	
Output high voltage <u>5/</u>	V _{OH}	V _{DD} = V _{DD} min (2.5 V), V _{CC} = V _{CC} min	1,2,3	<u>9/</u>	2.0		V
Output short circuit current <u>6/</u>	I _{OSN}	PO11 output at low level shortened to V _{CC}	1,2,3	<u>9/</u>		28	mA
Output short circuit current <u>6/</u>	I _{OSP}	PO11 output at high level shortened to V _{SS}	1,2,3	<u>9/</u>		17	mA
Threshold trigger input voltage <u>6/</u>	V _{T+}			<u>9/</u>	2.0		V
Threshold trigger input voltage <u>6/</u>	V _{T-}			<u>9/</u>		0.8	V
Input capacitance <u>6/</u>	C _{IN}		4	<u>9/</u>		2.4	pF
Output capacitance <u>6/</u>	C _{OUT}		4	<u>9/</u>		5.6	pF
I/O capacitance <u>6/</u>	C _{I/O}		4	<u>9/</u>		6.6	pF

See footnotes at end of table.

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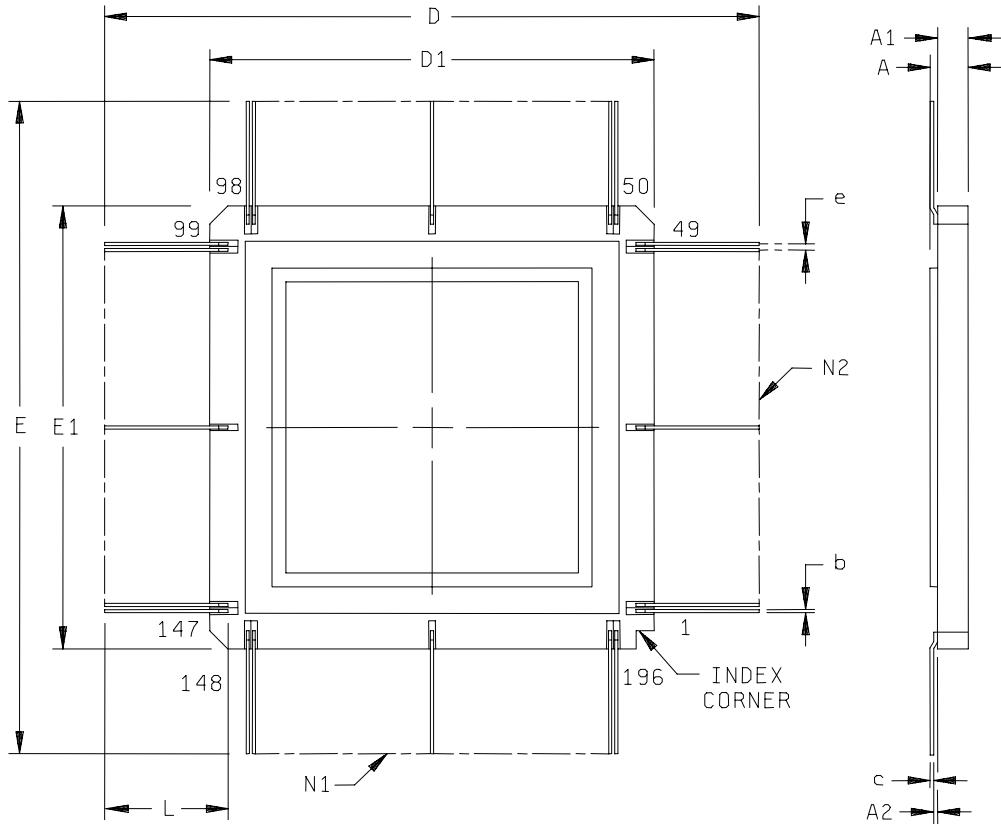
TABLE I. Electrical performance characteristics – Continued.

Notes:

- 1/ Devices supplied to this drawing will meet all levels M, D, P, L and R of irradiation. However, this device is only tested at the 'R' level. Pre and Post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, $T_A = +25$ C. Post irradiation electrical parameters shall be as specified in the AID.
- 2/ Standard pull-ups: PRU# where # = [1-31] index for Ron:
 - Ron = # x R0 = 19 kΩ typ (12 to 30 kΩ) in 2.5 V range.
 - Ron = # x R0 = 15 kΩ typ (10 to 25 kΩ) in 3.0 V range.
 - Ron = # x R0 = 14 kΩ typ (9 to 25 kΩ) in 3.3 V range.
 5 V tolerant/compliant pull-ups: PRU# where # = [1-31] index for Ron:
 - Ron = # x R0 = 14 kΩ typ (8 to 25kΩ) in each range.
- 3/ Standard pull-downs: PRD# where # = [1-31] index for Ron:
 - Ron = # x R0 = 11 kΩ typ (5 to 30 kΩ) in 2.5 V range.
 - Ron = # x R0 = 9 kΩ typ (4 to 25 kΩ) in 3.0 V range.
 - Ron = # x R0 = 8 kΩ typ (4 to 20 kΩ) in 3.3 V range.
 5 V tolerant/compliant pull-downs: PRD# where # = [1-31] index for Ron:
 - Ron = # x R0 = 36 kΩ typ (17 to 80 kΩ) in 2.5 V range.
 - Ron = # x R0 = 23 kΩ typ (11 to 55 kΩ) in 3.0 V range.
 - Ron = # x R0 = 19 kΩ typ (9 to 45 kΩ) in 3.3 V range.
- 4/ Output buffers: PO\$# where
 - \$ = [1-12] quantity of output driving capability of p-channels.
 - # = [1-12] quantity of output driving capability of n-channels.
 Standard buffers (including cold sparing)
 - IO = 1.6, 1.8, 2.0 mA measured at $V_{OL} = 0.4, 0.4, 0.4$ V in 2.5, 3.0, 3.3 V range respectively.
 Tolerance buffers (including cold sparing)
 - IO = 1.0, 1.3, 1.4 mA measured at $V_{OL} = 0.4, 0.4, 0.4$ V in 2.5, 3.0, 3.3 V range respectively.
 Compliant buffers ($V_{CC} = 4.5$ V)
 - IO = 1.1, 1.4, 1.6 mA measured at $V_{OL} = 0.4, 0.4, 0.4$ V in 2.5, 3.0, 3.3 V range respectively.
- 5/ Output buffers: PO\$# where
 - \$ = [1-12] quantity of output driving capability of p-channels.
 - # = [1-12] quantity of output driving capability of n-channels.
 Standard buffers (including cold sparing)
 - IO = -1.6, -1.8, -2.0 mA measured at $V_{OH} = 2.0, 2.4, 2.4$ V in 2.5, 3.0, 3.3 V range respectively.
 Tolerance buffers (including cold sparing)
 - IO = -1.0, -1.3, -1.4 mA measured at $V_{OH} = 2.0, 2.4, 2.4$ V in 2.5, 3.0, 3.3 V range respectively.
 Compliant buffers ($V_{CC} = 4.5$ V)
 - IO = -1.1, -1.4, -1.6 mA measured at $V_{OH} = 2.0, 2.4, 2.4$ V in 2.5, 3.0, 3.3 V range respectively.
- 6/ Tested at initial design and after major process changes, otherwise guaranteed.
- 7/ 5 V tolerant buffers.
- 8/ 5 V compliant buffers.
- 9/ Device types 5-8, 13-16,21-24, 29-32.

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CASE X



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.13	2.65	.084	.104
A1	1.83	2.24	.072	.088
A2	0.203 REF		.008 REF	
C	0.102	0.203	.004	.008
D/E	46.73	47.94	1.840	1.887
D1/E1	34.03	34.54	1.340	1.360
e	0.635 BSC		.025 BSC	
f	0.20 REF		.008 REF	
L	6.35	6.70	.250	.264
N1/N2	49		49	

FIGURE 1. Case Outline.

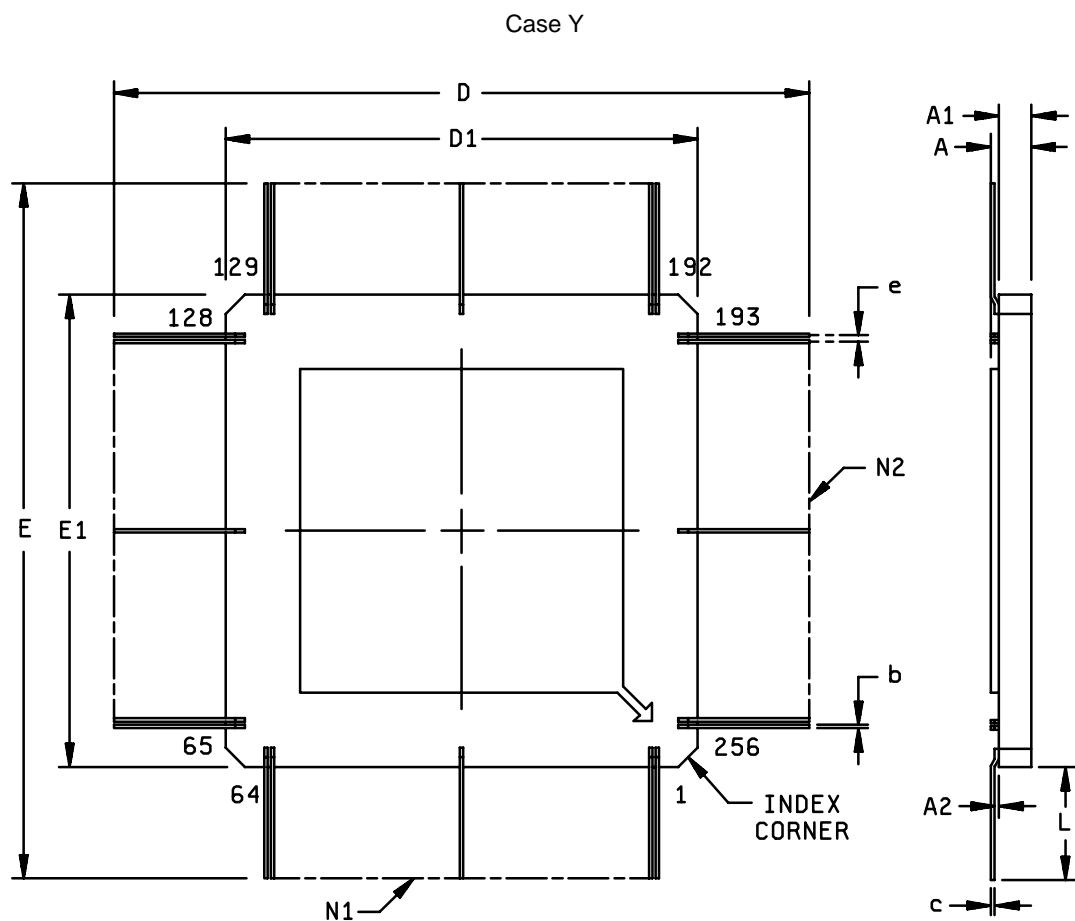
**STANDARD
MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

**SIZE
A**

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Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.41	3.18	.095	.125
C	0.10	0.20	.004	.008
D/D1	53.23	55.74	2.095	2.195
E/E1	36.83	37.34	1.450	1.470
e	0.508 BSC		.020 BSC	
f	0.15	0.25	.006	.010
A1	2.06	2.56	.081	.101
A2	0.05	0.36	.002	.014
L	8.20	9.20	.323	.362
N1/N2	64		64	

FIGURE 1. Case Outline – Continued.

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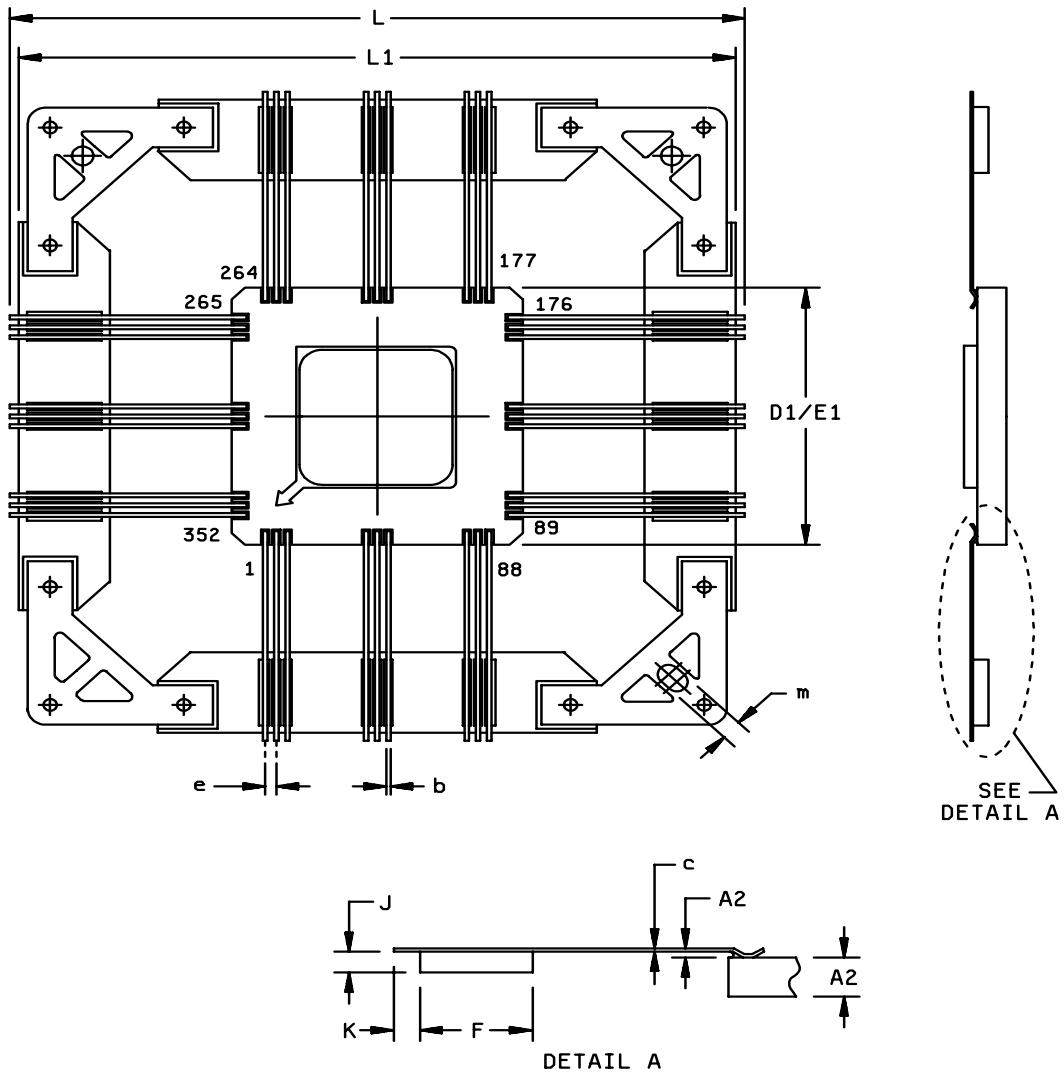
**SIZE
A**

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CASE Z

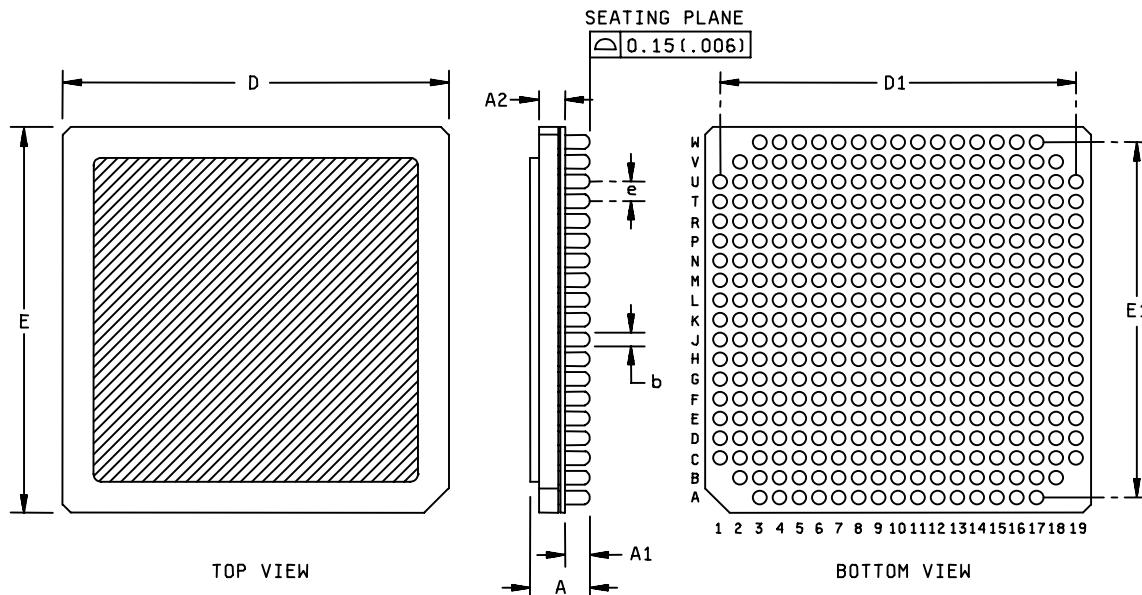


Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A1	2.35	3.15	.092	.124	G	2.50	2.60	.098	.104
A2	0.05	0.35	.002	.014	J	0.75	1.05	.029	.041
b	0.19	0.25	.007	.010	K			0.50	
c	0.11	0.20	.004	.009	L	74.85	76.40	2.947	3.008
D1/E1	47.52	48.48	1.871	1.908	L1	74.60	75.40	2.937	2.969
e	0.50 Basic		.0196 Basic		m	2.50	2.65	.098	.104
F	4.50	5.50	.177	.217					

FIGURE 1. Case Outline – Continued.

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Case U



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	4.30	5.90	.169	.232
A1	1.40	1.85	.055	.073
A2	2.40	3.45	.094	.136
b	0.79	0.99	.031	.040
D/E	24.80	25.20	.976	.992
D1/E1	22.86 (1.27 x 18)		.900 (.05 x 18)	
e	1.27 REF		.050 REF	

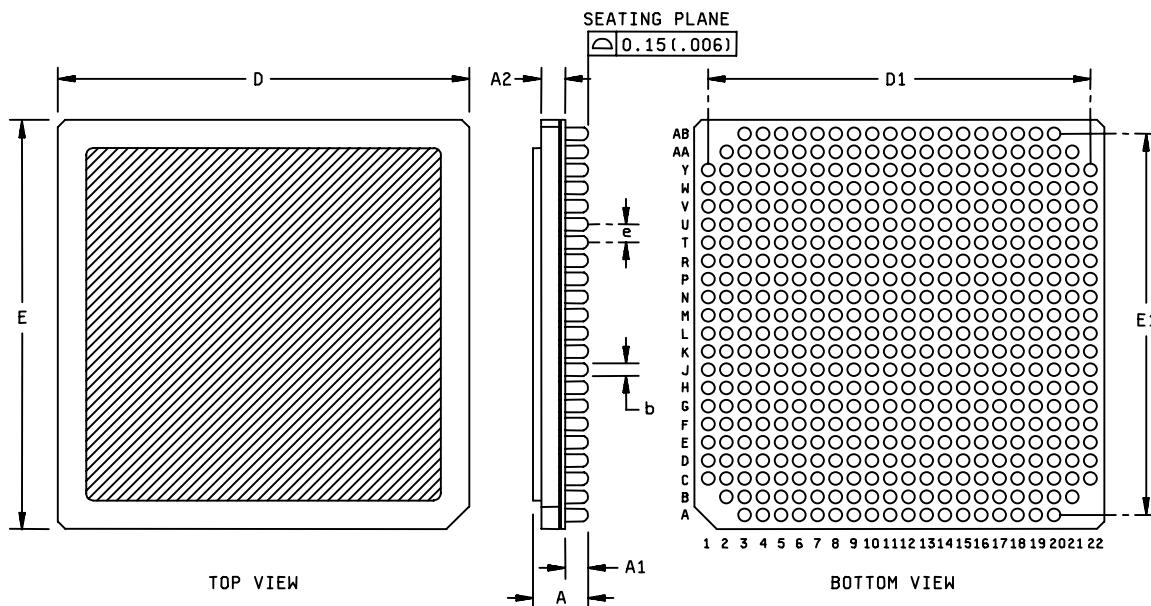
NOTES:

1. All dimensions and tolerance conform to ANSI Y14.5 – 1994.
2. Solder column position designation per JEDEC publication 95-1 standard procedures and practices SP-010.
3. "e" represents the basic solder column grid pitch.
4. Dimension b is measured at the maximum solder column diameter, parallel to primary datum.
5. Primary datum and seating plane are defined by the ends of the solder columns.
6. The A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, indentation, or other feature of package body, lid or integral heat slug.
7. Solder column array may be depopulated by any method, provided there is no pattern shifting. Depopulation is the omission of solder columns from a full matrix.

Figure 1. Case Outline – Continued.

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Case T



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	4.30	5.90	.169	.232
A1	1.40	1.85	.055	.073
A2	2.60	3.45	.102	.136
b	0.79	0.99	.031	.040
D/E	28.77	29.23	1.133	1.151
D1/E1	26.67 (1.27 x 21)		1.05 (.05 x 21)	
e	1.27 REF		.050 REF	

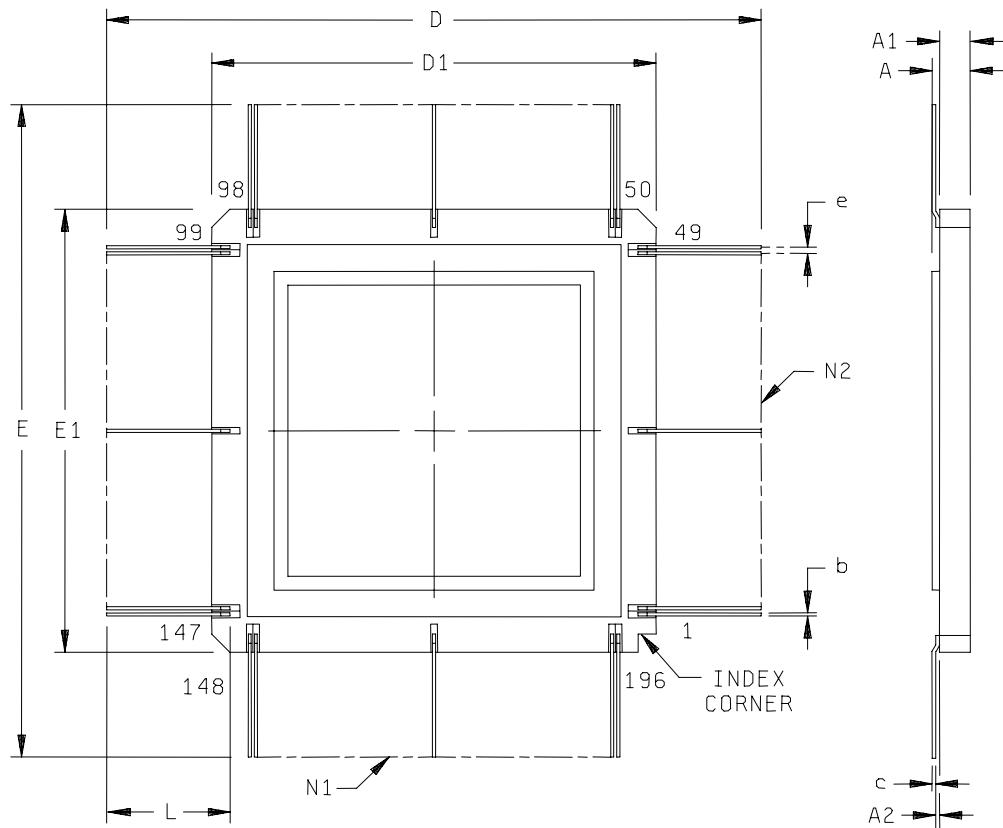
NOTES:

1. All dimensions and tolerance conform to ANSI Y14.5 – 1994.
2. Solder column position designation per JEDEC publication 95-1 standard procedures and practices SP-010.
3. "e" represents the basic solder column grid pitch.
4. Dimension b is measured at the maximum solder column diameter, parallel to primary datum.
5. Primary datum and seating plane are defined by the ends of the solder columns.
6. The A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, indentation, or other feature of package body, lid or integral heat slug.
7. Solder column array may be depopulated by any method, provided there is no pattern shifting. Depopulation is the omission of solder columns from a full matrix.

Figure 1. Case Outline – Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A	5962-01B01
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CASE M



Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	2.13	2.65	.084	.104	D1/E1	34.03	34.54	1.340	1.360
A1	1.83	2.24	.072	.088	e	0.635	BSC	.025	BSC
A2	0.203 REF		.008 REF		f	0.20 REF		.008 REF	
C	0.102	0.203	.004	.008	L	6.35	6.70	.250	.264
D/E	46.73	47.94	1.840	1.887	N1/N2	49		49	

NOTE:

1. Lid is connected to ground.

FIGURE 1. Case Outline - Continued.

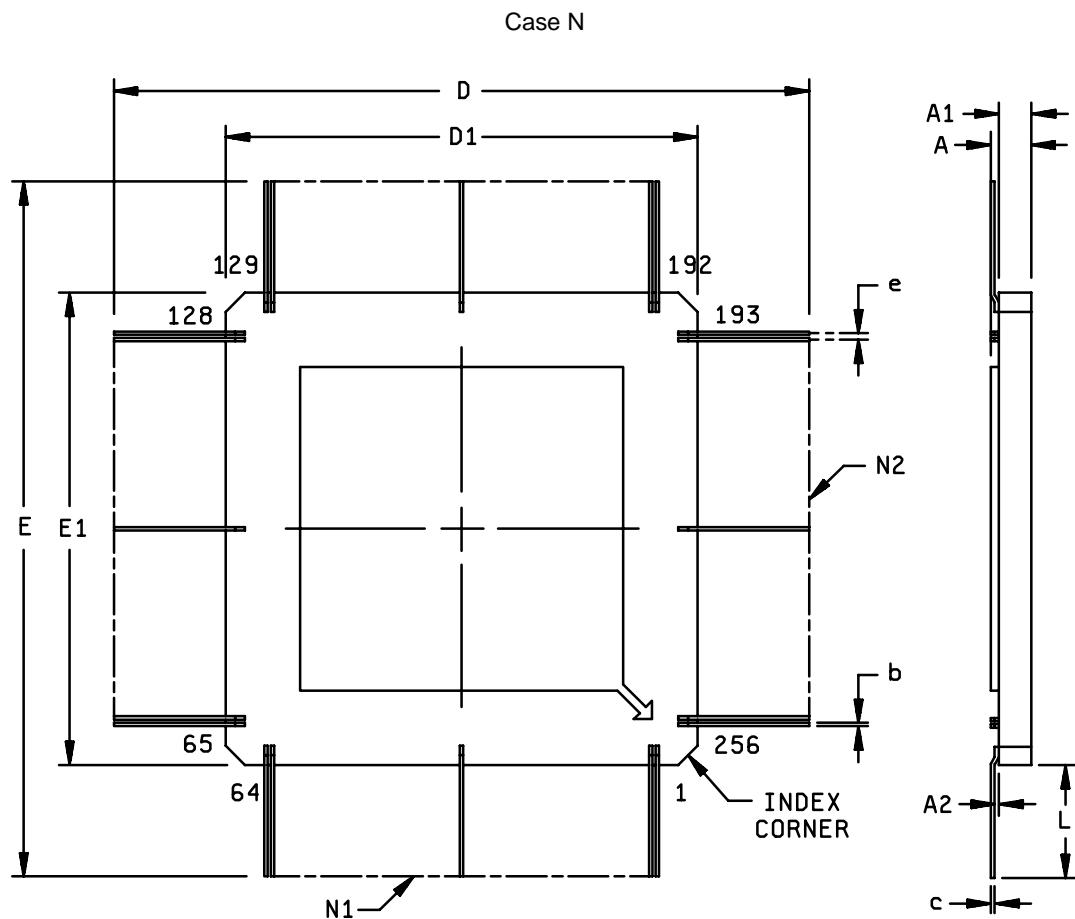
**STANDARD
MICROCIRCUIT DRAWING**
DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

SIZE
A

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REVISION LEVEL
D

SHEET
18



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.41	3.18	.095	.125
C	0.10	0.20	.004	.008
D/D1	53.23	55.74	2.095	2.195
E/E1	36.83	37.34	1.450	1.470
e	0.508 BSC		.020 BSC	
f	0.15	0.25	.006	.010
A1	2.06	2.56	.081	.101
A2	0.05	0.36	.002	.014
L	8.20	9.20	.323	.362
N1/N2	64		64	

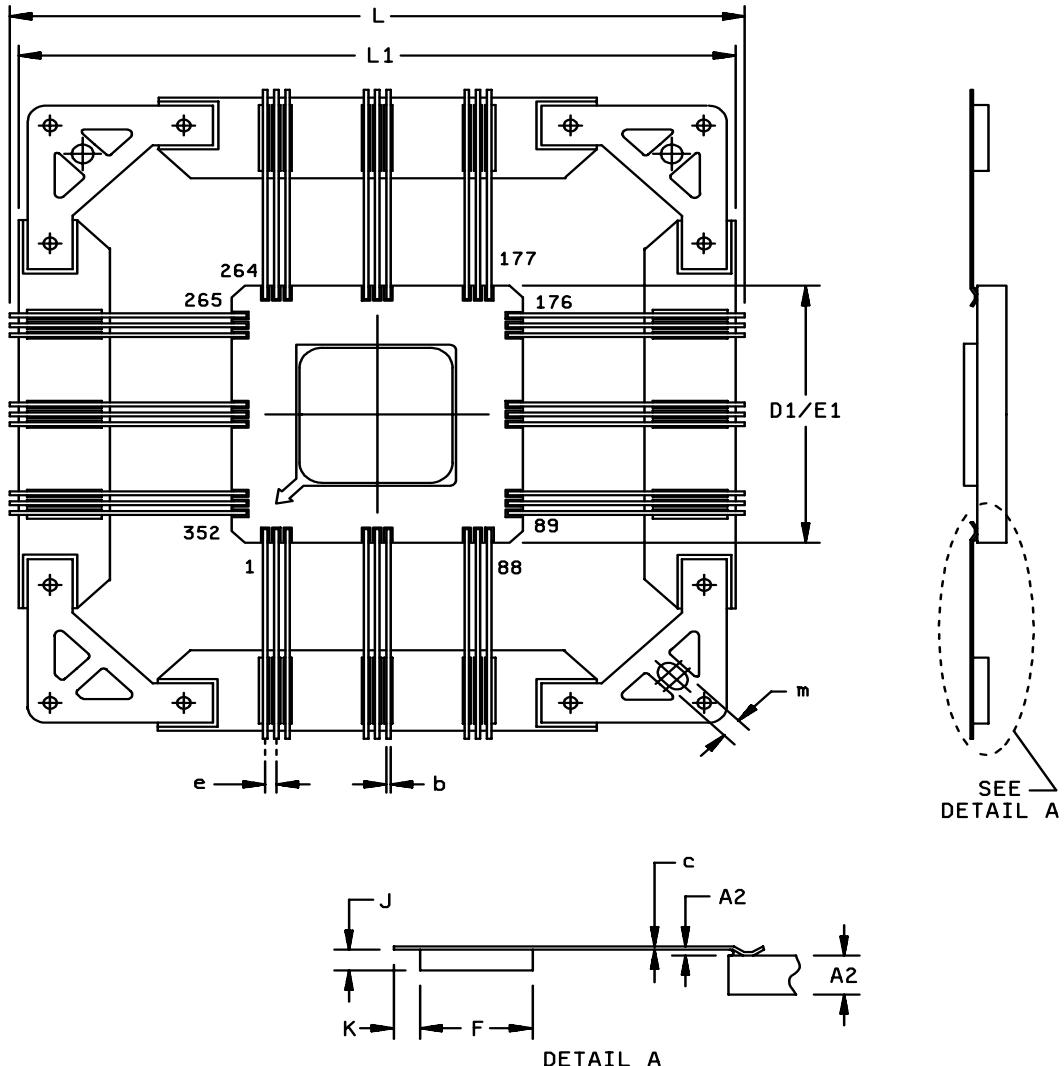
NOTE:

1. Lid is connected to ground.

FIGURE 1. Case Outline – Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A	5962-01B01
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CASE 4



Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A1	2.35	3.15	.092	.124	G	2.50	2.60	.098	.104
A2	0.05	0.35	.002	.014	J	0.75	1.05	.029	.041
b	0.19	0.25	.007	.010	K			0.50	
c	0.11	0.20	.004	.009	L	74.85	76.40	2.947	3.008
D1/E1	47.52	48.48	1.871	1.908	L1	74.60	75.40	2.937	2.969
e	0.50 Basic		.0196 Basic		m	2.50	2.65	.098	.104
F	4.50	5.50	.177	.217					

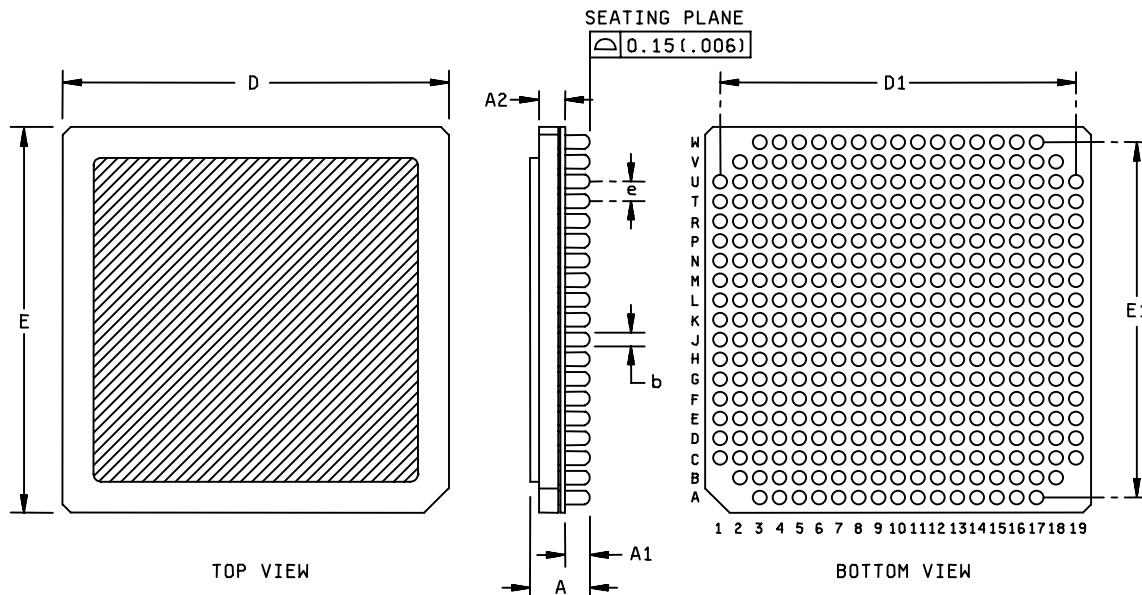
NOTE:

1. Lid is connected to ground.

FIGURE 1. Case Outline – Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A	5962-01B01
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Case 5



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	4.30	5.90	.169	.232
A1	1.40	1.85	.055	.073
A2	2.40	3.45	.094	.136
b	0.79	0.99	.031	.040
D/E	24.80	25.20	.976	.992
D1/E1	22.86 (1.27 x 18)		.900 (.05 x 18)	
e	1.27 REF		.050 REF	

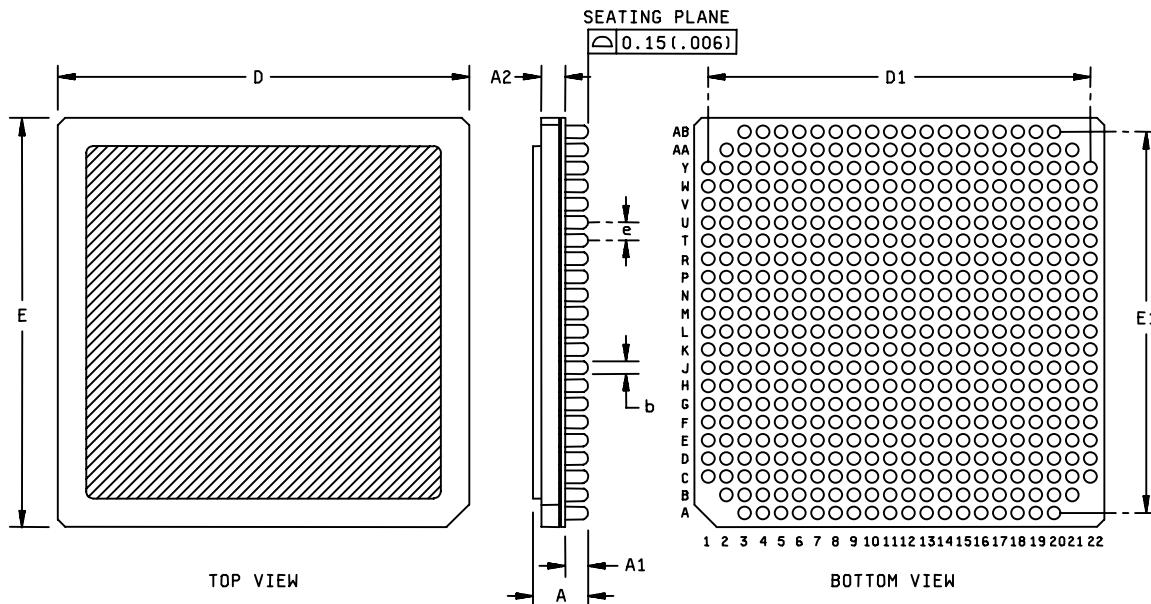
NOTES:

1. All dimensions and tolerance conform to ANSI Y14.5 – 1994.
2. Solder column position designation per JEDEC publication 95-1 standard procedures and practices SP-010.
3. "e" represents the basic solder column grid pitch.
4. Dimension b is measured at the maximum solder column diameter, parallel to primary datum.
5. Primary datum and seating plane are defined by the ends of the solder columns.
6. The A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, indentation, or other feature of package body, lid or integral heat slug.
7. Solder column array may be depopulated by any method, provided there is no pattern shifting. Depopulation is the omission of solder columns from a full matrix.
8. Lid is connected to ground.

Figure 1. Case Outline – Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A	5962-01B01
	REVISION LEVEL D	

Case 6



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	4.30	5.90	.169	.232
A1	1.40	1.85	.055	.073
A2	2.60	3.45	.102	.136
b	0.79	0.99	.031	.040
D/E	28.77	29.23	1.133	1.151
D1/E1	26.67 (1.27 x 21)		1.05 (.05 x 21)	
e	1.27 REF		.050 REF	

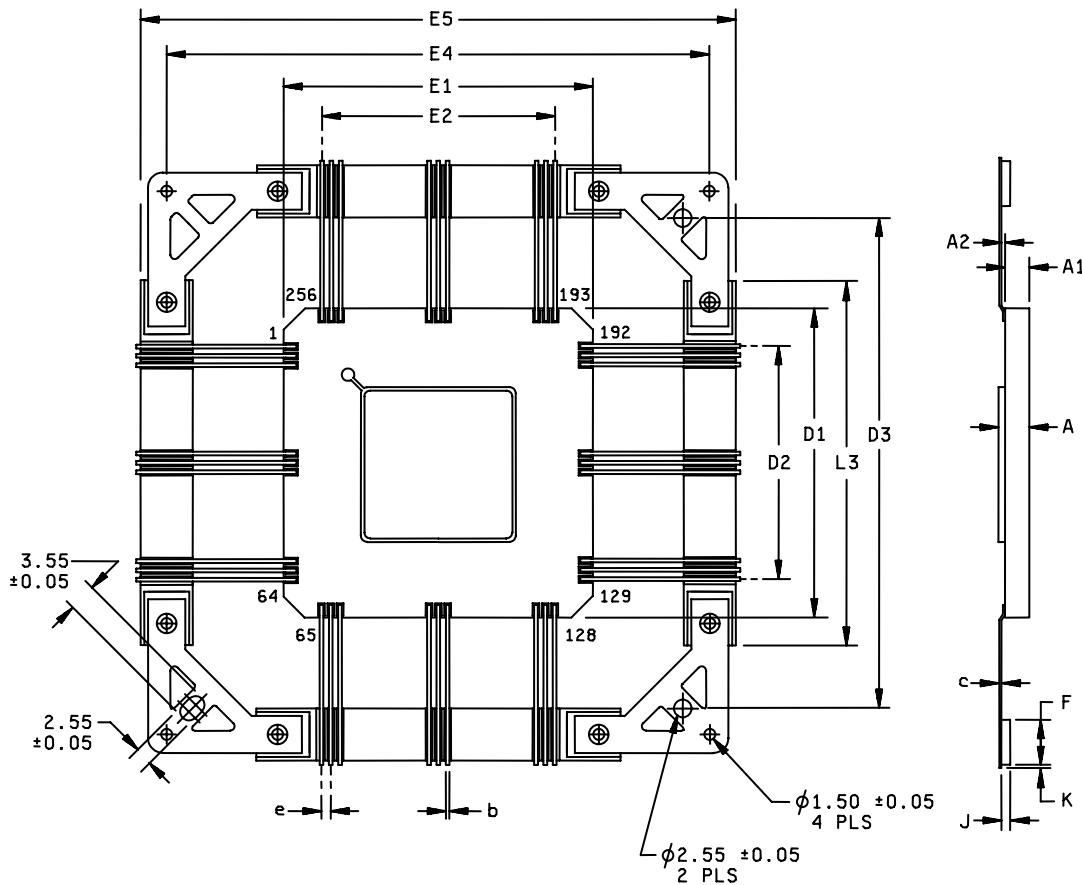
NOTES:

1. All dimensions and tolerance conform to ANSI Y14.5 – 1994.
2. Solder column position designation per JEDEC publication 95-1 standard procedures and practices SP-010.
3. "e" represents the basic solder column grid pitch.
4. Dimension b is measured at the maximum solder column diameter, parallel to primary datum.
5. Primary datum and seating plane are defined by the ends of the solder columns.
6. The A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, indentation, or other feature of package body, lid or integral heat slug.
7. Solder column array may be depopulated by any method, provided there is no pattern shifting. Depopulation is the omission of solder columns from a full matrix.
8. Lid is connected to ground.

Figure 1. Case Outline – Continued.

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Case 7



Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	2.50	3.22	.090	.127	E4	70.00 BSC		2.756 BSC	
A1	2.06	2.56	.001	.101	E5	74.60	75.40	2.937	2.968
A2	0.20 BSC		.008 BSC		e	0.50 BSC		.020 BSC	
b	0.20 TYP		.008 TYP		L3	56.30 BSC		2.217 BSC	
c	0.10	0.20	.004	.008	J	0.77	1.03	.030	.040
E1/D1	35.64	36.36	1.403	1.431	K		0.25		.010
E2/D2	31.50 BSC		1.240 BSC		F	7.05	8.45	.277	.332
D3	65.90 BSC		2.594 BSC						

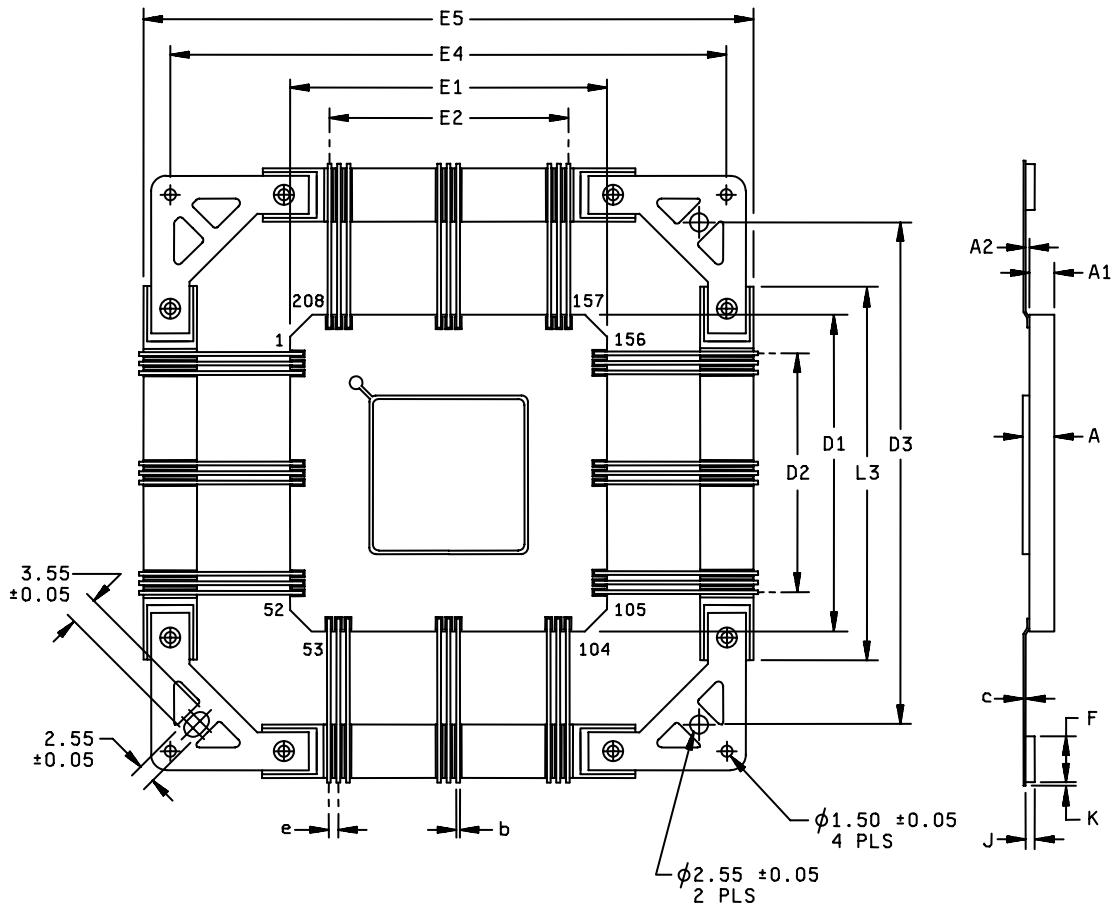
NOTE:

1. Lid is connected to ground.

FIGURE 1. Case Outline – Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A	5962-01B01
	REVISION LEVEL D	

Case 8



Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	2.40	3.20	.095	.126	E4	70.00 BSC		2.756 BSC	
A1	2.06	2.56	.001	.101	E5	74.60	75.40	2.937	2.968
A2	0.20 BSC		.008 BSC		e	0.50 BSC		.020 BSC	
b	0.20 TYP		.008 TYP		L3	56.30 BSC		2.217 BSC	
c	0.10	0.20	.004	.008	J	0.76	1.02	.030	.040
E1/D1	28.96	29.46	1.14	1.16	K		0.25		.010
E2/D2	25.50 BSC		1.004 BSC		F	7.05	8.45	.277	.332
D3	65.90 BSC		2.594 BSC						

NOTE:

1. Lid is connected to ground.

FIGURE 1. Case Outline – Continued.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) $T_A = +125^{\circ}\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535 appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

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TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,7,9	1,7,9	1,7,9
Final electrical parameters (see 4.2)	1,2,3,7,8,9,10,11 1/	1,2,3,7,8,9, 10,11 1/	1,2,3,7,8,9, 10,11 2/
Group A test requirements (see 4.4)	1,7,9	1,7,9	1,7,9
Group C end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1.

2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, D, or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
- b. $T_A = +125^\circ\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

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4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q, and V shall be as specified in MIL-I-38535.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$, after exposure, to the subgroups specified in table II herein.
- c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition "B" unless otherwise specified in the AID.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q will replace device class M.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

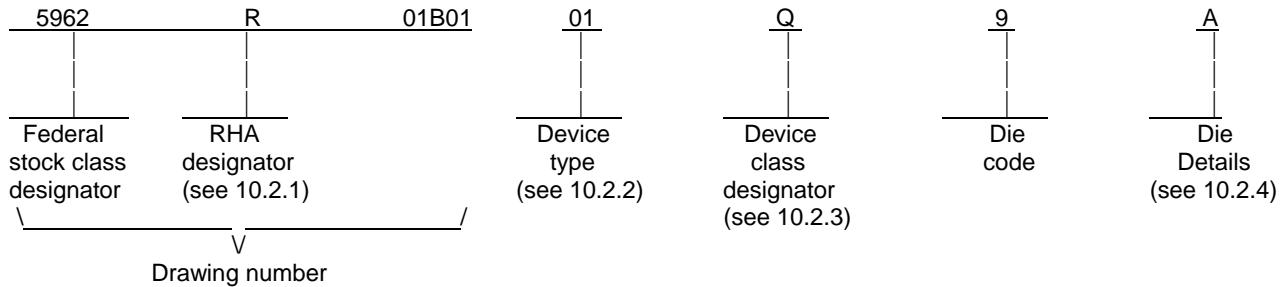
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10. SCOPE

10.1 **Scope.** This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QML plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

10.2 **PIN.** The PIN is as shown in the following example:



10.2.1 **RHA designator.** Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

10.2.2 **Device type(s).** The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	MH1099ER	988,000 sites available MH1RT
02	MH1156ER	1,558,000 sites available MH1RT
03	MH1242ER	2,422,000 sites available MH1RT
04	MH1332ER	3,319,000 sites available MH1RT
05	MH1099ES	988,000 sites available MH1RT
06	MH1156ES	1,558,000 sites available MH1RT
07	MH1242ES	2,422,000 sites available MH1RT
08	MH1332ES	3,319,000 sites available MH1RT
09	MH1M099ER	composite 988,000 sites MH1RT
10	MH1M156ER	composite 1,558,000 sites MH1RT
11	MH1M242ER	composite 2,422,000 sites MH1RT
12	MH1M332ER	composite 3,319,000 sites MH1RT
13	MH1M099ES	composite 988,000 sites MH1RT
14	MH1M156ES	composite 1,558,000 sites MH1RT
15	MH1M242ES	composite 2,422,000 sites MH1RT
16	MH1M332ES	composite 3,319,000 sites MH1RT

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<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
17	MH1099R	988,000 sites available MH1
18	MH1156R	1,558,000 sites available MH1
19	MH1242R	2,422,000 sites available MH1
20	MH1332R	3,319,000 sites available MH1
21	MH1099S	988,000 sites available MH1
22	MH1156S	1,558,000 sites available MH1
23	MH1242S	2,422,000 sites available MH1
24	MH1332S	3,319,000 sites available MH1
25	MH1M099R	composite 988,000 sites MH1
26	MH1M156R	composite 1,55,000 sites MH1
27	MH1M242R	composite 2,422,000 sites MH1
28	MH1M332R	composite 3,319,000 sites MH1
29	MH1M099S	composite 988,000 sites MH1
30	MH1M156S	composite 1,558,000 sites MH1
31	MH1M242S	composite 2,422,000 sites MH1
32	MH1M332S	composite 3,319,000 sites MH1

10.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

10.2.4. Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

10.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1
02	A-2
03	A-3
04	A-4 reserved – not yet available
05	A-1
06	A-2
07	A-3
08	A-4 reserved – not yet available
09	A-1
10	A-2
11	A-3
12	A-4 reserved – not yet available
13	A-1
14	A-2
15	A-3
16	A-4 reserved – not yet available

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Die type	Figure number
17	A-1
18	A-2
19	A-3
20	A-4 reserved – not yet available
21	A-1
22	A-2
23	A-3
24	A-4 reserved – not yet available
25	A-1
26	A-2
27	A-3
28	A-4 reserved – not yet available
29	A-1
30	A-2
31	A-3
32	A-4 reserved – not yet available

10.2.4.2. Die bonding pad locations and electrical functions.

Die type	Figure number
33	A-1
34	A-2
35	A-3
36	A-4 reserved – not yet available
37	A-1
38	A-2
39	A-3
40	A-4 reserved – not yet available
41	A-1
42	A-2
43	A-3
44	A-4 reserved – not yet available
45	A-1
46	A-2
47	A-3
48	A-4 reserved – not yet available
49	A-1
50	A-2
51	A-3
52	A-4 reserved – not yet available
53	A-1
54	A-2
55	A-3
56	A-4 reserved – not yet available
57	A-1
58	A-2
59	A-3
60	A-4 reserved – not yet available
61	A-1
62	A-2
63	A-3
64	A-4 reserved – not yet available

1/ Not yet available as die only

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10.2.4.3. Interface materials.

Die type	Figure number
65	A-1
66	A-2
67	A-3
68	A-4 reserved – not yet available
69	A-1
70	A-2
71	A-3
72	A-4 reserved – not yet available
73	A-1
74	A-2
75	A-3
76	A-4 reserved – not yet available
77	A-1
78	A-2
79	A-3
80	A-4 reserved – not yet available
81	A-1
82	A-2
83	A-3
84	A-4 reserved – not yet available
85	A-1
86	A-2
87	A-3
88	A-4 reserved – not yet available
89	A-1
90	A-2
91	A-3
92	A-4 reserved – not yet available
93	A-1
94	A-2
95	A-3
96	A-4 reserved – not yet available

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10.2.4.4. Assembly related information.

Die type	Figure number
97	A-1
98	A-2
99	A-3
100	A-4 reserved – not yet available
101	A-1
102	A-2
103	A-3
104	A-4 reserved – not yet available
105	A-1
106	A-2
107	A-3
108	A-4 reserved – not yet available
109	A-1
110	A-2
111	A-3
112	A-4 reserved – not yet available
113	A-1
114	A-2
115	A-3
116	A-4 reserved – not yet available
117	A-1
118	A-2
119	A-3
120	A-4 reserved – not yet available
121	A-1
122	A-2
123	A-3
124	A-4 reserved – not yet available
125	A-1
126	A-2
127	A-3
128	A-4 reserved – not yet available

10.3. Absolute maximum ratings. See paragraph 1.3 within the body of this drawing for details.

10.4 Recommended operating conditions. See paragraph 1.4 within the body of this drawing for details.

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20. APPLICABLE DOCUMENTS.

20.1 Government specifications, standards, and handbooks. . Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

20.2. Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

30. REQUIREMENTS

30.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit or function as described herein.

30.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

30.2.1 Die physical dimensions. The die physical dimensions shall be as specified in 10.2.4.1 and on figure A-1.

30.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in 10.2.4.2 and on figure A-1.

30.2.3 Interface materials. The interface materials for the die shall be as specified in 10.2.4.3 and on figure A-1.

30.2.4 Assembly related information. The assembly related information shall be as specified in 10.2.4.4 and figure A-1.

30.2.5 Truth table(s). The truth table(s) shall be as defined within paragraph 3.2.3. of the body of this document.

30.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined within paragraph 3.2.4. of the body of this document.

30.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

30.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

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30.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in 10.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

30.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 60.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

30.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

40. QUALITY ASSURANCE PROVISIONS

40.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not effect the form, fit or function as described herein.

40.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

- a) Wafer lot acceptance for Class V product using the criteria defined within H.3.2.3 as approved by the manufacturers TRB and the Qualifying activity.
- b) 100% wafer probe (see paragraph 30.4).
- c) 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883 test method 2010 or the alternate procedures allowed within MIL-STD-883 test method 5004.

40.3 Conformance inspection.

40.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see 30.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified within paragraphs 4.4.4.1, 4.4.4.1.1., 4.4.4.2, 4.4.4.3, 4.4.4.4 and 4.4.4.5.

50. DIE CARRIER

50.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

60 NOTES

60.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

60.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43216-5000 or telephone (614)-692-0547.

60.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined within MIL-PRF-38535 and MIL-STD-1331.

60.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see 30.6 herein) to DSCC-VA and have agreed to this drawing.

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Due to the complexity of the device , a graphical representation of the pad locations is not available .This figure shall be maintained and available from the device manufacturer.

See subsequent pages for a table of pad locations.

Die bonding pad locations and electrical functions – mask number 5542

Die physical dimensions.

Die size: 8 624 x 8 624 microns (with scribe line)

Die thickness: 475 microns

Interface materials.

Top metallization: Aluminium + Copper

Backside metallization: bare silicon

Glassivation.

Type: Oxinitride

Thickness: 21,000 Angstroms

Substrate: Single crystal silicon

Assembly related information.

Substrate potential: not connected

Special assembly instructions: None

Pads list :

1.	X	3866.5	Y	4090.5	21.	X	1966.7	Y	4090.5
2.	X	3771.5	Y	4090.5	22.	X	1871.7	Y	4090.5
3.	X	3676.5	Y	4090.5	23.	X	1776.7	Y	4090.5
4.	X	3581.6	Y	4090.5	24.	X	1681.8	Y	4090.5
5.	X	3486.6	Y	4090.5	25.	X	1586.8	Y	4090.5
6.	X	3391.6	Y	4090.5	26.	X	1491.8	Y	4090.5
7.	X	3296.6	Y	4090.5	27.	X	1396.8	Y	4090.5
8.	X	3201.6	Y	4090.5	28.	X	1301.8	Y	4090.5
9.	X	3106.6	Y	4090.5	29.	X	1206.8	Y	4090.5
10.	X	3011.6	Y	4090.5	30.	X	1111.8	Y	4090.5
11.	X	2916.6	Y	4090.5	31.	X	1016.8	Y	4090.5
12.	X	2821.6	Y	4090.5	32.	X	921.8	Y	4090.5
13.	X	2726.6	Y	4090.5	33.	X	826.8	Y	4090.5
14.	X	2631.7	Y	4090.5	34.	X	731.9	Y	4090.5
15.	X	2536.7	Y	4090.5	35.	X	636.9	Y	4090.5
16.	X	2441.7	Y	4090.5	36.	X	541.9	Y	4090.5
17.	X	2346.7	Y	4090.5	37.	X	446.9	Y	4090.5
18.	X	2251.7	Y	4090.5	38.	X	351.9	Y	4090.5
19.	X	2156.7	Y	4090.5	39.	X	256.9	Y	4090.5
20.	X	2061.7	Y	4090.5	40.	X	161.9	Y	4090.5

FIGURE A-1. Die bonding pad locations and electrical functions.

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Pads list :

121.	X -4090.5	Y 351.9	161.	X -4090.5	Y -3447.7
122.	X -4090.5	Y 256.9	162.	X -4090.5	Y -3542.7
123.	X -4090.5	Y 161.9	163.	X -4090.5	Y -3637.7
124.	X -4090.5	Y 66.9	164.	X -4090.5	Y -3732.7
125.	X -4090.5	Y -28.1	165.	X -4090.5	Y -3827.7
126.	X -4090.5	Y -123.1	166.	X -4090.5	Y -3922.7
127.	X -4090.5	Y -218.1	167.	X -3866.5	Y -4090.5
128.	X -4090.5	Y -313.0	168.	X -3771.5	Y -4090.5
129.	X -4090.5	Y -408.0	169.	X -3676.5	Y -4090.5
130.	X -4090.5	Y -503.0	170.	X -3581.6	Y -4090.5
131.	X -4090.5	Y -598.0	171.	X -3486.6	Y -4090.5
132.	X -4090.5	Y -693.0	172.	X -3391.6	Y -4090.5
133.	X -4090.5	Y -788.0	173.	X -3296.6	Y -4090.5
134.	X -4090.5	Y -883.0	174.	X -3201.6	Y -4090.5
135.	X -4090.5	Y -978.0	175.	X -3106.6	Y -4090.5
136.	X -4090.5	Y -1073.0	176.	X -3011.6	Y -4090.5
137.	X -4090.5	Y -1168.0	177.	X -2916.6	Y -4090.5
138.	X -4090.5	Y -1262.9	178.	X -2821.6	Y -4090.5
139.	X -4090.5	Y -1357.9	179.	X -2726.6	Y -4090.5
140.	X -4090.5	Y -1452.9	180.	X -2631.7	Y -4090.5
141.	X -4090.5	Y -1547.9	181.	X -2536.7	Y -4090.5
142.	X -4090.5	Y -1642.9	182.	X -2441.7	Y -4090.5
143.	X -4090.5	Y -1737.9	183.	X -2346.7	Y -4090.5
144.	X -4090.5	Y -1832.9	184.	X -2251.7	Y -4090.5
145.	X -4090.5	Y -1927.9	185.	X -2156.7	Y -4090.5
146.	X -4090.5	Y -2022.9	186.	X -2061.7	Y -4090.5
147.	X -4090.5	Y -2117.8	187.	X -1966.7	Y -4090.5
148.	X -4090.5	Y -2212.8	188.	X -1871.7	Y -4090.5
149.	X -4090.5	Y -2307.8	189.	X -1776.7	Y -4090.5
150.	X -4090.5	Y -2402.8	190.	X -1681.8	Y -4090.5
151.	X -4090.5	Y -2497.8	191.	X -1586.8	Y -4090.5
152.	X -4090.5	Y -2592.8	192.	X -1491.8	Y -4090.5
153.	X -4090.5	Y -2687.8	193.	X -1396.8	Y -4090.5
154.	X -4090.5	Y -2782.8	194.	X -1301.8	Y -4090.5
155.	X -4090.5	Y -2877.8	195.	X -1206.8	Y -4090.5
156.	X -4090.5	Y -2972.8	196.	X -1111.8	Y -4090.5
157.	X -4090.5	Y -3067.8	197.	X -1016.8	Y -4090.5
158.	X -4090.5	Y -3162.7	198.	X -921.8	Y -4090.5
159.	X -4090.5	Y -3257.7	199.	X -826.8	Y -4090.5
160.	X -4090.5	Y -3352.7	200.	X -731.9	Y -4090.5

FIGURE A-1. Die bonding pad locations and electrical functions - Continued.

STANDARD MICROCIRCUIT DRAWING <small>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000</small>	SIZE A		5962-01B01
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Pads list :

281.	X	4090.5	Y	-921.8	311.	X	4090.5	Y	1927.9
282.	X	4090.5	Y	-826.8	312.	X	4090.5	Y	2022.9
283.	X	4090.5	Y	-731.9	313.	X	4090.5	Y	2117.8
284.	X	4090.5	Y	-636.9	314.	X	4090.5	Y	2212.8
285.	X	4090.5	Y	-541.9	315.	X	4090.5	Y	2307.8
286.	X	4090.5	Y	-446.9	316.	X	4090.5	Y	2402.8
287.	X	4090.5	Y	-351.9	317.	X	4090.5	Y	2497.8
288.	X	4090.5	Y	-256.9	318.	X	4090.5	Y	2592.8
289.	X	4090.5	Y	-161.9	319.	X	4090.5	Y	2687.8
290.	X	4090.5	Y	-66.9	320.	X	4090.5	Y	2782.8
291.	X	4090.5	Y	28.1	321.	X	4090.5	Y	2877.8
292.	X	4090.5	Y	123.1	322.	X	4090.5	Y	2972.8
293.	X	4090.5	Y	218.1	323.	X	4090.5	Y	3067.8
294.	X	4090.5	Y	313.0	324.	X	4090.5	Y	3162.7
295.	X	4090.5	Y	408.0	325.	X	4090.5	Y	3257.7
296.	X	4090.5	Y	503.0	326.	X	4090.5	Y	3352.7
297.	X	4090.5	Y	598.0	327.	X	4090.5	Y	3447.7
298.	X	4090.5	Y	693.0	328.	X	4090.5	Y	3542.7
299.	X	4090.5	Y	788.0	329.	X	4090.5	Y	3637.7
300.	X	4090.5	Y	883.0	330.	X	4090.5	Y	3732.7
301.	X	4090.5	Y	978.0	331.	X	4090.5	Y	3827.7
302.	X	4090.5	Y	1073.0	332.	X	4090.5	Y	3922.7
303.	X	4090.5	Y	1168.0					
304.	X	4090.5	Y	1262.9					
305.	X	4090.5	Y	1357.9					
306.	X	4090.5	Y	1452.9					
307.	X	4090.5	Y	1547.9					
308.	X	4090.5	Y	1642.9					
309.	X	4090.5	Y	1737.9					
310.	X	4090.5	Y	1832.9					

FIGURE A-1. Die bonding pad locations and electrical functions - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A	REVISION LEVEL D	5962-01B01
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APPENDIX A FORMS A PART OF SMD 5962-01B01

Due to the complexity of the device , a graphical representation of the pad locations is not available .This figure shall be maintained and available from the device manufacturer.

See subsequent pages for a table of pad locations.

Die bonding pad locations and electrical functions – mask number 5543

Die physical dimensions.

Die size: 10 528 x 10 528 microns (with scribe line)

Die thickness: 475 microns

Interface materials.

Top metallization: Aluminium + Copper

Backside metallization: bare silicon

Glassivation.

Type: Oxinitride

Thickness: 21,000 Angstroms

Substrate: Single crystal silicon

Assembly related information.

Substrate potential: not connected

Special assembly instructions: None

Pads list :

1.	X	4816.4	Y	5040.4	11.	X	3866.5	Y	5040.4
2.	X	4721.4	Y	5040.4	12.	X	3771.5	Y	5040.4
3.	X	4626.4	Y	5040.4	13.	X	3676.5	Y	5040.4
4.	X	4531.4	Y	5040.4	14.	X	3581.6	Y	5040.4
5.	X	4436.5	Y	5040.4	15.	X	3486.6	Y	5040.4
6.	X	4341.5	Y	5040.4	16.	X	3391.6	Y	5040.4
7.	X	4246.5	Y	5040.4	17.	X	3296.6	Y	5040.4
8.	X	4151.5	Y	5040.4	18.	X	3201.6	Y	5040.4
9.	X	4056.5	Y	5040.4	19.	X	3106.6	Y	5040.4
10.	X	3961.5	Y	5040.4	20.	X	3011.6	Y	5040.4

FIGURE A-2. Die bonding pad locations and electrical functions.

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APPENDIX A FORMS A PART OF SMD 5962-01B01

Due to the complexity of the device , a graphical representation of the pad locations is not available .This figure shall be maintained and available from the device manufacturer.

See subsequent pages for a table of pad locations.

Die bonding pad locations and electrical functions – mask number 5544

Die physical dimensions.

Die size: 13 097 x 13 097 microns (with scribe line)

Die thickness: 475 microns

Interface materials.

Top metallization: Aluminium + Copper

Backside metallization: bare silicon

Glassivation.

Type: Oxinitride

Thickness: 21,000 Angstroms

Substrate: Single crystal silicon

Assembly related information.

Substrate potential: not connected

Special assembly instructions: None

Pads list :

1.	X	6003.8	Y	6227.8	11.	X	5053.9	Y	6227.8
2.	X	5908.8	Y	6227.8	12.	X	4958.9	Y	6227.8
3.	X	5813.8	Y	6227.8	13.	X	4863.9	Y	6227.8
4.	X	5718.8	Y	6227.8	14.	X	4768.9	Y	6227.8
5.	X	5623.8	Y	6227.8	15.	X	4673.9	Y	6227.8
6.	X	5528.8	Y	6227.8	16.	X	4578.9	Y	6227.8
7.	X	5433.9	Y	6227.8	17.	X	4484.0	Y	6227.8
8.	X	5338.9	Y	6227.8	18.	X	4389.0	Y	6227.8
9.	X	5243.9	Y	6227.8	19.	X	4294.0	Y	6227.8
10.	X	5148.9	Y	6227.8	20.	X	4199.0	Y	6227.8

FIGURE A-3. Die bonding pad locations and electrical functions .

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Pads list :

181.	X	-6227.8	Y	1064.3	221.	X	-6227.8	Y	-2735.3
182.	X	-6227.8	Y	969.3	222.	X	-6227.8	Y	-2830.3
183.	X	-6227.8	Y	874.3	223.	X	-6227.8	Y	-2925.3
184.	X	-6227.8	Y	779.3	224.	X	-6227.8	Y	-3020.3
185.	X	-6227.8	Y	684.4	225.	X	-6227.8	Y	-3115.2
186.	X	-6227.8	Y	589.4	226.	X	-6227.8	Y	-3210.2
187.	X	-6227.8	Y	494.4	227.	X	-6227.8	Y	-3305.2
188.	X	-6227.8	Y	399.4	228.	X	-6227.8	Y	-3400.2
189.	X	-6227.8	Y	304.4	229.	X	-6227.8	Y	-3495.2
190.	X	-6227.8	Y	209.4	230.	X	-6227.8	Y	-3590.2
191.	X	-6227.8	Y	114.4	231.	X	-6227.8	Y	-3685.2
192.	X	-6227.8	Y	19.4	232.	X	-6227.8	Y	-3780.2
193.	X	-6227.8	Y	-75.6	233.	X	-6227.8	Y	-3875.2
194.	X	-6227.8	Y	-170.6	234.	X	-6227.8	Y	-3970.2
195.	X	-6227.8	Y	-265.5	235.	X	-6227.8	Y	-4065.1
196.	X	-6227.8	Y	-360.5	236.	X	-6227.8	Y	-4160.1
197.	X	-6227.8	Y	-455.5	237.	X	-6227.8	Y	-4255.1
198.	X	-6227.8	Y	-550.5	238.	X	-6227.8	Y	-4350.1
199.	X	-6227.8	Y	-645.5	239.	X	-6227.8	Y	-4445.1
200.	X	-6227.8	Y	-740.5	240.	X	-6227.8	Y	-4540.1
201.	X	-6227.8	Y	-835.5	241.	X	-6227.8	Y	-4635.1
202.	X	-6227.8	Y	-930.5	242.	X	-6227.8	Y	-4730.1
203.	X	-6227.8	Y	-1025.5	243.	X	-6227.8	Y	-4825.1
204.	X	-6227.8	Y	-1120.5	244.	X	-6227.8	Y	-4920.1
205.	X	-6227.8	Y	-1215.4	245.	X	-6227.8	Y	-5015.0
206.	X	-6227.8	Y	-1310.4	246.	X	-6227.8	Y	-5110.0
207.	X	-6227.8	Y	-1405.4	247.	X	-6227.8	Y	-5205.0
208.	X	-6227.8	Y	-1500.4	248.	X	-6227.8	Y	-5300.0
209.	X	-6227.8	Y	-1595.4	249.	X	-6227.8	Y	-5395.0
210.	X	-6227.8	Y	-1690.4	250.	X	-6227.8	Y	-5490.0
211.	X	-6227.8	Y	-1785.4	251.	X	-6227.8	Y	-5585.0
212.	X	-6227.8	Y	-1880.4	252.	X	-6227.8	Y	-5680.0
213.	X	-6227.8	Y	-1975.4	253.	X	-6227.8	Y	-5775.0
214.	X	-6227.8	Y	-2070.4	254.	X	-6227.8	Y	-5870.0
215.	X	-6227.8	Y	-2165.3	255.	X	-6227.8	Y	-5964.9
216.	X	-6227.8	Y	-2260.3	256.	X	-6227.8	Y	-6059.9
217.	X	-6227.8	Y	-2355.3	257.	X	-6003.8	Y	-6227.8
218.	X	-6227.8	Y	-2450.3	258.	X	-5908.8	Y	-6227.8
219.	X	-6227.8	Y	-2545.3	259.	X	-5813.8	Y	-6227.8
220.	X	-6227.8	Y	-2640.3	260.	X	-5718.8	Y	-6227.8

FIGURE A-3. Die bonding pad locations and electrical functions - Continued.

**STANDARD
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 DEFENSE SUPPLY CENTER COLUMBUS
 COLUMBUS, OHIO 43216-5000

**SIZE
A**

5962-01B01

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APPENDIX A FORMS A PART OF SMD 5962-01B01

Pads list :

261.	X -5623.8	Y -6227.8	301.	X -1824.2	Y -6227.8
262.	X -5528.8	Y -6227.8	302.	X -1729.2	Y -6227.8
263.	X -5433.9	Y -6227.8	303.	X -1634.3	Y -6227.8
264.	X -5338.9	Y -6227.8	304.	X -1539.3	Y -6227.8
265.	X -5243.9	Y -6227.8	305.	X -1444.3	Y -6227.8
266.	X -5148.9	Y -6227.8	306.	X -1349.3	Y -6227.8
267.	X -5053.9	Y -6227.8	307.	X -1254.3	Y -6227.8
268.	X -4958.9	Y -6227.8	308.	X -1159.3	Y -6227.8
269.	X -4863.9	Y -6227.8	309.	X -1064.3	Y -6227.8
270.	X -4768.9	Y -6227.8	310.	X -969.3	Y -6227.8
271.	X -4673.9	Y -6227.8	311.	X -874.3	Y -6227.8
272.	X -4578.9	Y -6227.8	312.	X -779.3	Y -6227.8
273.	X -4484.0	Y -6227.8	313.	X -684.4	Y -6227.8
274.	X -4389.0	Y -6227.8	314.	X -589.4	Y -6227.8
275.	X -4294.0	Y -6227.8	315.	X -494.4	Y -6227.8
276.	X -4199.0	Y -6227.8	316.	X -399.4	Y -6227.8
277.	X -4104.0	Y -6227.8	317.	X -304.4	Y -6227.8
278.	X -4009.0	Y -6227.8	318.	X -209.4	Y -6227.8
279.	X -3914.0	Y -6227.8	319.	X -114.4	Y -6227.8
280.	X -3819.0	Y -6227.8	320.	X -19.4	Y -6227.8
281.	X -3724.0	Y -6227.8	321.	X 75.6	Y -6227.8
282.	X -3629.0	Y -6227.8	322.	X 170.6	Y -6227.8
283.	X -3534.1	Y -6227.8	323.	X 265.5	Y -6227.8
284.	X -3439.1	Y -6227.8	324.	X 360.5	Y -6227.8
285.	X -3344.1	Y -6227.8	325.	X 455.5	Y -6227.8
286.	X -3249.1	Y -6227.8	326.	X 550.5	Y -6227.8
287.	X -3154.1	Y -6227.8	327.	X 645.5	Y -6227.8
288.	X -3059.1	Y -6227.8	328.	X 740.5	Y -6227.8
289.	X -2964.1	Y -6227.8	329.	X 835.5	Y -6227.8
290.	X -2869.1	Y -6227.8	330.	X 930.5	Y -6227.8
291.	X -2774.1	Y -6227.8	331.	X 1025.5	Y -6227.8
292.	X -2679.1	Y -6227.8	332.	X 1120.5	Y -6227.8
293.	X -2584.2	Y -6227.8	333.	X 1215.4	Y -6227.8
294.	X -2489.2	Y -6227.8	334.	X 1310.4	Y -6227.8
295.	X -2394.2	Y -6227.8	335.	X 1405.4	Y -6227.8
296.	X -2299.2	Y -6227.8	336.	X 1500.4	Y -6227.8
297.	X -2204.2	Y -6227.8	337.	X 1595.4	Y -6227.8
298.	X -2109.2	Y -6227.8	338.	X 1690.4	Y -6227.8
299.	X -2014.2	Y -6227.8	339.	X 1785.4	Y -6227.8
300.	X -1919.2	Y -6227.8	340.	X 1880.4	Y -6227.8

FIGURE A-3. Die bonding pad locations and electrical functions - Continued.

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Pads list :

341.	X	1975.4	Y	-6227.8	381.	X	5775.0	Y	-6227.8
342.	X	2070.4	Y	-6227.8	382.	X	5870.0	Y	-6227.8
343.	X	2165.3	Y	-6227.8	383.	X	5964.9	Y	-6227.8
344.	X	2260.3	Y	-6227.8	384.	X	6059.9	Y	-6227.8
345.	X	2355.3	Y	-6227.8	385.	X	6227.8	Y	-6003.8
346.	X	2450.3	Y	-6227.8	386.	X	6227.8	Y	-5908.8
347.	X	2545.3	Y	-6227.8	387.	X	6227.8	Y	-5813.8
348.	X	2640.3	Y	-6227.8	388.	X	6227.8	Y	-5718.8
349.	X	2735.3	Y	-6227.8	389.	X	6227.8	Y	-5623.8
350.	X	2830.3	Y	-6227.8	390.	X	6227.8	Y	-5528.8
351.	X	2925.3	Y	-6227.8	391.	X	6227.8	Y	-5433.9
352.	X	3020.3	Y	-6227.8	392.	X	6227.8	Y	-5338.9
353.	X	3115.2	Y	-6227.8	393.	X	6227.8	Y	-5243.9
354.	X	3210.2	Y	-6227.8	394.	X	6227.8	Y	-5148.9
355.	X	3305.2	Y	-6227.8	395.	X	6227.8	Y	-5053.9
356.	X	3400.2	Y	-6227.8	396.	X	6227.8	Y	-4958.9
357.	X	3495.2	Y	-6227.8	397.	X	6227.8	Y	-4863.9
358.	X	3590.2	Y	-6227.8	398.	X	6227.8	Y	-4768.9
359.	X	3685.2	Y	-6227.8	399.	X	6227.8	Y	-4673.9
360.	X	3780.2	Y	-6227.8	400.	X	6227.8	Y	-4578.9
361.	X	3875.2	Y	-6227.8	401.	X	6227.8	Y	-4484.0
362.	X	3970.2	Y	-6227.8	402.	X	6227.8	Y	-4389.0
363.	X	4065.1	Y	-6227.8	403.	X	6227.8	Y	-4294.0
364.	X	4160.1	Y	-6227.8	404.	X	6227.8	Y	-4199.0
365.	X	4255.1	Y	-6227.8	405.	X	6227.8	Y	-4104.0
366.	X	4350.1	Y	-6227.8	406.	X	6227.8	Y	-4009.0
367.	X	4445.1	Y	-6227.8	407.	X	6227.8	Y	-3914.0
368.	X	4540.1	Y	-6227.8	408.	X	6227.8	Y	-3819.0
369.	X	4635.1	Y	-6227.8	409.	X	6227.8	Y	-3724.0
370.	X	4730.1	Y	-6227.8	410.	X	6227.8	Y	-3629.0
371.	X	4825.1	Y	-6227.8	411.	X	6227.8	Y	-3534.1
372.	X	4920.1	Y	-6227.8	412.	X	6227.8	Y	-3439.1
373.	X	5015.0	Y	-6227.8	413.	X	6227.8	Y	-3344.1
374.	X	5110.0	Y	-6227.8	414.	X	6227.8	Y	-3249.1
375.	X	5205.0	Y	-6227.8	415.	X	6227.8	Y	-3154.1
376.	X	5300.0	Y	-6227.8	416.	X	6227.8	Y	-3059.1
377.	X	5395.0	Y	-6227.8	417.	X	6227.8	Y	-2964.1
378.	X	5490.0	Y	-6227.8	418.	X	6227.8	Y	-2869.1
379.	X	5585.0	Y	-6227.8	419.	X	6227.8	Y	-2774.1
380.	X	5680.0	Y	-6227.8	420.	X	6227.8	Y	-2679.1

FIGURE A-3. Die bonding pad locations and electrical functions - Continued.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-01-24

Approved sources of supply for SMD 5962-01B01 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor Similar PIN <u>2/ 3/</u>
5962-01B0101QZC	F7400	TH1099ERHabcYCMQ
5962-01B0101QYC	F7400	TH1099ERHabcKZMQ
5962-01B0101QXC	F7400	TH1099ERHabcK9MQ
5962-01B0101QUB	F7400	TH1099ERHabc2EMQ
5962-01B0101Q4C	F7400	TH1099ERHabcYFMQ
5962-01B0101QNC	F7400	TH1099ERHabcKAMQ
5962-01B0101QMC	F7400	TH1099ERHabcKBMQ
5962-01B0101Q5B	F7400	TH1099ERHabc2HMQ
5962-01B0101Q9A	F7400	TH1099ERHabcDDMQ
5962-01B0101VZC	F7400	TH1099ERHabcYCSV
5962-01B0101VYC	F7400	TH1099ERHabcKZSV
5962-01B0101VXC	F7400	TH1099ERHabcK9SV
5962-01B0101VUB	F7400	TH1099ERHabc2ESV
5962-01B0101V4C	F7400	TH1099ERHabcYFSV
5962-01B0101VNC	F7400	TH1099ERHabcKASV
5962-01B0101VMC	F7400	TH1099ERHabcKBSV
5962-01B0101V5B	F7400	TH1099ERHabc2HSV
5962-01B0101V9A	F7400	TH1099ERHabcDDSV
5962R01B0101VZC	F7400	TH1099ERHabcYCSR
5962R01B0101VYC	F7400	TH1099ERHabcKZSR
5962R01B0101VXC	F7400	TH1099ERHabcK9SR
5962R01B0101VUB	F7400	TH1099ERHabc2ESR
5962R01B0101V4C	F7400	TH1099ERHabcYFSR
5962R01B0101VNC	F7400	TH1099ERHabcKASR
5962R01B0101VMC	F7400	TH1099ERHabcKBSR
5962R01B0101V5B	F7400	TH1099ERHabc2HSR
5962-01B0102QZC	F7400	TH1156ERHabcYCMQ
5962-01B0102QYC	F7400	TH1156ERHabcKZMQ
5962-01B0102QTB	F7400	TH1156ERHabc2CMQ
5962-01B0102QUB	F7400	TH1156ERHabc2EMQ
5962-01B0102Q4C	F7400	TH1156ERHabcYFMQ
5962-01B0102QNC	F7400	TH1156ERHabcKAMQ
5962-01B0102Q6B	F7400	TH1156ERHabc2GMQ
5962-01B0102Q5B	F7400	TH1156ERHabc2HMQ
5962-01B0102Q9A	F7400	TH1156ERHabcDDMQ
5962-01B0102VZC	F7400	TH1156ERHabcYCSV
5962-01B0102VYC	F7400	TH1156ERHabcKZSV
5962-01B0102VTB	F7400	TH1156ERHabc2CSV
5962-01B0102VUB	F7400	TH1156ERHabc2ESV
5962-01B0102V4C	F7400	TH1156ERHabcYFSV
5962-01B0102VNC	F7400	TH1156ERHabcKASV

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor Similar PIN 2/ 3/
5962-01B0102V6B	F7400	TH1156ERHabc2GSV
5962-01B0102V5B	F7400	TH1156ERHabc2HSV
5962-01B0102V9A	F7400	TH1156ERHabcDDSV
5962R01B0102VZC	F7400	TH1156ERHabcYCSR
5962R01B0102VYC	F7400	TH156ERHabcKZSR
5962R01B0102VTB	F7400	TH1156ERHabc2CSR
5962R01B0102VUB	F7400	TH1156ERHabc2ESR
5962R01B0102V4C	F7400	TH1156ERHabcYFSR
5962R01B0102VNC	F7400	TH156ERHabcKASR
5962R01B0102V6B	F7400	TH1156ERHabc2GSR
5962R01B0102V5B	F7400	TH1156ERHabc2HSR
5962-01B0103QZC	F7400	TH1242ERHabcYCMQ
5962-01B0103QYC	F7400	TH1242ERHabcKZMQ
5962-01B0103QTB	F7400	TH1242ERHabc2CMQ
5962-01B0103QUB	F7400	TH1242ERHabc2EMQ
5962-01B0103Q4C	F7400	TH1242ERHabcYFMQ
5962-01B0103QNC	F7400	TH1242ERHabcKAMQ
5962-01B0103Q6B	F7400	TH1242ERHabc2GMQ
5962-01B0103Q5B	F7400	TH1242ERHabc2HMQ
5962-01B0103Q9A	F7400	TH1242ERHabcDDMQ
5962-01B0103VZC	F7400	TH1242ERHabcYCSV
5962-01B0103VYC	F7400	TH1242RHabcKZSV
5962-01B0103VTB	F7400	TH1242ERHabc2CSV
5962-01B0103VUB	F7400	TH1242ERHabc2ESV
5962-01B0103V4C	F7400	TH1242ERHabcYFSV
5962-01B0103VNC	F7400	TH1242RHabcKASV
5962-01B0103V6B	F7400	TH1242ERHabc2GSV
5962-01B0103V5B	F7400	TH1242ERHabc2HSV
5962-01B0103V9A	F7400	TH1242ERHabcDDSV
5962R01B0103VZC	F7400	TH1242ERHabcYCSR
5962R01B0103VYC	F7400	TH1242ERHabcKZSR
5962R01B0103VTB	F7400	TH1242ERHabc2CSR
5962R01B0103VUB	F7400	TH1242ERHabc2ESR
5962R01B0103V4C	F7400	TH1242ERHabcYFSR
5962R01B0103VNC	F7400	TH1242ERHabcKASR
5962R01B0103V6B	F7400	TH1242ERHabc2GSR
5962R01B0103V5B	F7400	TH1242ERHabc2HSR
5962-01B0104QZC	F7400	TH1332ERHabcYCMQ
5962-01B0104QTB	F7400	TH1332ERHabc2CMQ
5962-01B0104Q4C	F7400	TH1332ERHabcYFMQ
5962-01B0104Q6B	F7400	TH1332ERHabc2GMQ
5962-01B0104Q9A	F7400	TH1332ERHabcDDMQ
5962-01B0104VZC	F7400	TH1332ERHabcYCSV
5962-01B0104VTB	F7400	TH1332ERHabc2CSV
5962-01B0104V4C	F7400	TH1332ERHabcYFSV
5962-01B0104V6B	F7400	TH1332ERHabc2GSV
5962-01B0104V9A	F7400	TH1332ERHabcDDSV

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor Similar PIN 2/ 3/
5962R01B0104VZC	F7400	TH1332ERHabcYCSR
5962R01B0104VTB	F7400	TH1332ERHabc2CSR
5962R01B0104V4C	F7400	TH1332ERHabcYFSR
5962R01B0104V6B	F7400	TH1332ERHabc2GSR
5962-01B0105QZC	F7400	TH1099ESHabcYCMQ
5962-01B0105QYC	F7400	TH1099ESHabcKZMQ
5962-01B0105QXC	F7400	TH1099ESHabcK9MQ
5962-01B0105QUB	F7400	TH1099ESHabc2EMQ
5962-01B0105Q4C	F7400	TH1099ESHabcYFMQ
5962-01B0105QNC	F7400	TH1099ESHabcKAMQ
5962-01B0105QMC	F7400	TH1099ESHabcKBMQ
5962-01B0105Q5B	F7400	TH1099ESHabc2HMQ
5962-01B0105Q9A	F7400	TH1099ESHabcDDMQ
5962-01B0105VZC	F7400	TH1099ESHabcYCSV
5962-01B0105VYC	F7400	TH1099ESHabcKZSV
5962-01B0105VXC	F7400	TH1099ESHabcK9SV
5962-01B0105VUB	F7400	TH1099ESHabc2ESV
5962-01B0105V4C	F7400	TH1099ESHabcYFSV
5962-01B0105VNC	F7400	TH1099ESHabcKASV
5962-01B0105VMC	F7400	TH1099ESHabcKBSV
5962-01B0105V5B	F7400	TH1099ESHabc2HSV
5962-01B0105V9A	F7400	TH1099ESHabcDDSV
5962R01B0105VZC	F7400	TH1099ESHabcYCSR
5962R01B0105VYC	F7400	TH1099ESHabcKZSR
5962R01B0105VXC	F7400	TH1099ESHabcK9SR
5962R01B0105VUB	F7400	TH1099ESHabc2ESR
5962R01B0105V4C	F7400	TH1099ESHabcYFSR
5962R01B0105VNC	F7400	TH1099ESHabcKASR
5962R01B0105VMC	F7400	TH1099ESHabcKBSR
5962R01B0105V5B	F7400	TH1099ESHabc2HSR
5962-01B0106QZC	F7400	TH1156ESHabcYCMQ
5962-01B0106QYC	F7400	TH1156ESHabcKZMQ
5962-01B0106QTB	F7400	TH1156ESHabc2CMQ
5962-01B0106QUB	F7400	TH1156ESHabc2EMQ
5962-01B0106Q4C	F7400	TH1156ESHabcYFMQ
5962-01B0106QNC	F7400	TH1156ESHabcKAMQ
5962-01B0106Q6B	F7400	TH1156ESHabc2GMQ
5962-01B0106Q5B	F7400	TH1156ESHabc2HMQ
5962-01B0106Q9A	F7400	TH1156ESHabcDDMQ
5962-01B0106VZC	F7400	TH1156ESHabcYCSV
5962-01B0106VYC	F7400	TH1156ESHabcKZSV
5962-01B0106VTB	F7400	TH1156ESHabc2CSV
5962-01B0106VUB	F7400	TH1156ESHabc2ESV
5962-01B0106V4C	F7400	TH1156ESHabcYFSV
5962-01B0106VNC	F7400	TH1156ESHabcKASV
5962-01B0106V6B	F7400	TH1156ESHabc2GSV
5962-01B0106V5B	F7400	TH1156ESHabc2HSV

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor Similar PIN 2/ 3/
5962-01B0106V9A	F7400	TH1156ESHabcDDSV
5962R01B0106VZC	F7400	TH1156ESHabcYCSR
5962R01B0106VYC	F7400	TH1156ESHabcKZSR
5962R01B0106VTB	F7400	TH1156ESHabc2CSR
5962R01B0106VUB	F7400	TH1156ESHabc2ESR
5962R01B0106V4C	F7400	TH1156ESHabcYFSR
5962R01B0106VNC	F7400	TH1156ESHabcKASR
5962R01B0106V6B	F7400	TH1156ESHabc2GSR
5962R01B0106V5B	F7400	TH1156ESHabc2HSR
5962-01B0107QZC	F7400	TH1242ESHabcYCMQ
5962-01B0107QYC	F7400	TH1242ESHabcKZMQ
5962-01B0107QTB	F7400	TH1242ESHabc2CMQ
5962-01B0107QUB	F7400	TH1242ESHabc2EMQ
5962-01B0107Q4C	F7400	TH1242ESHabcYFMQ
5962-01B0107QNC	F7400	TH1242ESHabcKAMQ
5962-01B0107Q6B	F7400	TH1242ESHabc2GMQ
5962-01B0107Q5B	F7400	TH1242ESHabc2HMQ
5962-01B0107Q9A	F7400	TH1242ESHabcDDMQ
5962-01B0107VZC	F7400	TH1242ESHabcYCSV
5962-01B0107VYC	F7400	TH1242ESHabcKZSV
5962-01B0107VTB	F7400	TH1242ESHabc2CSV
5962-01B0107VUB	F7400	TH1242ESHabc2ESV
5962-01B0107V4C	F7400	TH1242ESHabcYFSV
5962-01B0107VNC	F7400	TH1242ESHabcKASV
5962-01B0107V6B	F7400	TH1242ESHabc2GSV
5962-01B0107V5B	F7400	TH1242ESHabc2HSV
5962-01B0107V9A	F7400	TH1242ESHabcDDSV
5962R01B0107VZC	F7400	TH1242ESHabcYCSR
5962R01B0107VYC	F7400	TH1242ESHabcKZSR
5962R01B0107VTB	F7400	TH1242ESHabc2CSR
5962R01B0107VUB	F7400	TH1242ESHabc2ESR
5962R01B0107V4C	F7400	TH1242ESHabcYFSR
5962R01B0107VNC	F7400	TH1242ESHabcKASR
5962R01B0107V6B	F7400	TH1242ESHabc2GSR
5962R01B0107V5B	F7400	TH1242ESHabc2HSR
5962-01B0108QZC	F7400	TH1332ESHabcYCMQ
5962-01B0108QTB	F7400	TH1332ESHabc2CMQ
5962-01B0108Q4C	F7400	TH1332ESHabcYFMQ
5962-01B0108Q6B	F7400	TH1332ESHabc2GMQ
5962-01B0108Q9A	F7400	TH1332ESHabcDDMQ

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor Similar PIN <u>2/ 3/</u>
5962-01B0108VZC	F7400	TH1332ESHabcYCSV
5962-01B0108VTB	F7400	TH1332ESHabc2CSV
5962-01B0108V4C	F7400	TH1332ESHabcYFSV
5962-01B0108V6B	F7400	TH1332ESHabc2GSV
5962-01B0108V9A	F7400	TH1332ESHabcDDSV
5962R01B0108VZC	F7400	TH1332ESHabcYCSR
5962R01B0108VTB	F7400	TH1332ESHabc2CSR
5962R01B0108V4C	F7400	TH1332ESHabcYFSR
5962R01B0108V6B	F7400	TH1332ESHabc2GSR
5962-01B0109QZC	F7400	TH1M099ERHabcYCMQ
5962-01B0109QYC	F7400	TH1M099ERHabcKZMQ
5962-01B0109QXC	F7400	TH1M099ERHabcK9MQ
5962-01B0109QUB	F7400	TH1M099ERHabc2EMQ
5962-01B0109Q4C	F7400	TH1M099ERHabcYFMQ
5962-01B0109QNC	F7400	TH1M099ERHabcKAMQ
5962-01B0109QMC	F7400	TH1M099ERHabcKBMQ
5962-01B0109Q5B	F7400	TH1M099ERHabc2HMQ
5962-01B0109Q9A	F7400	TH1M099ERHabcDDMQ
5962-01B0109VZC	F7400	TH1M099ERHabcYCSV
5962-01B0109VYC	F7400	TH1M099ERHabcKZSV
5962-01B0109VXC	F7400	TH1M099ERHabcK9SV
5962-01B0109VUB	F7400	TH1M099ERHabc2ESV
5962-01B0109V4C	F7400	TH1M099ERHabcYFSV
5962-01B0109VNC	F7400	TH1M099ERHabcKASV
5962-01B0109VMC	F7400	TH1M099ERHabcKBSV
5962-01B0109V5B	F7400	TH1M099ERHabc2HSV
5962-01B0109V9A	F7400	TH1M099ERHabcDDSV
5962R01B0109VZC	F7400	TH1M099ERHabcYCSR
5962R01B0109VYC	F7400	TH1M099ERHabcKZSR
5962R01B0109VXC	F7400	TH1M099ERHabcK9SR
5962R01B0109VUB	F7400	TH1M099ERHabc2ESR
5962R01B0109V4C	F7400	TH1M099ERHabcYFSR
5962R01B0109VNC	F7400	TH1M099ERHabcKASR
5962R01B0109VMC	F7400	TH1M099ERHabcKBSR
5962R01B0109V5B	F7400	TH1M099ERHabc2HSR
5962-01B0110QZC	F7400	TH1M156ERHabcYCMQ
5962-01B0110QYC	F7400	TH1M156ERHabcKZMQ
5962-01B0110QTB	F7400	TH1M156ERHabc2CMQ
5962-01B0110QUB	F7400	TH1M156ERHabc2EMQ
5962-01B0110Q4C	F7400	TH1M156ERHabcYFMQ
5962-01B0110QNC	F7400	TH1M156ERHabcKAMQ
5962-01B0110Q6B	F7400	TH1M156ERHabc2GMQ
5962-01B0110Q5B	F7400	TH1M156ERHabc2HMQ
5962-01B0110Q9A	F7400	TH1M156ERHabcDDMQ

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor Similar PIN <u>2/ 3/</u>
5962-01B0112VZC	F7400	TH1M332ERHabcYCSV
5962-01B0112VTB	F7400	TH1M332ERHabc2CSV
5962-01B0112V4C	F7400	TH1M332ERHabcYFSV
5962-01B0112V6B	F7400	TH1M332ERHabc2GSV
5962-01B0112V9A	F7400	TH1M332ERHabcDDSV
5962R01B0112VZC	F7400	TH1M332ERHabcYCSR
5962R01B0112VTB	F7400	TH1M332ERHabc2CSR
5962R01B0112V4C	F7400	TH1M332ERHabcYFSR
5962R01B0112V6B	F7400	TH1M332ERHabc2GSR
5962-01B0113QZC	F7400	TH1M099ESHabcYCMQ
5962-01B0113QYC	F7400	TH1M099ESHabcKZMQ
5962-01B0113QXC	F7400	TH1M099ESHabcK9MQ
5962-01B0113QUB	F7400	TH1M099ESHabc2EMQ
5962-01B0113Q4C	F7400	TH1M099ESHabcYFMQ
5962-01B0113QNC	F7400	TH1M099ESHabcKAMQ
5962-01B0113QMC	F7400	TH1M099ESHabcKBMQ
5962-01B0113Q5B	F7400	TH1M099ESHabc2HMQ
5962-01B0113Q9A	F7400	TH1M099ESHabcDDMQ
5962-01B0113VZC	F7400	TH1M099ESHabcYCSV
5962-01B0113VYC	F7400	TH1M099ESHabcKZSV
5962-01B0113VXC	F7400	TH1M099ESHabcK9SV
5962-01B0113VUB	F7400	TH1M099ESHabc2ESV
5962-01B0113V4C	F7400	TH1M099ESHabcYFSV
5962-01B0113VNC	F7400	TH1M099ESHabcKASV
5962-01B0113VMC	F7400	TH1M099ESHabcKBSV
5962-01B0113V5B	F7400	TH1M099ESHabc2HSV
5962-01B0113V9A	F7400	TH1M099ESHabcDDSV
5962R01B0113VZC	F7400	TH1M099ESHabcYCSR
5962R01B0113VYC	F7400	TH1M099ESHabcKZSR
5962R01B0113VXC	F7400	TH1M099ESHabcK9SR
5962R01B0113VUB	F7400	TH1M099ESHabc2ESR
5962R01B0113V4C	F7400	TH1M099ESHabcYFSR
5962R01B0113VNC	F7400	TH1M099ESHabcKASR
5962R01B0113VMC	F7400	TH1M099ESHabcKBSR
5962R01B0113V5B	F7400	TH1M099ESHabc2HSR
5962-01B0114QZC	F7400	TH1M156ESHabcYCMQ
5962-01B0114QYC	F7400	TH1M156ESHabcKZMQ
5962-01B0114QTB	F7400	TH1M156ESHabc2CMQ
5962-01B0114QUB	F7400	TH1M156ESHabc2EMQ
5962-01B0114Q4C	F7400	TH1M156ESHabcYFMQ
5962-01B0114QNC	F7400	TH1M156ESHabcKAMQ
5962-01B0114Q6B	F7400	TH1M156ESHabc2GMQ
5962-01B0114Q5B	F7400	TH1M156ESHabc2HMQ
5962-01B0114Q9A	F7400	TH1M156ESHabcDDMQ

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor Similar PIN 2/ 3/
5962-01B0116VZC	F7400	TH1M332ESHabcYCSV
5962-01B0116VTB	F7400	TH1M332ESHabc2CSV
5962-01B0116V4C	F7400	TH1M332ESHabcYFSV
5962-01B0116V6B	F7400	TH1M332ESHabc2GSV
5962-01B0116V9A	F7400	TH1M332ESHabcDDSV
5962R01B0116VZC	F7400	TH1M332ESHabcZCSR
5962R01B0116VTB	F7400	TH1M332ESHabc2CSR
5962R01B0116V4C	F7400	TH1M332ESHabcYFSR
5962R01B0116V6B	F7400	TH1M332ESHabc2GSR
5962-01B0117QZC	F7400	TH1099RabcYCMQ
5962-01B0117QYC	F7400	TH1099RabcKZMQ
5962-01B0117QXC	F7400	TH1099RabcK9MQ
5962-01B0117QUB	F7400	TH1099Rabc2EMQ
5962-01B0117Q4C	F7400	TH1099RabcYFMQ
5962-01B0117QNC	F7400	TH1099RabcKAMQ
5962-01B0117QMC	F7400	TH1099RabcKBMQ
5962-01B0117Q5B	F7400	TH1099Rabc2HMQ
5962-01B0117Q9A	F7400	TH1099RabcDDMQ
5962-01B0118QZC	F7400	TH1156RabcYCMQ
5962-01B0118QYC	F7400	TH1156RabcKZMQ
5962-01B0118QTB	F7400	TH1156Rabc2CMQ
5962-01B0118QUB	F7400	TH1156Rabc2EMQ
5962-01B0118Q4C	F7400	TH1156RabcYFMQ
5962-01B0118QNC	F7400	TH1156RabcKAMQ
5962-01B0118Q6B	F7400	TH1156Rabc2GMQ
5962-01B0118Q5B	F7400	TH1156Rabc2HMQ
5962-01B0118Q9A	F7400	TH1156RabcDDMQ
5962-01B0119QZC	F7400	TH1242RabcYCMQ
5962-01B0119QYC	F7400	TH1242RabcKZMQ
5962-01B0119QTB	F7400	TH1242Rabc2CMQ
5962-01B0119QUB	F7400	TH1242Rabc2EMQ
5962-01B0119Q4C	F7400	TH1242RabcYFMQ
5962-01B0119QNC	F7400	TH1242RabcKAMQ
5962-01B0119Q6B	F7400	TH1242Rabc2GMQ
5962-01B0119Q5B	F7400	TH1242Rabc2HMQ
5962-01B0119Q9A	F7400	TH1242RabcDDMQ
5962-01B0120QZC	F7400	TH1332RabcYCMQ
5962-01B0120QTB	F7400	TH1332Rabc2CMQ
5962-01B0120Q4C	F7400	TH1332RabcYFMQ
5962-01B0120Q6B	F7400	TH1332Rabc2GMQ
5962-01B0120Q9A	F7400	TH1332RabcDDMQ

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor Similar PIN <u>2</u> / <u>3</u> /
5962-01B0121QZC	F7400	TH1099SabcYCMQ
5962-01B0121QYC	F7400	TH1099SabcKZMQ
5962-01B0121QXC	F7400	TH1099SabcK9MQ
5962-01B0121QUB	F7400	TH1099Sabc2EMQ
5962-01B0121Q4C	F7400	TH1099SabcYFMQ
5962-01B0121QNC	F7400	TH1099SabcKAMQ
5962-01B0121QMC	F7400	TH1099SabcKBMQ
5962-01B0121Q5B	F7400	TH1099Sabc2HMQ
5962-01B0121Q9A	F7400	TH1099SabcDDMQ
5962-01B0122QZC	F7400	TH1156SabcYCMQ
5962-01B0122QYC	F7400	TH1156SabcKZMQ
5962-01B0122QTB	F7400	TH1156Sabc2CMQ
5962-01B0122QUB	F7400	TH1156Sabc2EMQ
5962-01B0122Q4C	F7400	TH1156SabcYFMQ
5962-01B0122QNC	F7400	TH1156SabcKAMQ
5962-01B0122Q6B	F7400	TH1156Sabc2GMQ
5962-01B0122Q5B	F7400	TH1156Sabc2HMQ
5962-01B0122Q9A	F7400	TH1156SabcDDMQ
5962-01B0123QZC	F7400	TH1242SabcYCMQ
5962-01B0123QYC	F7400	TH1242SabcKZMQ
5962-01B0123QTB	F7400	TH1242Sabc2CMQ
5962-01B0123QUB	F7400	TH1242Sabc2EMQ
5962-01B0123Q4C	F7400	TH1242SabcYFMQ
5962-01B0123QNC	F7400	TH1242SabcKAMQ
5962-01B0123Q6B	F7400	TH1242Sabc2GMQ
5962-01B0123Q5B	F7400	TH1242Sabc2HMQ
5962-01B0123Q9A	F7400	TH1242SabcDDMQ
5962-01B0124QZC	F7400	TH1332SabcYCMQ
5962-01B0124QTB	F7400	TH1332Sabc2CMQ
5962-01B0124Q4C	F7400	TH1332SabcYFMQ
5962-01B0124Q6B	F7400	TH1332Sabc2GMQ
5962-01B0124Q9A	F7400	TH1332SabcDDMQ
5962-01B0125QZC	F7400	TH1M099RDabcYCMQ
5962-01B0125QYC	F7400	TH1M099RDabcKZMQ
5962-01B0125QXC	F7400	TH1M099RDabcK9MQ
5962-01B0125QUB	F7400	TH1M099RDabc2EMQ
5962-01B0125Q4C	F7400	TH1M099RDabcYFMQ
5962-01B0125QNC	F7400	TH1M099RDabcKAMQ
5962-01B0125QMC	F7400	TH1M099RDabcKBMQ
5962-01B0125Q5B	F7400	TH1M099RDabc2HMQ
5962-01B0125Q9A	F7400	TH1M099RDabcDDMQ

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor Similar PIN 2/ 3/
5962-01B0126QZC	F7400	TH1M156RDabcYCMQ
5962-01B0126QYC	F7400	TH1M156RDabcKZMQ
5962-01B0126QTB	F7400	TH1M156RDabc2CMQ
5962-01B0126QUB	F7400	TH1M156RDabc2EMQ
5962-01B0126Q4C	F7400	TH1M156RDabcYFMQ
5962-01B0126QNC	F7400	TH1M156RDabcKAMQ
5962-01B0126Q6B	F7400	TH1M156RDabc2GMQ
5962-01B0126Q5B	F7400	TH1M156RDabc2HMQ
5962-01B0126Q9A	F7400	TH1M156RDabcDDMQ
5962-01B0127QZC	F7400	TH1M242RDabcYCMQ
5962-01B0127QYC	F7400	TH1M242RDabcKZMQ
5962-01B0127QTB	F7400	TH1M242RDabc2CMQ
5962-01B0127QUB	F7400	TH1M242RDabc2EMQ
5962-01B0127Q4C	F7400	TH1M242RDabcYFMQ
5962-01B0127QNC	F7400	TH1M242RDabcKAMQ
5962-01B0127Q6B	F7400	TH1M242RDabc2GMQ
5962-01B0127Q5B	F7400	TH1M242RDabc2HMQ
5962-01B0127Q9A	F7400	TH1M242RDabcDDMQ
5962-01B0128QZC	F7400	TH1M332RDabcYCMQ
5962-01B0128QTB	F7400	TH1M332RDabc2CMQ
5962-01B0128Q4C	F7400	TH1M332RDabcYFMQ
5962-01B0128Q6B	F7400	TH1M332RDabc2GMQ
5962-01B0128Q9A	F7400	TH1M332RDabcDDMQ
5962-01B0129QZC	F7400	TH1M099SDabcYCMQ
5962-01B0129QYC	F7400	TH1M099SDabcKZMQ
5962-01B0129QXC	F7400	TH1M099SDabcK9MQ
5962-01B0129QUB	F7400	TH1M099SDabc2EMQ
5962-01B0129Q4C	F7400	TH1M099SDabcYFMQ
5962-01B0129QNC	F7400	TH1M099SDabcKAMQ
5962-01B0129QMC	F7400	TH1M099SDabcKBMQ
5962-01B0129Q5B	F7400	TH1M099SDabc2HMQ
5962-01B0129Q9A	F7400	TH1M099SDabcDDMQ
5962-01B0130QZC	F7400	TH1M156SDabcYCMQ
5962-01B0130QYC	F7400	TH1M156SDabcKZMQ
5962-01B0130QTB	F7400	TH1M156SDabc2CMQ
5962-01B0130QUB	F7400	TH1M156SDabc2EMQ
5962-01B0130Q4C	F7400	TH1M156SDabcYFMQ
5962-01B0130QNC	F7400	TH1M156SDabcKAMQ
5962-01B0130Q6B	F7400	TH1M156SDabc2GMQ
5962-01B0130Q5B	F7400	TH1M156SDabc2HMQ
5962-01B0130Q9A	F7400	TH1M156SDabcDDMQ

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor Similar PIN <u>2/ 3/</u>
5962-01B0131QZC	F7400	TH1M242SDabcYCMQ
5962-01B0131QYC	F7400	TH1M242SDabcKZMQ
5962-01B0131QTB	F7400	TH1M242SDabc2CMQ
5962-01B0131QUB	F7400	TH1M242SDabc2EMQ
5962-01B0131Q4C	F7400	TH1M242SDabcYFMQ
5962-01B0131QNC	F7400	TH1M242SDabcKAMQ
5962-01B0131Q6B	F7400	TH1M242SDabc2GMQ
5962-01B0131Q5B	F7400	TH1M242SDabc2HMQ
5962-01B0131Q9A	F7400	TH1M242SDabcDDMQ
5962-01B0132QZC	F7400	TH1M332SDabcYCMQ
5962-01B0132QTB	F7400	TH1M332SDabc2CMQ
5962-01B0132Q4C	F7400	TH1M332SDabcYFMQ
5962-01B0132Q6B	F7400	TH1M332SDabc2GMQ
5962-01B0132Q9A	F7400	TH1M332SDabcDDMQ
5962-01B0133Q7C	F7400	TH1256AabcYEMQ
5962-01B0133Q8C	F7400	TH1256AabcYDMQ
5962-01B0133V7C	F7400	TH1256AabcYESV
5962-01B0133V8C	F7400	TH1256AabcYDSV
5962R01B0133V7C	F7400	TH1256AabcYESR
5962R01B0133V8C	F7400	TH1256AabcYDSR

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ The "abc" is reserved to indicate the customer specific code.

Vendor CAGE
number

F7400

Vendor name
and address

Atmel Nantes SA.
BP 70602
44306 Nantes Cedex 3
France

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