REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
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REV																				
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REV STATUS				REV			A		A	A								A	A	
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	

PMIC N/A

PREPARED BY

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY

Phu H. Nguyen

APPROVED BY

Thomas M. Hess

DRAWING APPROVAL DATE

03-08-11

REVISION LEVEL

A

MICROCIRCUIT, DIGITAL, CMOS GATE ARRAY BASED ON CAN ASIC SPACE APPLICATION (CASA2), MONOLITHIC SILICON

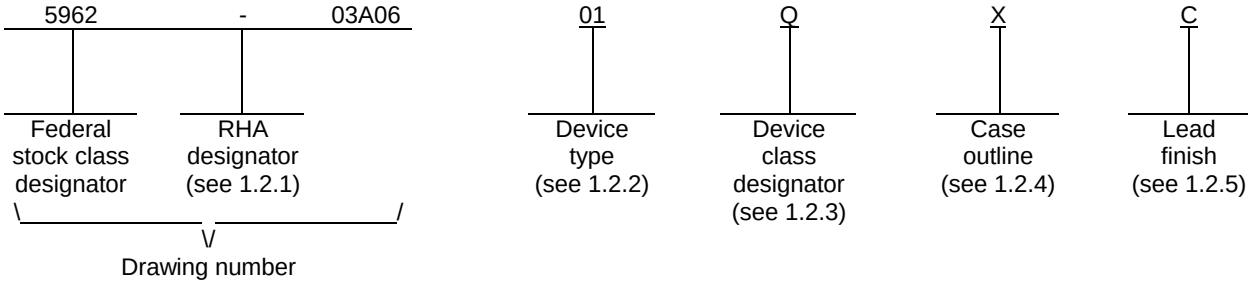
SIZE	CAGE CODE	
A	**67268**	**5962-03A06**

SHEET 1 OF 13

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	AT7908E	Can ASIC space application

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	44	Multilayer ceramic package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{DD}) ..... -0.5 V to 6.0 V 2/
Input voltage range (V_{IN}) ..... -0.5 V to V_{DD} + 0.5 V 3/
Storage temperature range ..... -65°C to +150°C
Lead temperature ..... +300°C 4/
Maximum junction temperature (T_J) ..... +175°C
Maximum power dissipation (P_D) ..... 0.3 W
Thermal resistance, junction-to-case (θ_{JC}) ..... 5.1°C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{DD}) ..... 4.5 V to 5.5 V
Ambient temperature (T_A) ..... -55°C to 125°C
Storage conditions ..... 30°C, 20 to 65% RH, dust free, original packing

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltages referenced to ground unless otherwise specified.
3/ V_{DD} + 0.5 V shall not exceed 6.0 V.
4/ Duration 10 second maximum at a distance not less than 1.6 mm.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block or logic diagram. The block or logic diagram shall be as specified on figure 3.

3.2.4 Timing waveforms. The timing waveforms shall be specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 123 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A Subgroups	Limits		Units
				Min.	Max.	
Input clamp voltage to ground 1/	V_{IC}	I_{OH} = -300 µA	1, 2, 3	-1.2	-0.2	V
Low level input current 2/	I_{IL}	V_{IN} = GND, V_{DD} = 5.5 V	1, 2, 3	-5		µA
Low level input current, pull-up 2/	I_{ILPU}	V_{IN} = GND, V_{DD} = 5.5 V	1, 2, 3	-100		µA
Low level input current, pull-down 2/	I_{LLPD}	V_{IN} = GND, V_{DD} = 5.5 V	1, 2, 3	-5		µA
High level input current 2/	I_{IH}	V_{IN} = V_{DD} = 5.5 V	1, 2, 3		5	µA
High level input current, pull-up 2/	I_{IHPU}	V_{IN} = V_{DD} = 5.5 V	1, 2, 3		5	µA
High level input current, pull-down 2/	I_{IHPD}	V_{IN} = V_{DD} = 5.5 V	1, 2, 3		300	µA
Output leakage low current 2/	I_{OZL}	V_{OUT} = GND, Outputs disabled	1, 2, 3	-5		µA
Output leakage high current, pull-down output 2/	I_{OZHPD}	V_{OUT} = V_{DD}, Outputs disabled	1, 2, 3		300	µA
Output leakage low current, pull-up output 2/	I_{OZLPU}	V_{OUT} = GND, Outputs disabled	1, 2, 3	-100		µA
Output leakage high current 2/	I_{OZH}	V_{OUT} = V_{DD}, Outputs disabled	1, 2, 3		5	µA
Low level output voltage, BOUT12 2/	V_{OL1}	V_{DD} = 4.5 V, I_{OL} = +12 mA	1, 2, 3		0.4	V
Low level output voltage, BOUT6 2/	V_{OL2}	V_{DD} = 4.5 V, I_{OL} = +6 mA	1, 2, 3		0.4	V
Low level output voltage, BOUT3 2/	V_{OL3}	V_{DD} = 4.5 V, I_{OL} = +3 mA	1, 2, 3		0.4	V
High level output voltage, BOUT12 2/	V_{OH1}	V_{DD} = 4.5 V, I_{OL} = -12 mA	1, 2, 3	3.9		V
High level output voltage, BOUT6 2/	V_{OH2}	V_{DD} = 4.5 V, I_{OL} = -6 mA	1, 2, 3	3.9		V
High level output voltage, BOUT3 2/	V_{OH3}	V_{DD} = 4.5 V, I_{OL} = -3 mA	1, 2, 3	3.9		V
Low level input voltage 1/	V_{IL}	Functional verification	1, 2, 3		0.3 V_{DD}	V
High level input voltage 1/	V_{IH}	Functional verification	1, 2, 3	0.7 V_{DD}		V
Input capacitance 3/	C_I	V_{DD} = 0 V	4		15	pF
Output capacitance 3/	C_{IO}	V_{DD} = 0 V	4		15	pF
Supply current stand by for array 2/	I_{DDSBA}	V_{DA} = 5.5V	1, 2, 3		50	µA
Supply current operating for array 2/	I_{DDOPA}	V_{DA} = 5.5V	4, 5, 6		25	mA
Supply current operating for buffer 2/	I_{DDOPB}	V_{DB} = 5.5V	4, 5, 6		10	mA

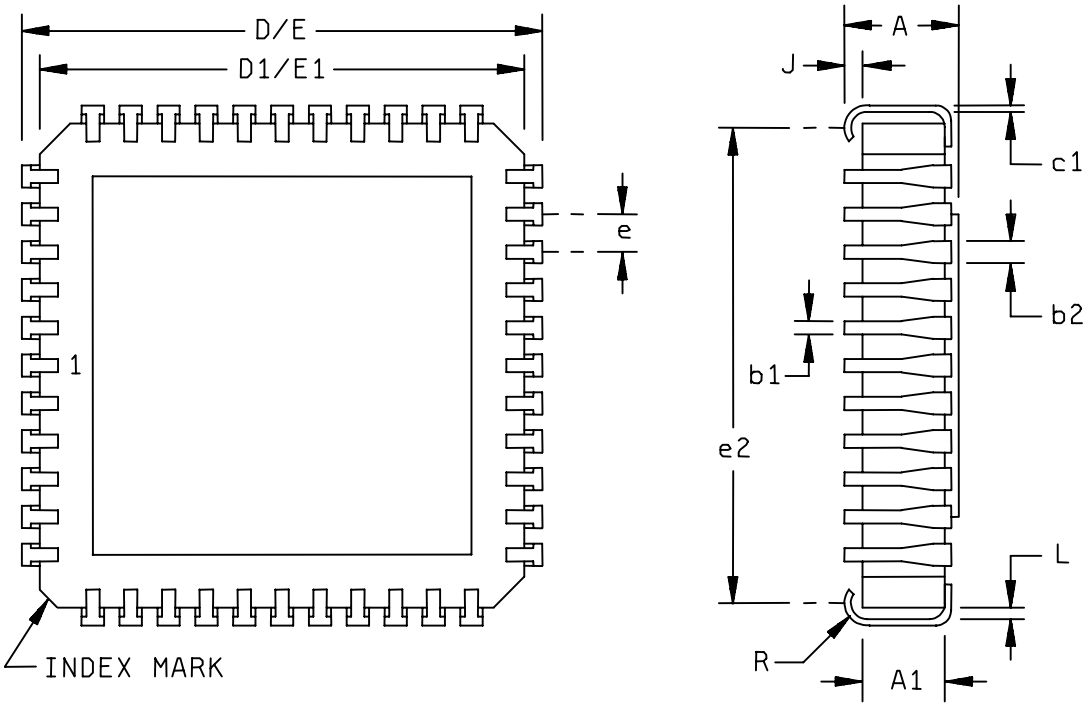
See notes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A Subgroups	Limits		Units
				Min.	Max.	
Address valid to ALE low 2/	T_{AVLL}	V_{DD} = 5V ±10%,	9, 10, 11		4	ns
Address hold after ALE low 2/	T_{LLAX}	V_{SS} = 0V,	9, 10, 11		4	
ALE high time	T_{LHLL}	Tclk = 100 ns	9, 10, 11		100	
ALE low to RD low	T_{LLRL}		9, 10, 11		200	
CS high to RD low 2/	T_{CHRL}		9, 10, 11		100	
Input data valid to WR High	T_{DVWH}		9, 10, 11		300	
Input data hold after WR high	T_{WHQX}		9, 10, 11		10	
WR pulse width	T_{WLWH}		9, 10, 11		300	
WR high to next ALE high	T_{WHLH}		9, 10, 11		100	
WR setup time before clock 2/	T_{WS}		9, 10, 11		-3	
WR hold time after clock	T_{WH}		9, 10, 11		7	
RD pulse width	T_{RLRH}		9, 10, 11		300	
RD low to data valid	T_{RLDV}		9, 10, 11	6	82	
Data float after RD High	T_{RHDZ}		9, 10, 11	4	20	

Notes:
1. Forcing conditions of the functional test assure that these limits are met but they will not be individually recorded.
2. Read and record measurements in accordance with MIL-PRF-38535.
3. Tested at initial design and after major process changes, otherwise guaranteed.

Case X



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.67	4.95	.105	.195
A1	1.65 NOM		.065 NOM	
b1	0.33	0.56	.013	.022
b2	0.55	0.88	.022	.035
c1	0.17	0.25	.007	.010
D/E	17.14	17.78	.675	.700
D1/E1	15.74	16.75	.620	.660
e	1.27 BSC		.050 BSC	
e2	16.00 BSC		.630 BSC	
L	0.12		.005	
ND/NE	11		11	
R	0.50	1.01	.020	.040
J	0.58		.023	

FIGURE 1. Case outline.

Pin number	Signal name	Type	Note
1	V_{DDA1}		Power for array
2	Addr[4]	I	Input address (mode 1) or output address (mode 0)
3	Addr[5]	I	Input address (mode 1) or output address (mode 0)
4	Addr[6]	I	Input address (mode 1) or output address (mode 0)
5	Addr[7]	I	Input address (mode 1) or output address (mode 0)
6	V_{SSB1}		Ground for periphery
7	V_{DDB2}		Power for periphery
8	Cs	I	Chip Select signal
9	Mode	I	Interface operational mode
10	Ale	I	Adress latch enable
11	Wr	I	Write signal
12	V_{SSA1}		Ground for Array
13	Rd	I	Read signal
14	Sena	I	Scan enable
15	Test	I	Input signal to increase testability
16	Reset	I	Reset signal
17	V_{SSB2}		Ground for periphery
18	V_{DDB3}		Power for periphery
19	Can_rx	I	RX signal
20	Hasync	O	Output synchronization signal
21			Not connected
22	Xtalout	I/O	Output from internal oscillator
23	Xtalin	I	Input to internal oscillator or clock input from external oscillator
24	V_{DDA2}		Power for array
25	Int	O	Interrupt request
26	Hatrig	O	Output signal to trigger the message matching
27	Can_tx	O	TX signal
28	V_{SSB3}		Ground for periphery
29	V_{DDB4}		Power for periphery
30	Data[0]	I/O	Adress data bus
31	Data[1]	I/O	Adress data bus
32	Data[2]	I/O	Adress data bus
33	Data[3]	I/O	Adress data bus
34	V_{SSA2}		Ground for Array
35	Data[4]	I/O	Adress data bus

FIGURE 2. Terminal connections.

Pin number	Signal name	Type	Note
36	Data[5]	I/O	Adress data bus
37	Data[6]	I/O	Adress data bus
38	Data[7]	I/O	Adress data bus
39	V_{SSB4}		Ground for periphery
40	V_{DDB1}		Power for periphery
41	Addr[0]	I	Input address (mode 1) or output address (mode 0)
42	Addr[1]	I	Input address (mode 1) or output address (mode 0)
43	Addr[2]	I	Input address (mode 1) or output address (mode 0)
44	Addr[3]	I	Input address (mode 1) or output address (mode 0)

Notes:
1. Mode : Input pin to select operational mode of interface:
   mode = 0 : 8 bit data bus multiplexed with lowest 8-bit address(register mapped between 8000Hex and 804Chex)
   mode = 1 : 8 bit not multiplexed address data bus (register mapped between 00 Hex and 4C Hex)
2. $V_{DDA1} = V_{DDA2} = V_{DDB1} = V_{DDB2} = V_{DDB3} = V_{DDB4} = 5$ V
3. $V_{SSA1} = V_{SSA2} = V_{SSB1} = V_{SSB2} = V_{SSB3} = V_{SSB4} = 0$V
4. I = Input, O = Output

FIGURE 2. Terminal connections - Continued.

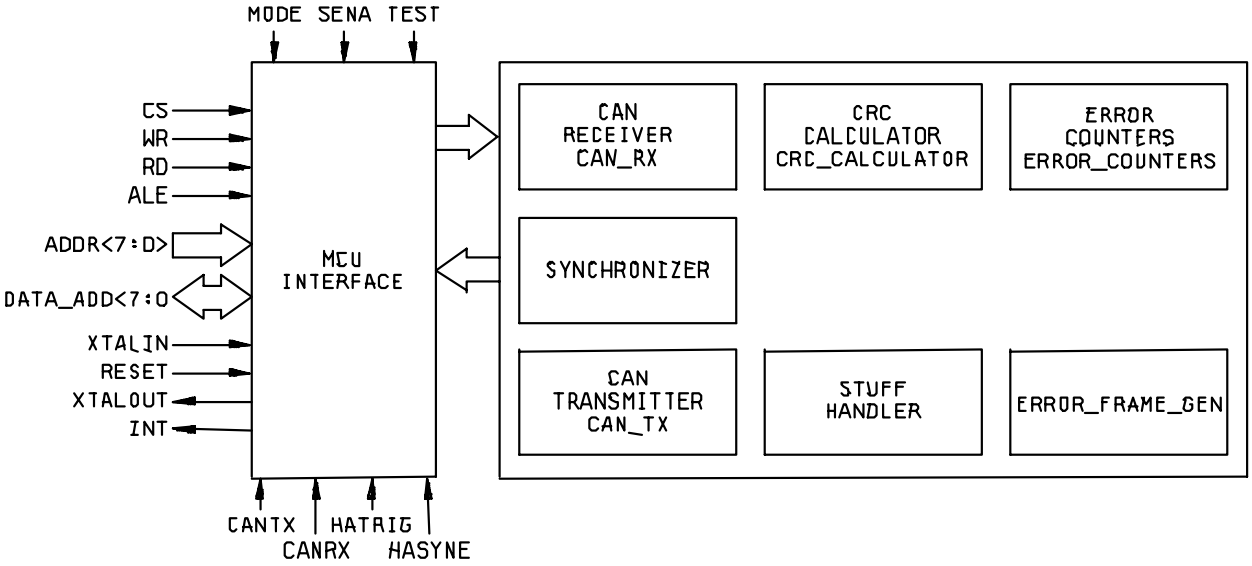


FIGURE 3. Block diagram.

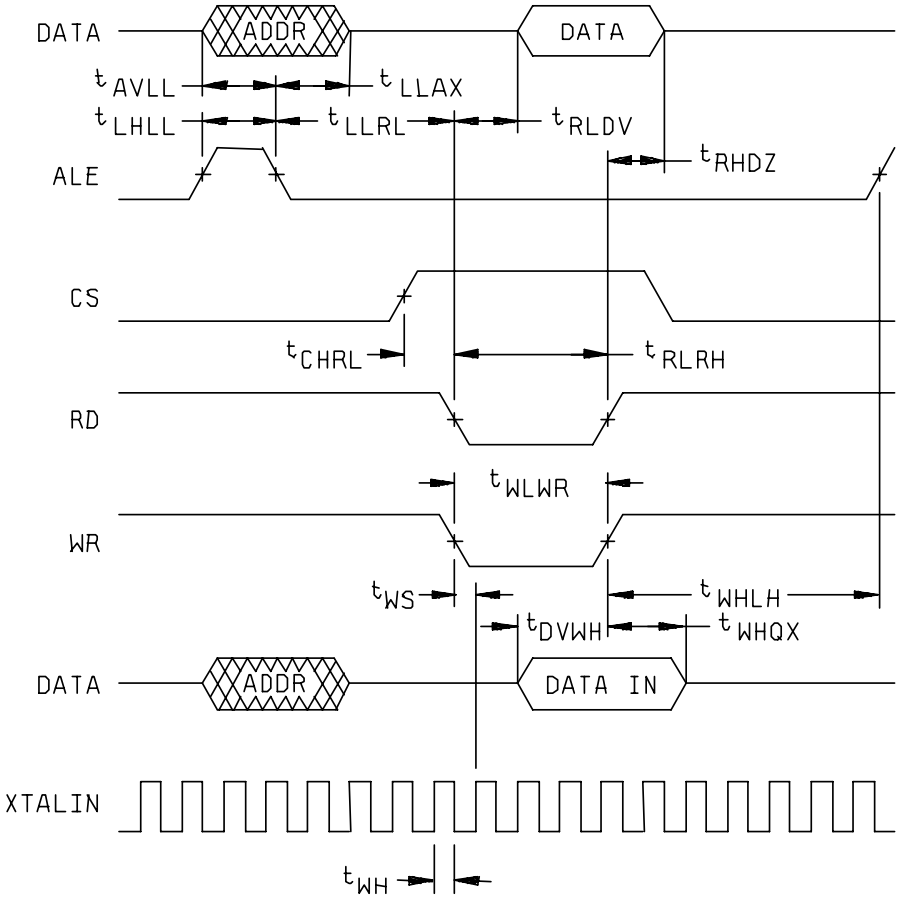


FIGURE 4. Timing waveforms.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9	1, 7, 9 Δ 1/
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 2/	1, 2, 3, 7, 8, 9, 10, 11 2/	1, 2, 3, 7, 8, 9, 10, 11 3/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 7, 9	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1. Δ indicates delta limits (see table IIB) shall be required where specified and the delta values shall be computed with reference to previous interim electrical parameters. For device class V, performance of delta limits shall be specified by the manufacturer's QM plan.
2. PDA applies to subgroups 1.
3. PDA applies to subgroups 1 and 7.

TABLE IIB. Delta limits at 25°C

Parameters 1/	All device types
I_{CCSBA}	± 5 µA
V_{OL}/V_{OH}	± 0.1 V
I_{OZL}/I_{OZH}	± 0.1 µA
I_{IL}/I_{IH}	± 0.1 µA

1. The above parameters shall be recorded before and after burn-in and life test to determine the drift.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with
MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-03-06

Approved sources of supply for SMD 5962-03A06 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-03A0601QXC	F7400	AT7908EJLMQ
5962-03A0601VXC	F7400	AT7908EJLSV

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
F7400	Atmel Nantes SA BP 70602 44306 Nantes Cedex 3 France