INTEGRATED CIRCUITS



Product data sheet Supersedes data of 1998 Feb 13

2004 Sep 14





74ALVT16543

FEATURES

- 16-bit universal bus interface
- 5 V I/O Compatible
- 3-State buffers
- Output capability: +64 mA/-32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted

QUICK REFERENCE DATA

- Power-up 3-State
- Power-up reset
- No bus current loading when output is tied to 5 V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ALVT16543 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5 V or 3.3 V with I/O compatibility up to 5 V. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

The 74ALVT16543 contains two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B Enable (nEAB) input and the A-to-B Latch Enable (nEAB) input are LOW, the A-to-B path is transparent.

A subsequent LOW-to-HIGH transition of the nLEAB signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With nEAB and nOEAB both LOW, the 3-State B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the nEBA, nLEBA, and nOEBA inputs.

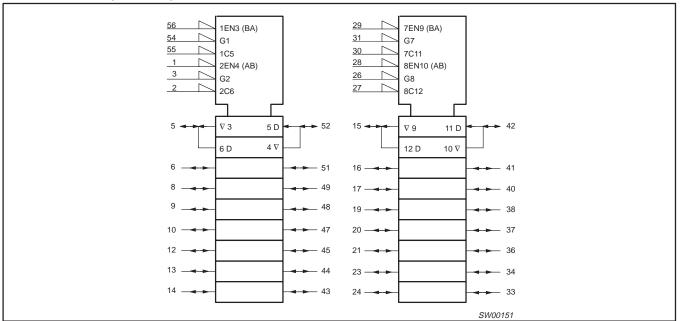
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

SYMBOL	PARAMETER	CONDITIONS	TYPI	UNIT	
STMBOL	PARAMETER	$T_{amb} = 25 \ ^{\circ}C; \ GND = 0 \ V$	2.5 V	3.3 V	UNIT
t _{PLH} t _{PHL}	Propagation delay nAx to nBx or nBx to nAx	C _L = 50 pF	1.8 2.7	1.6 1.8	ns
C _{IN}	Input capacitance DIR, \overline{OE}	$V_I = 0 V \text{ or } V_{CC}$	3	3	pF
C _{I/O}	I/O pin capacitance	Outputs disabled; $V_{I/O} = 0 V \text{ or } V_{CC}$	9	9	pF
I _{CCZ}	Total supply current	Outputs disabled	40	70	μΑ

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	TYPE NUMBER	DWG NUMBER
56-Pin Plastic SSOP Type III	–40 °C to +85 °C	74ALVT16543DL	SOT371-1
56-Pin Plastic TSSOP Type II	–40 °C to +85 °C	74ALVT16543DGG	SOT364-1

LOGIC SYMBOL (IEEE/IEC)

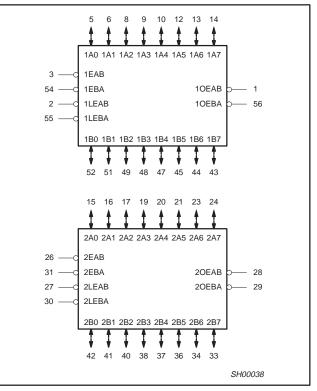


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1OEAB	1	56	1 OEBA
1LEAB	2	55	1LEBA
1EAB	3	54	1EBA
GND	4	53	GND
1A0	5	52	1B0
1A1	6	51	1B1
Vcc	7	50	VCC
1A2	8	49	1B2
1A3	9	48	1B3
1A4	10	47	1B4
GND	11	46	GND
1A5	12	45	1B5
1A6	13	44	1B6
1A7	14	43	1B7
2A0	15	42	2B0
2A1	16	41	2B1
2A2	17	40	2B2
GND	18	39	GND
2A3	19	38	2B3
2A4	20	37	2B4
2A5	21	36	2B5
Vcc	22	35	VCC
2A6	23	34	2B6
2A7	24	33	2B7
GND	25	32	GND
2EAB	26	31	2EBA
2LEAB	27	30	2LEBA
20EAB	28	29	20EBA
		SH00037	

PIN CONFIGURATION

LOGIC SYMBOL

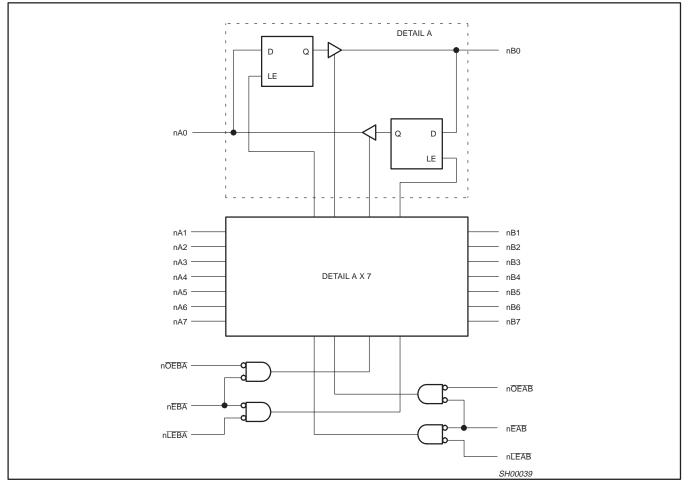


PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7, 2A0 – 2A7	A Data inputs/outputs
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40,38, 37, 36, 34, 33	1B0 – 1B7, 2B0 – 2B7	B Data inputs/outputs
1, 56 28, 29	1 <u>OEAB</u> , 1 <u>OEBA,</u> 2 <u>OEAB</u> , 2 <u>OEBA</u>	A to B / B to A Output Enable inputs (active-LOW)
3, 54 26, 31	1EAB, 1EBA, 2EAB, 2EBA	A to B / B to A Enable inputs (active-LOW)
2, 55 27, 30	1LEAB, 1LEBA, 2LEAB, 2LEBA	A to B / B to A Latch Enable inputs (active-LOW)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0 V)
7, 22, 35, 50	V _{CC}	Positive supply voltage

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LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	STATUS	
nOEXX	nEXX	nLEXX	nAx or nBx	nBx or nAx	STATUS
Н	Х	Х	Х	Z	Disabled
Х	Н	Х	Х	Z	Disabled
L	$\uparrow \uparrow$	L	h I	Z Z	Disabled + Latch
L L	L L	$\stackrel{\uparrow}{\leftarrow}$	h I	H L	Latch + Display
L L	L L	L	H L	H L	Transparent
L	L	Н	Х	NC	Hold

 $\begin{array}{l} H = & HIGH \text{ voltage level} \\ h = & HIGH \text{ voltage level one setup time prior to the LOW-to-HIGH transition of nLEXX or nEXX (XX = AB or BA) } \end{array}$

= LOW voltage level L

= LOW voltage level one setup time prior to the LOW-to-HIGH transition of nLEXX or nEXX (XX = AB or BA) 1

Don't care

X ↑ = LOW-to-HIGH transition of $n\overline{\text{LEXX}}$ or $n\overline{\text{EXX}}$ (XX = AB or BA)

NC= No change

Z = High-impedance or "off" state

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ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +4.6	V
I _{IK}	DC input diode current	V ₁ < 0 V	-50	mA
VI	DC input voltage ³		-0.5 to +7.0	V
Ι _{ΟΚ}	DC output diode current	V _O < 0 V	-50	mA
V _{OUT}	DC output voltage ³	Output in Off or HIGH state	-0.5 to +7.0	V
		Output in LOW state	128	mA
IOUT	DC output current	Output in HIGH state	-64	
T _{stg}	Storage temperature range		-65 to +150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

 The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5 V RAN	GE LIMITS	3.3 V RAN	UNIT	
STMBOL	TANAMETEN	MIN	MAX	MIN	MAX	UNIT
V _{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
VI	Input voltage	0	5.5	0	5.5	V
V _{IH}	HIGH-level input voltage	1.7		2.0		V
V _{IL}	Input voltage		0.7		0.8	V
I _{ОН}	HIGH-level output current		-8		-32	mA
	LOW-level output current		8		32	mA
IOL	LOW-level output current; current duty cycle \leq 50 %; f \geq 1 kHz		24		64	
Δt/Δv	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T _{amb}	Operating free-air temperature range	-40	+85	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS (3.3 V \pm 0.3 V RANGE)

				L	IMITS		
SYMBOL PARAMETER		TEST CONDITIONS		Temp = -40 °C to +85 °C			UNIT
				MIN	TYP ¹	МАХ	
V _{IK}	Input clamp voltage	V _{CC} = 3.0 V; I _{IK} = -18 mA		-	-0.85	-1.2	V
M		V_{CC} = 3.0 V to 3.6 V; I_{OH} = -100 μ A		V _{CC} - 0.2	V _{CC}	-	v
V _{OH}	HIGH-level output voltage	$V_{CC} = 3.0 \text{ V}; \text{ I}_{OH} = -32 \text{ mA}$		2.0	2.3	-	
		$V_{CC} = 3.0 \text{ V}; \text{ I}_{OL} = 100 \mu\text{A}$		-	0.07	0.2	
M.	LOW-level output voltage	V _{CC} = 3.0 V; I _{OL} = 16 mA		-	0.25	0.4	v
V _{OL}		V _{CC} = 3.0 V; I _{OL} = 32 mA		-	0.3	0.5	v
		V _{CC} = 3.0 V; I _{OL} = 64 mA		-	0.4	0.55	
V _{RST}	Power-up output low voltage ⁶	V_{CC} = 3.6 V; I _O = 1 mA; V _I = V _{CC} or GN	C	-	-	0.55	V
		V_{CC} = 3.6 V; V_{I} = V_{CC} or GND	Control pins	-	0.1	± 1	μΑ
		$V_{CC} = 0 \text{ V or } 3.6 \text{ V}; \text{ V}_{I} = 5.5 \text{ V}$		-	0.1	10	
I _I	I _I Input leakage current	$V_{CC} = 3.6 \text{ V}; \text{ V}_{I} = V_{CC}$	Data pins ⁴	-	0.5	1	
		$V_{CC} = 3.6 \text{ V}; \text{ V}_{I} = 0 \text{ V}$		-	0.1	-5	
		$V_{CC} = 3.6 \text{ V}; \text{ V}_{I} = 5.5 \text{ V}$		-	0.1	20	
I _{OFF}	Off current	V_{CC} = 0 V; V_{I} or V_{O} = 0 V to 4.5 V		-	0.1	± 100	μA
	Due Mald average	$V_{CC} = 3 \text{ V}; \text{ V}_{I} = 0.8 \text{ V}$		75	130	-	
I _{HOLD}	Bus Hold current Data inputs ⁷	V _{CC} = 3 V; V _I = 2.0 V		-75	-140	-	μA
		V_{CC} = 0 V to 3.6 V; V_{CC} = 3.6 V		± 500	-	-	
I_{EX}	Current into an output in the High state when $V_O > V_{CC}$	$V_{O} = 5.5 \text{ V}; V_{CC} = 3.0 \text{ V}$		-	50	125	μΑ
I _{PU/PD}	Power-up/down 3-State output current ³	$V_{CC} \leq$ 1.2 V; V_{O} = 0.5 V to $V_{CC};$ V_{I} = GN OE/OE = Don't care	D or V _{CC} ;	-	40	± 100	μA
ICCH		V_{CC} = 3.6 V; Outputs HIGH; V_{I} = GND o I_{O} = 0 mA	V_{CC} = 3.6 V; Outputs HIGH; V_I = GND or V_{CC} ; I_O = 0 mA		0.07	0.1	
I _{CCL}	Quiescent supply current	V_{CC} = 3.6 V; Outputs LOW; V _I = GND of I _O = 0 mA	V _{CC} ;	-	3.6	5	mA
I _{CCZ}		V_{CC} = 3.6 V; Outputs disabled; V _I = GND or V _{CC} , I _O = 0 mA ⁵		-	0.07	0.1	
ΔI_{CC}	Additional supply current per input pin ²	V_{CC} = 3 V to 3.6 V; One input at V_{CC} – 0 Other inputs at V_{CC} or GND	0.6 V;	-	0.04	0.4	mA

NOTES:

1. All typical values are at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C. 2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND. 3. This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 msec. From $V_{CC} = 1.2$ V to $V_{CC} = 3.3$ V ± 0.3 V a transition time of 100 µsec is permitted. This parameter is valid for $T_{amb} = 25$ °C only.

4. Unused pins at V_{CC} or GND. 5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground. 6. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power. 7. This is the bus hold overdrive current required to force the input to the opposite logic state.

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DC ELECTRICAL CHARACTERISTICS (2.5 V \pm 0.2 V RANGE)

					IMITS		
SYMBOL	PARAMETER	TEST CONDITIONS		Temp = -40 °C to +8		+85 °C	
				MIN	TYP ¹	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 2.3 V; I _{IK} = -18 mA		-	-0.85	-1.2	V
V	HIGH-level output voltage	V_{CC} = 2.3 V to 3.6 V; I_{OH} = –100 μA		V _{CC} – 0.2	V _{CC}	-	v
V _{OH}	nigh-level output voltage	V _{CC} = 2.3 V; I _{OH} = -8 mA		1.8	2.1	-	1 [×]
		V _{CC} = 2.3 V; I _{OL} = 100 μA		-	0.07	0.2	
V _{OL}	LOW-level output voltage	V _{CC} = 2.3 V; I _{OL} = 24 mA		-	0.3	0.5	V
		V _{CC} = 2.3 V; I _{OL} = 8 mA		-	-	0.4	1
V _{RST}	Power-up output low voltage ⁷	V_{CC} = 2.7 V; I_{O} = 1 mA; V_{I} = V_{CC} or GN	ID	-	-	0.55	V
		V_{CC} = 2.7 V; V_{I} = V_{CC} or GND	Control pins	-	0.1	± 1	
		$V_{CC} = 0 \text{ V or } 2.7 \text{ V; } V_{I} = 5.5 \text{ V}$		-	0.1	10	
I _I	Input leakage current $V_{CC} = 2.7 \text{ V}; \text{ V}_{I} = 5.5 \text{ V}$ $V_{CC} = 2.7 \text{ V}; \text{ V}_{I} = V_{CC}$ Data pins ⁴		-	0.1	20	μA	
		$V_{CC} = 2.7 \text{ V}; \text{ V}_{I} = V_{CC}$	Data pins ⁴	-	0.1	10	
		V _{CC} = 2.7 V; V _I = 0 V	1	-	0.1	-5	
I _{OFF}	Off current	V_{CC} = 0 V; V _I or V _O = 0 V to 4.5 V		-	0.1	± 100	μA
I _{HOLD}	Bus Hold current	$V_{CC} = 2.3 \text{ V}; \text{ V}_{I} = 0.7 \text{ V}$		-	120	-	
HOLD	Data inputs ⁶	V _{CC} = 2.3 V; V _I = 1.7 V		-	-6	-	μA
I _{EX}	Current into an output in the HIGH state when $V_O > V_{CC}$	V _O = 5.5 V; V _{CC} = 2.3 V		_	50	125	μA
I _{PU/PD}	Power-up/down 3-State output current ³	V_{CC} \leq 1.2 V; V_{O} = 0.5 V to $V_{CC};$ V_{I} = GI OE/OE = Don't care	ND or V _{CC} ;	-	40	100	μA
ICCH		$V_{CC} = 2.7 \text{ V}$; Outputs HIGH, $V_{I} = \text{GND}$ (I _O = 0 mA	V_{CC} = 2.7 V; Outputs HIGH, V_I = GND or V_{CC} ; I_O = 0 mA		0.04	0.1	
I _{CCL}	Quiescent supply current	V_{CC} = 2.7 V; Outputs LOW, V _I = GND o	r V _{CC} ;	-	2.6	4.5	mA
I _{CCZ}		V_{CC} = 2.7 V; Outputs disabled; V_{I} = GN I_{O} = 0 mA^{5}	D or V _{CC} ;	_	0.04	0.1	
ΔI_{CC}	Additional supply current per input pin ²	V_{CC} = 2.3 V to 2.7 V; One input at V_{CC} Other inputs at V_{CC} or GND	– 0.6 V;	_	0.01	0.4	mA

NOTES:

All typical values are at V_{CC} = 2.5 V and T_{amb} = 25 °C.
 This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
 This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 msec. From V_{CC} = 1.2 V to V_{CC} = 2.5 V ± 0.2 V a transition time of 100 µsec is permitted. This parameter is valid for T_{amb} = 25 °C only.

4. Unused pins at V_{CC} or GND.

5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.

6. Not guaranteed.

7. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

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AC CHARACTERISTICS (3.3 V \pm 0.3 V RANGE)

GND = 0 V; $t_R = t_F$ = 2.5 ns; C_L = 50 pF; R_L = 500 Ω ; T_{amb} = -40 °C to +85 °C.

SYMBOL	PARAMETER	WAVEFORM	Vcc	3 V	UNIT	
			MIN	TYP ¹	MAX	
t _{PLH} t _{PHL}	Propagation delay nAx to nBx or nBx to nAx	2	0.5 0.5	1.6 1.8	2.6 3.0	ns
t _{PLH}	Propagation delay	1	1.0	2.4	4.0	ns
t _{PHL}	nLEBA to nAx, nLEAB to nBx	2	1.0	2.4	4.0	
t _{PZH}	Output enable time	4	1.0	2.3	4.0	ns
t _{PZL}	nOEBA to nAx, nOEAB to nBx	5	1.0	1.8	3.1	
t _{PHZ}	Output disable time	4	1.0	3.1	4.8	ns
t _{PLZ}	nOEBA to nAx, nOEAB to nBx	5	1.0	2.7	4.2	
t _{PZH}	Output enable time	4	1.0	2.5	4.2	ns
t _{PZL}	nEBA to nAx, nEAB to nBx	5	1.0	1.9	3.1	
t _{PHZ}	Output disable time	4	1.0	2.9	4.9	ns
t _{PLZ}	nEBA to nAx, nEAB to nBx	5	1.0	2.4	4.2	

NOTE:

1. All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

AC SETUP REQUIREMENTS (3.3 V ± 0.3 V RANGE)

GND = 0 V; $t_R = t_F = 2.5 \text{ ns}$; $C_L = 50 \text{ pF}$; $R_L = 500 \Omega$; $T_{amb} = -40 \text{ °C to } +85 \text{ °C}$.

			LIMITS		
SYMBOL	PARAMETER	WAVEFORM	V _{CC} = 3.3	V_{CC} = 3.3 V \pm 0.3 V	
			MIN	ТҮР	
t _s (H) t _s (L)	Setup time nAx to nLEAB, nBx to nLEBA	3	0.5 0.7	0 -0.4	ns
t _h (H) t _h (L)	Hold time nAx to nLEAB, nBx to nLEBA	3	1.5 1.5	0.2 -0.3	ns
t _s (H) t _s (L)	Setup time nAx to nEAB, nBx to nEBA	3	0.5 1.1	-0.3 -0.6	ns
t _h (H) t _h (L)	Hold time nAx to nEAB, nBx to nEBA	3	1.2 2.0	0.6 0.1	ns
t _W (L)	Latch enable pulse width, LOW	3	1.5	_	ns

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AC CHARACTERISTICS (2.5 V \pm 0.2 V RANGE)

GND = 0 V; $t_R = t_F = 2.5$ ns; $C_L = 50$ pF; $R_L = 500 \Omega$; $T_{amb} = -40 \ ^\circ C$ to +85 $^\circ C$.

SYMBOL	PARAMETER	WAVEFORM	Vcc	UNIT		
			MIN	TYP ¹	MAX	1
t _{PLH} t _{PHL}	Propagation delay nAx to nBx or nBx to nAx	2	1.0 1.0	1.8 2.7	5.1 4.5	ns
t _{PLH}	Propagation delay	1	1.5	3.9	6.4	ns
t _{PHL}	nLEBA to nAx, nLEAB to nBx	2	1.5	3.6	5.9	
t _{PZH}	Output enable time	4	1.5	4.0	6.5	ns
t _{PZL}	nOEBA to nAx, nOEAB to nBx	5	1.5	2.7	4.6	
t _{PHZ}	Output disable time	4	1.5	3.7	5.6	ns
t _{PLZ}	nOEBA to nAx, nOEAB to nBx	5	1.5	2.6	4.0	
t _{PZH}	Output enable time	4	1.5	4.2	7.0	ns
t _{PZL}	nEBA to nAx, nEAB to nBx	5	1.5	2.8	5.0	
t _{PHZ}	Output disable time	4	1.5	3.6	5.6	ns
t _{PLZ}	nEBA to nAx, nEAB to nBx	5	1.5	2.4	3.9	

NOTE:

1. All typical values are at V_{CC} = 2.5 V and T_{amb} = 25 °C.

AC SETUP REQUIREMENTS (2.5 V ± 0.2 V RANGE)

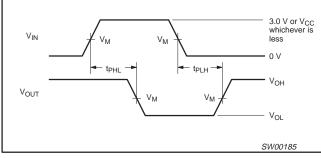
GND = 0 V; $t_R = t_F = 2.5 \text{ ns}$; $C_L = 50 \text{ pF}$; $R_L = 500 \Omega$; $T_{amb} = -40 \text{ °C to } +85 \text{ °C}$.

	PARAMETER	WAVEFORM	LIMITS		UNIT
SYMBOL			V_{CC} = 2.5 V \pm 0.2 V		
			MIN	TYP	
t _s (H) t _s (L)	Setup time nAx to nLEAB, nBx to nLEBA	3	0.5 1.0	0.2 0.5	ns
t _h (H) t _h (L)	Hold time nAx to nLEAB, nBx to nLEBA	3	1.0 1.0	0.2 0.2	ns
t _s (H) t _s (L)	Setup time nAx to nEAB, nBx to nEBA	3	0.5 1.5	-0.3 -0.6	ns
t _h (H) t _h (L)	Hold time nAx to nEAB, nBx to nEBA	3	1.2 1.5	0 0.2	ns
t _W (L)	Latch enable pulse width, LOW	3	1.5	_	ns

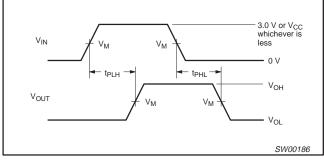
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AC WAVEFORMS

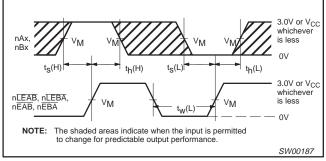
For all waveforms V_M = 1.5 V or V_{CC}/2, whichever is less.



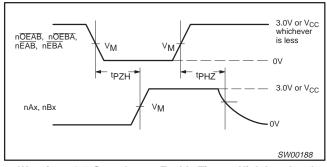
Waveform 1. Propagation Delay For Inverting Output



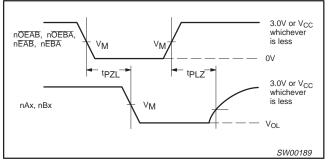
Waveform 2. Propagation Delay For Non-Inverting Output



Waveform 3. Data Setup and Hold Times and Latch Enable Pulse Width



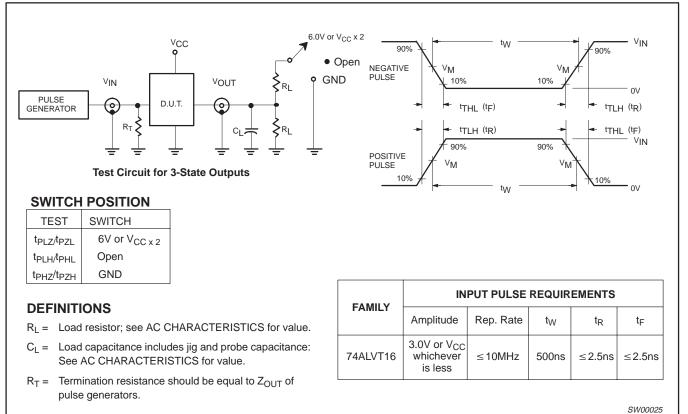
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



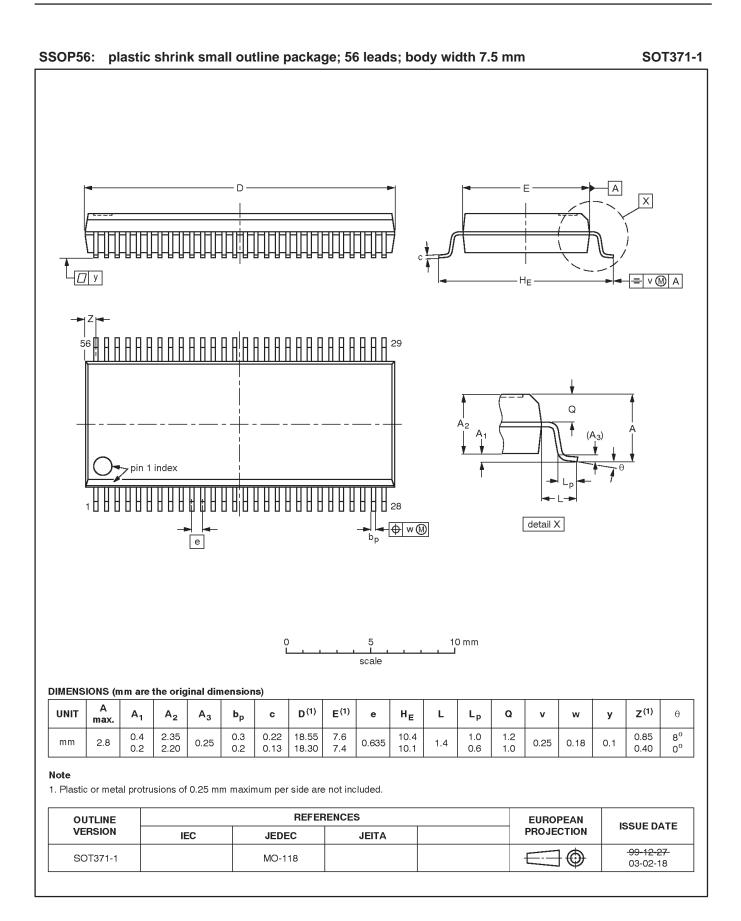
Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

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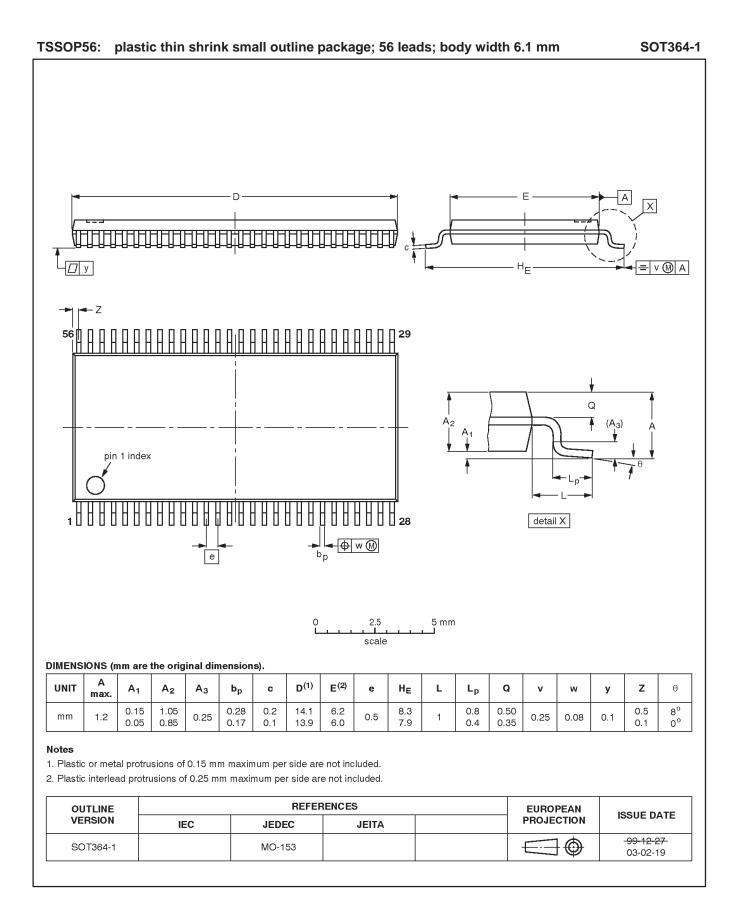
TEST CIRCUIT AND WAVEFORMS



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74ALVT16543



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REVISION HISTORY

Rev	Date	Description		
3	Date 20040914	 Product data sheet (9397 750 14059). Supersedes data of 1998 Feb 13 (9397 750 03568). Modifications: Ordering information table on page 2: remove "North America" column; rename third column from "Outside North America" to "Type Number". DC Electrical Characteristics (3.3 V ± 0.3 V range) table on page 6: I₁ on Data pins: add condition 'V{CC} = 3.6 V; V₁ = 5.5 V' and values 0.1 µA (typ) and 20 µA (max). AC Characteristics (3.3 V ± 0.3 V range) table on page 8: change propagation delay nAx to nBx t_{PLH} Max. time from 2.5 ns to 2.6 ns change output disable time nOEBA to nAx, nOEAB to nBx t_{PLZ} (Max.) time from 4.7 ns to 4.8 ns change output disable time nOEBA to nAx, nOEAB to nBx t_{PLZ} (Max.) time from 4.0 ns to 4.2 ns change output disable time nEBA to nAx, nEAB to nBx t_{PLZ} (Max.) time from 4.5 ns to 4.9 ns change output disable time nEBA to nAx, nEAB to nBx t_{PLZ} (Max.) time from 3.8 ns to 4.2 ns 		
		 AC Setup Requirements (3.3 V ± 0.3 V range) table on page 8: change setup time nAx to nLEAB, nBx to nLEBA t_s(H) (Min.) from 0.0 ns to 0.5 ns; (Typ.) from -0.8 ns to 0 ns change setup time nAx to nLEAB, nBx to nLEBA t_s(L) (Typ.) from -0.3 ns to -0.4 ns change hold time nAx to nLEAB, nBx to nLEBA t_h(H) (Typ.) from 0.4 ns to 0.2 ns change setup time nAx to nLEAB, nBx to nLEBA t_h(L) (Typ.) from 0.8 ns to -0.3 ns change setup time nAx to nLEAB, nBx to nLEBA t_s(L) (Typ.) from 0.8 ns to -0.3 ns change setup time nAx to nLEAB, nBx to nLEBA t_s(H) (Typ.) from 0.8 ns to -0.3 ns change setup time nAx to nEAB, nBx to nEBA t_s(L) (Typ.) from -0.8 ns to -0.3 ns change setup time nAx to nEAB, nBx to nEBA t_s(L) (Typ.) from 0.3 ns to -0.6 ns change hold time nAx to nEAB, nBx to nEBA t_s(L) (Typ.) from 0.3 ns to 0.6 ns change hold time nAx to nEAB, nBx to nEBA t_h(L) (Typ.) from 1.1 ns to 0.1 ns AC Setup Requirements (2.5 V ± 0.2 V range) table on page 9: change setup time nAx to nLEAB, nBx to nLEBA t_s(H) (Min.) from 0 ns to 0.5 ns; (Typ.) from -0.9 ns to -0.2 ns change setup time nAx to nLEAB, nBx to nLEBA t_s(L) (Typ.) from 0.2 ns to -0.5 ns change setup time nAx to nLEAB, nBx to nLEBA t_s(L) (Typ.) from 0.2 ns to -0.5 ns change setup time nAx to nLEAB, nBx to nLEBA t_s(L) (Typ.) from 0.8 ns to 1.0 ns; (Typ.) from -0.2 ns to 0.2 ns change hold time nAx to nLEAB, nBx to nLEBA t_s(L) (Min.) from 0.8 ns to 1.0 ns; (Typ.) from -0.2 ns to -0.2 ns 		
		 change setup time nAx to nEAB, nBx to nEBA t_s(H) (Min.) from 0 ns to 0.5 ns; (Typ.) from -1.0 ns to -0.3 ns change setup time nAx to nEAB, nBx to nEBA t_s(L) (Typ.) from 0.4 ns to -0.6 ns change hold time nAx to nEAB, nBx to nEBA t_h(H) (Min.) from 0.5 ns to 1.2 ns; (Typ.) from 0.2 ns to 0 ns change hold time nAx to nEAB, nBx to nEBA t_h(L) (Min.) from 2.0 ns to 1.5 ns; (Typ.) from 1.3 ns to 0.2 ns 		
_2	19980213	Product specification (9397 750 03568). ECN 853-1823 18958 of 13 February 1998. Supersedes data of 1995 Dec 21.		
_1	19951221			

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Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definitions
I	Objective data sheet	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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