DISCRETE SEMICONDUCTORS

DATA SHEET

BT137X-600D Triacs

logic level

Product specification

June 2001



Triacs logic level

BT137X-600D

GENERAL DESCRIPTION

Passivated, sensitive gate triac in a full pack plastic envelope, intended for use in general purpose bidirectional switching and phase control applications. This device is intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

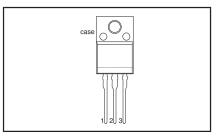
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V _{DRM}	Repetitive peak off-state voltages	600	V
I _{T(RMS)}	RMS on-state current	8	A
I _{TSM}	Non-repetitive peak on-state current	65	A

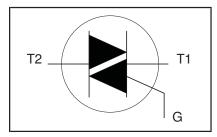
PINNING - SOT186A

PIN	DESCRIPTION			
1	main terminal 1			
2	main terminal 2			
3	gate			
case	isolated			

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DRM}	Repetitive peak off-state voltages		-	600 ¹	V
I _{T(RMS)} I _{TSM}	RMS on-state current Non-repetitive peak on-state current	full sine wave; $T_{hs} \le 73 ^{\circ}\text{C}$ full sine wave; $T_j = 25 ^{\circ}\text{C}$ prior to surge	-	8	А
l ² t	I ² t for fusing	t = 20 ms t = 16.7 ms t = 10 ms	- - -	65 71 21	A A A ² s
dI _T /dt	Repetitive rate of rise of on-state current after triggering	$\begin{array}{c} I_{TM} = 12 \text{ A; } I_{G} = 0.2 \text{ A;} \\ dI_{G}/dt = 0.2 \text{ A/}\mu\text{s} \\ & T2+\text{ G+} \\ & T2+\text{ G-} \\ & T2-\text{ G-} \\ & T2-\text{ G+} \\ \end{array}$	- - -	50 50 50 10	A/μs A/μs A/μs A/μs
$\begin{matrix} I_{GM} \\ V_{GM} \\ P_{GM} \\ P_{G(AV)} \\ T_{stg} \\ T_{j} \end{matrix}$	Peak gate current Peak gate voltage Peak gate power Average gate power Storage temperature Operating junction temperature	over any 20 ms period	- - - -40	2 5 5 0.5 150 125	Α Α V W °C °C

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¹ Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 6 A/ μ s.

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ISOLATION LIMITING VALUE & CHARACTERISTIC

 $T_{hs} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65%; clean and dustfree	-	-	2500	V
C _{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R _{th j-hs}	,	full or half cycle with heatsink compound without heatsink compound	-	-	4.5 6.5	K/W K/W
R _{th j-a}	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_i = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
I _{GT}	Gate trigger current	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}$					
"			!+ G+	-	2.5	5 5 5	mA
			?+ G-	-	3.5	5	mA
		T2	?- G-	-	3.5	5	mA
		T2	?- G+	-	6.5	10	mA
I _I	Latching current	$V_D = 12 \text{ V}; I_{GT} = 0.1 \text{ A}$					
-			2+ G+	-	1.6	15	mA
		T2	2+ G-	-	8.5	20	mA
		T2	2- G-	-	1.2	15	mA
		T2	?- G+	-	2.5	20	mA
l _H	Holding current	$V_D = 12 \text{ V}; I_{GT} = 0.1 \text{ A}$		-	1.5	10	mA
V_{T}	On-state voltage	$I_{T} = 10 \text{ A}$		-	1.3	1.65	V
V _{GT}	Gate trigger voltage	$\dot{V}_{D} = 12 \text{ V}; I_{T} = 0.1 \text{ A}$		-	0.7	1.5	V
		$V_D = 400 \text{ V}$: $I_T = 0.1 \text{ A}$: $T_1 = 125 ^{\circ}\text{C}$		0.25	0.4	-	V
I _D	Off-state leakage current	$V_D^{\prime} = V_{DRM(max)}$; $T_j = 125$ °C		-	0.1	0.5	mA

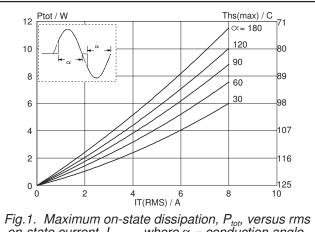
DYNAMIC CHARACTERISTICS

 $T_j = 25$ °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV _D /dt	off-state voltage	$V_{DM} = 67\% V_{DRM(max)}; T_j = 125 °C;$ exponential waveform; $R_{GK} = 1 k\Omega$	-	5	-	V/μs
t _{gt}	Gate controlled turn-on time	$I_{TM} = 12 \text{ A}$; $V_D = V_{DRM(max)}$; $I_G = 0.1 \text{ A}$; $dI_G/dt = 5 \text{ A}/\mu s$	-	2	-	μs

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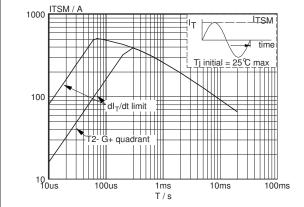


 73° C

8 73° C

8 9_{50} 100 150 150Fig.4. Maximum permissible rms current $I_{T(RMS)}$,

Fig.1. Maximum on-state dissipation, P_{tot} , versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.



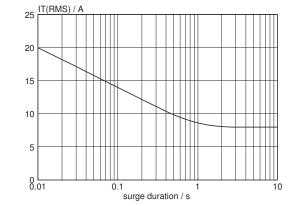
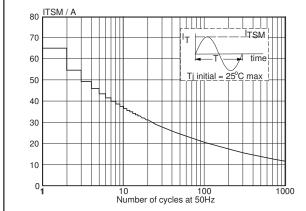


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus pulse width t_p , for sinusoidal currents, $t_p \le 20$ ms.

Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{hs} \le 73$ °C.



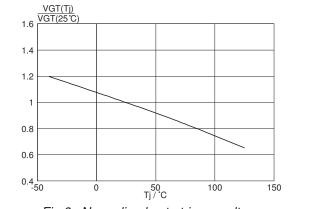
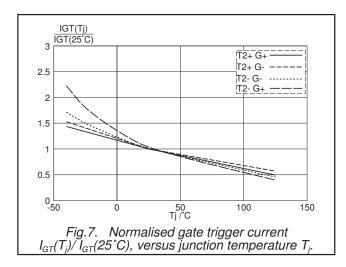


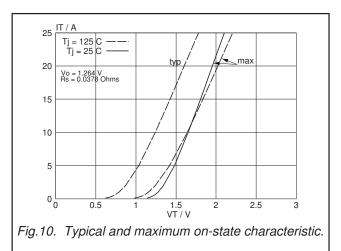
Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM} , versus number of cycles, for sinusoidal currents, f = 50 Hz.

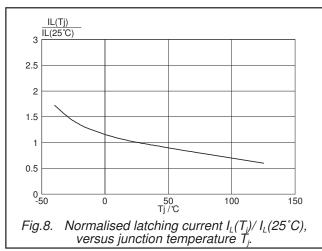
Fig.6. Normalised gate trigger voltage $V_{GT}(T_i)/V_{GT}(25^{\circ}C)$, versus junction temperature T_i .

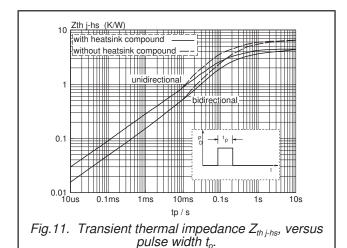
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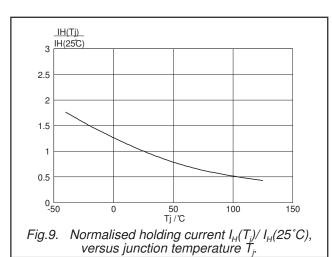
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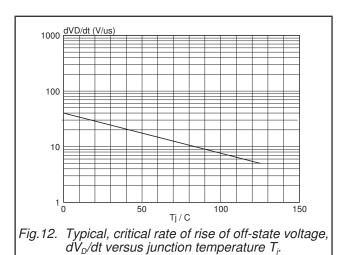






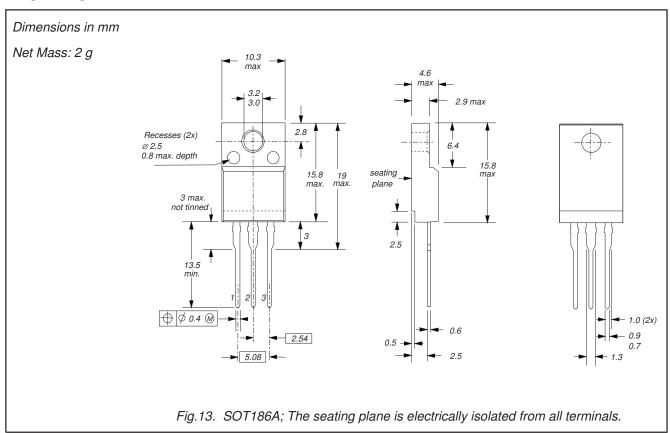






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MECHANICAL DATA



- Refer to mounting instructions for F-pack envelopes.
 Epoxy meets UL94 V0 at 1/8".

Legal information

DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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