

BTA2008-800E

3Q Hi-Com Triac
8 November 2012

Product data sheet

1. Product profile

1.1 General description

Planar passivated high commutation three quadrant triac in a SOT54 (TO-92) plastic package. This "series E" triac balances the requirements of commutation performance and gate sensitivity and is intended for interfacing with low power drivers and logic ICs including microcontrollers.

1.2 Features and benefits

- 3Q technology for improved noise immunity
- Direct gate triggering from low power drivers and logic ICs
- High commutation capability with sensitive gate
- High voltage capability
- Planar passivated for voltage ruggedness and reliability
- Sensitive gate for easy logic level triggering
- Triggering in three quadrants only

1.3 Applications

- Low power motor controls
- Small inductive loads e.g. solenoids, door locks, water valves
- Small loads in large white goods

1.4 Quick reference data

Table 1. Quick reference data

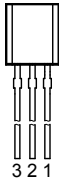
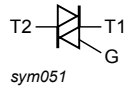
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--------------------------------------|--|-----|-----|-----|------|
| V_{DRM} | repetitive peak off-state voltage | | - | - | 800 | V |
| I_{TSM} | non-repetitive peak on-state current | full sine wave; $T_{\text{j(Init)}} = 25\text{ }^{\circ}\text{C}$; $t_{\text{p}} = 20\text{ ms}$; Fig. 4 ; Fig. 5 | - | - | 9 | A |
| $I_{\text{T(RMS)}}$ | RMS on-state current | full sine wave; $T_{\text{lead}} \leq 70\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3 | - | - | 0.8 | A |
| Static characteristics | | | | | | |
| I_{GT} | gate trigger current | $V_{\text{D}} = 12\text{ V}$; $I_{\text{T}} = 0.1\text{ A}$; T2+ G+; $T_{\text{j}} = 25\text{ }^{\circ}\text{C}$; Fig. 7 | 0.5 | - | 10 | mA |
| | | $V_{\text{D}} = 12\text{ V}$; $I_{\text{T}} = 0.1\text{ A}$; T2+ G-; $T_{\text{j}} = 25\text{ }^{\circ}\text{C}$; Fig. 7 | 0.5 | - | 10 | mA |



| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|---|-----|-----|-----|------|
| | | $V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 7 | 0.5 | - | 10 | mA |

2. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-----------------|--|---|
| 1 | T2 | main terminal 2 |  <p>TO-92 (SOT54)</p> |  <p>sym051</p> |
| 2 | G | gate | | |
| 3 | T1 | main terminal 1 | | |

3. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|--------------|---------|---|---------|
| | Name | Description | Version |
| BTA2008-800E | TO-92 | plastic single-ended leaded (through hole) package; 3 leads | SOT54 |

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------------|--------------------------------------|--|-----|------|------------------|
| V_{DRM} | repetitive peak off-state voltage | | - | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{lead} \leq 70\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3 | - | 0.8 | A |
| I_{TSM} | non-repetitive peak on-state current | full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5 | - | 9 | A |
| | | full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$ | - | 9.9 | A |
| I^2t | I^2t for fusing | $t_p = 10\text{ ms}$; SIN | - | 0.41 | A ² s |
| di_T/dt | rate of rise of on-state current | $I_T = 1.5\text{ A}$; $I_G = 20\text{ mA}$; $di_G/dt = 0.2\text{ A}/\mu\text{s}$ | - | 100 | A/ μs |
| I_{GM} | peak gate current | | - | 1 | A |
| P_{GM} | peak gate power | | - | 2 | W |
| $P_{G(AV)}$ | average gate power | over any 20 ms period | - | 0.1 | W |
| T_{stg} | storage temperature | | -40 | 150 | °C |

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------|----------------------|------------|-----|-----|------|
| T_j | junction temperature | | - | 125 | °C |

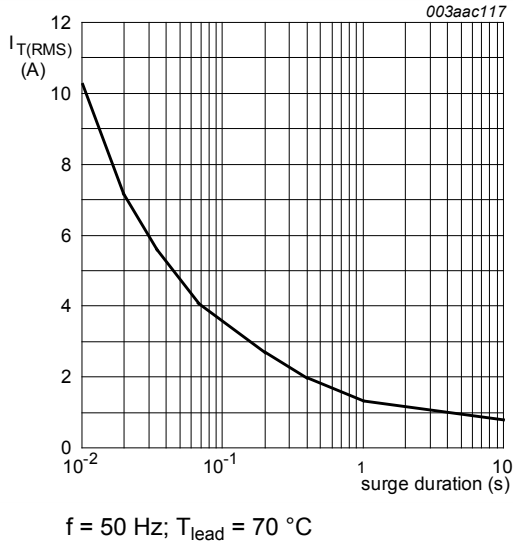


Fig. 1. RMS on-state current as a function of surge duration; maximum values

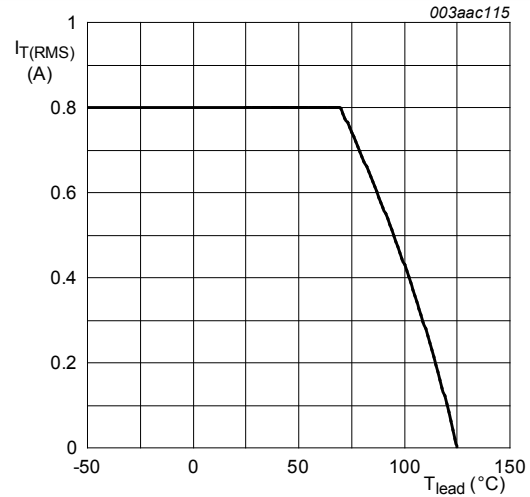


Fig. 2. RMS on-state current as a function of lead temperature; maximum values

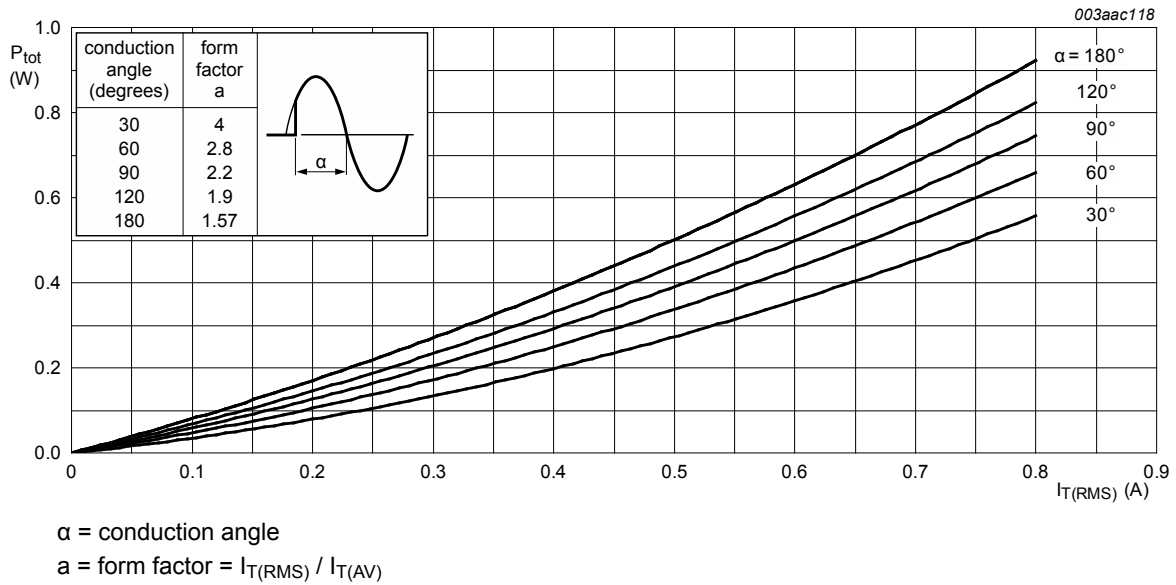


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

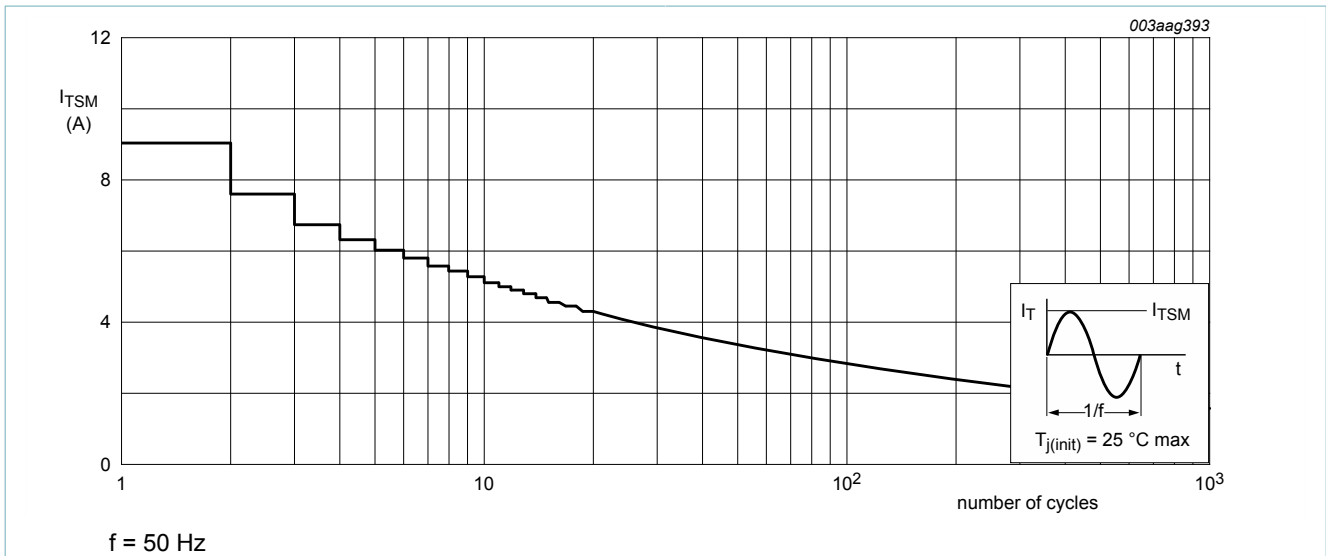


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

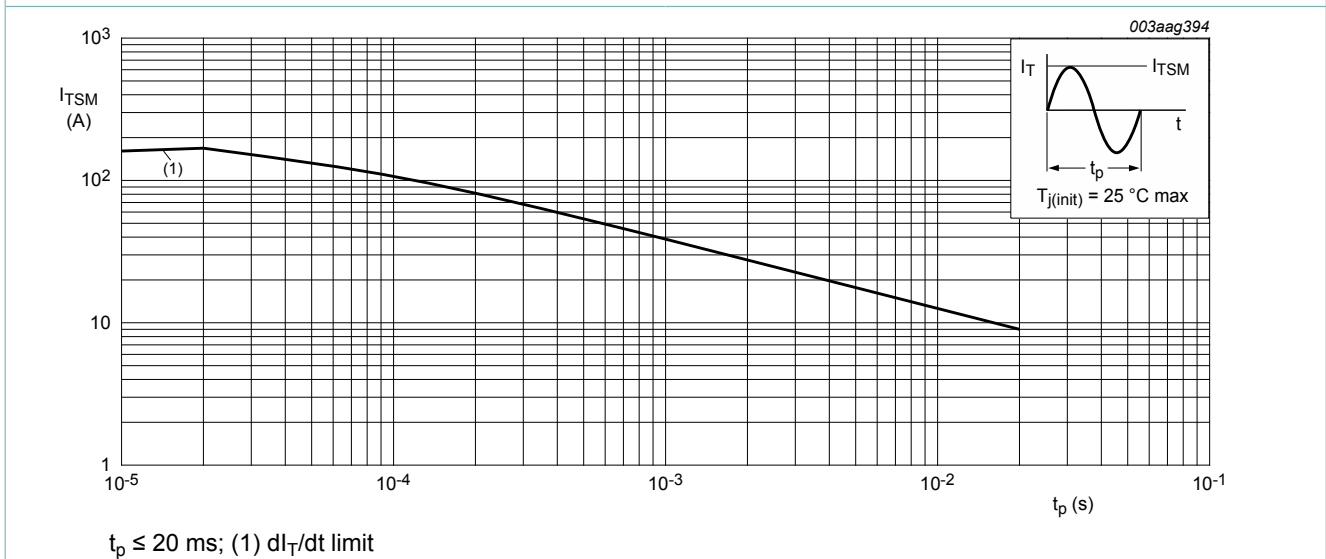


Fig. 5. Non-repetitive peak on-state current as a function of pulse duration; maximum values

5. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|---|---|-----|-----|-----|------|
| $R_{th(j-lead)}$ | thermal resistance from junction to lead | full cycle; Fig. 6 | - | - | 60 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | printed circuit board mounted: lead length = 4 mm | - | 150 | - | K/W |

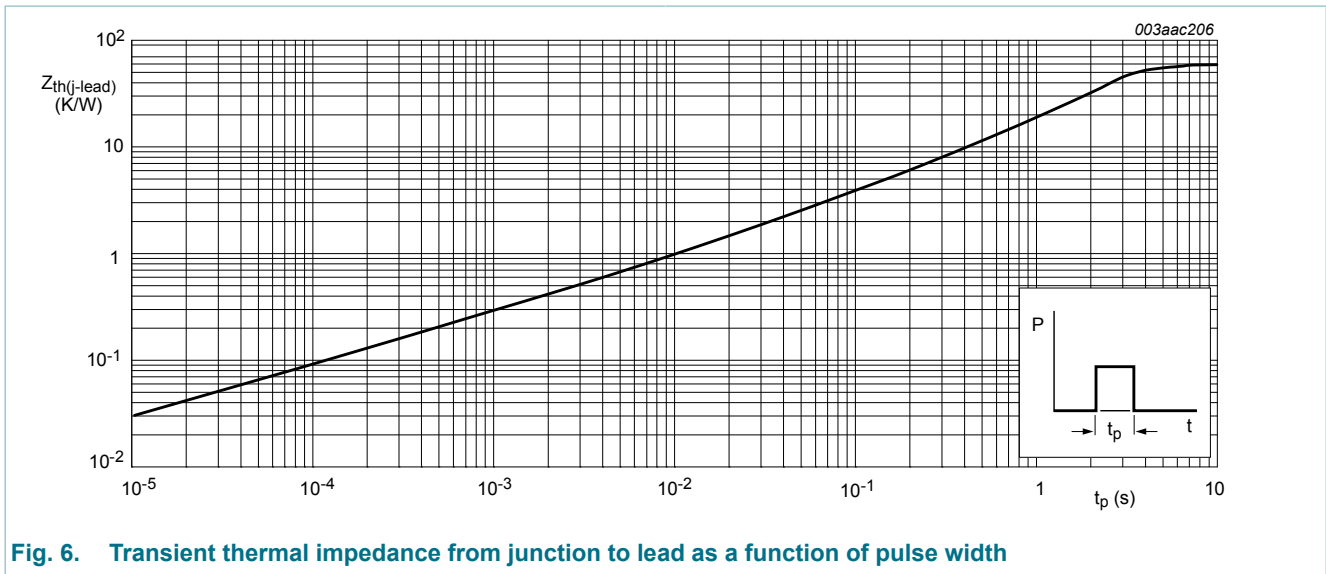


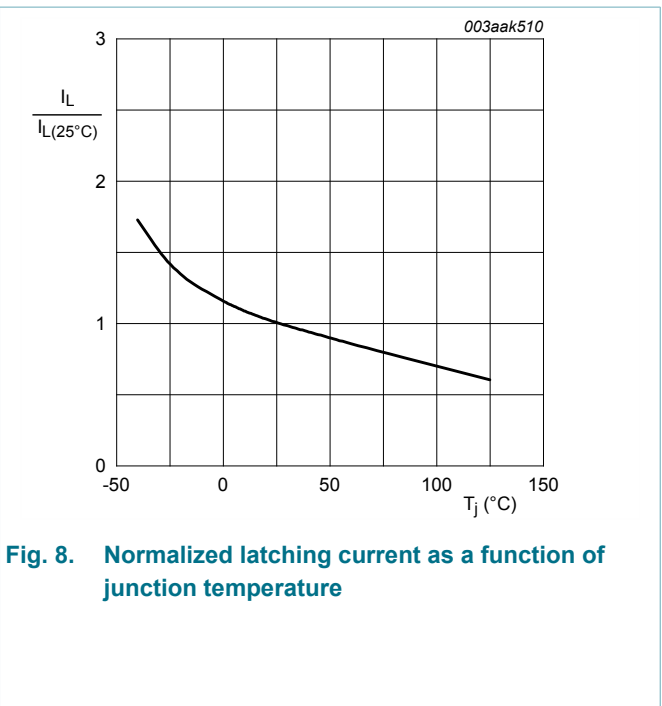
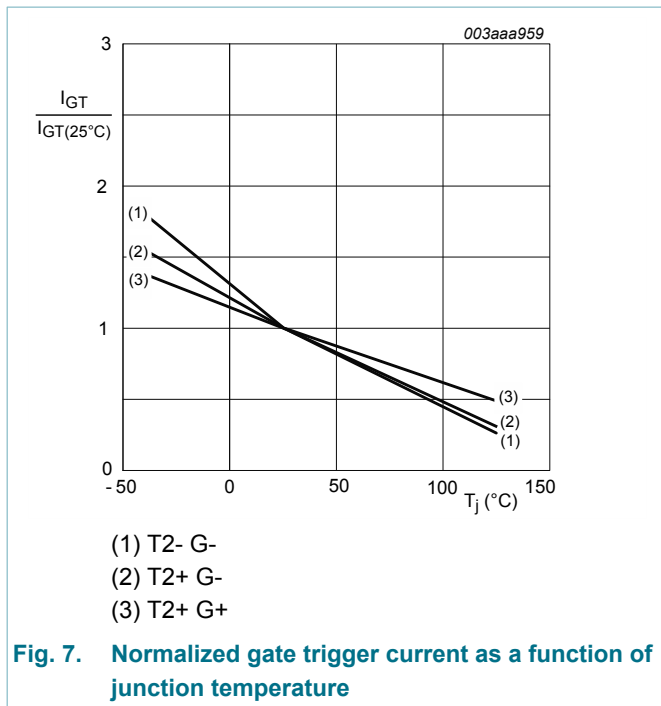
Fig. 6. Transient thermal impedance from junction to lead as a function of pulse width

6. Characteristics

Table 6. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|----------------------|--|-----|------|-----|------|
| Static characteristics | | | | | | |
| I _{GT} | gate trigger current | V _D = 12 V; I _T = 0.1 A; T2+ G+; T _j = 25 °C; Fig. 7 | 0.5 | - | 10 | mA |
| | | V _D = 12 V; I _T = 0.1 A; T2+ G-; T _j = 25 °C; Fig. 7 | 0.5 | - | 10 | mA |
| | | V _D = 12 V; I _T = 0.1 A; T2- G-; T _j = 25 °C; Fig. 7 | 0.5 | - | 10 | mA |
| I _L | latching current | V _D = 12 V; I _G = 0.1 A; T2+ G+; T _j = 25 °C; Fig. 8 | - | - | 12 | mA |
| | | V _D = 12 V; I _G = 0.1 A; T2+ G-; T _j = 25 °C; Fig. 8 | - | - | 20 | mA |
| | | V _D = 12 V; I _G = 0.1 A; T2- G-; T _j = 25 °C; Fig. 8 | - | - | 12 | mA |
| I _H | holding current | V _D = 12 V; T _j = 25 °C; Fig. 9 | - | - | 12 | mA |
| V _T | on-state voltage | I _T = 0.85 A; T _j = 25 °C; Fig. 10 | - | 1.35 | 1.6 | V |
| V _{GT} | gate trigger voltage | V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; Fig. 11 | - | 0.9 | 2 | V |
| | | V _D = 400 V; I _T = 0.1 A; T _j = 125 °C; Fig. 11 | 0.2 | 0.3 | - | V |
| I _D | off-state current | V _D = 800 V; T _j = 125 °C | - | 0.1 | 0.5 | mA |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|---------------------------------------|--|-----|-----|-----|------------------|
| Dynamic characteristics | | | | | | |
| dV_D/dt | rate of rise of off-state voltage | $V_{DM} = 536 \text{ V}$; $T_j = 125 \text{ }^\circ\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit | 600 | - | - | V/ μs |
| dI_{com}/dt | rate of change of commutating current | $V_D = 400 \text{ V}$; $T_j = 125 \text{ }^\circ\text{C}$; $I_{T(RMS)} = 0.8 \text{ A}$; $dV_{com}/dt = 10 \text{ V}/\mu\text{s}$; gate open circuit | 1.6 | - | - | A/ms |



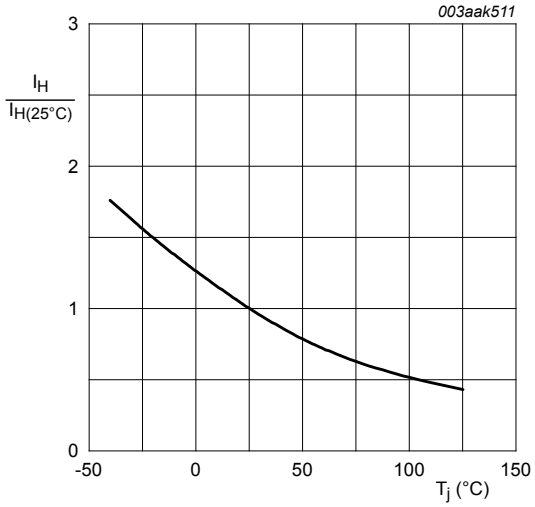
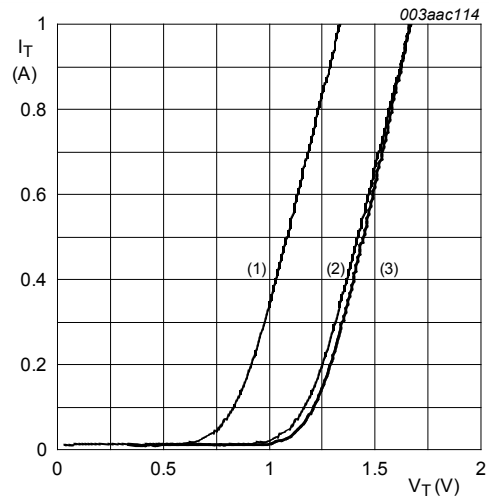


Fig. 9. Normalized holding current as a function of junction temperature



$V_o = 0.835 \text{ V}$; $R_s = 0.50 \Omega$

(1) $T_j = 125^\circ\text{C}$; typical values

(2) $T_j = 125^\circ\text{C}$; maximum values

(3) $T_j = 25^\circ\text{C}$; maximum values

Fig. 10. On-state current as a function of on-state voltage

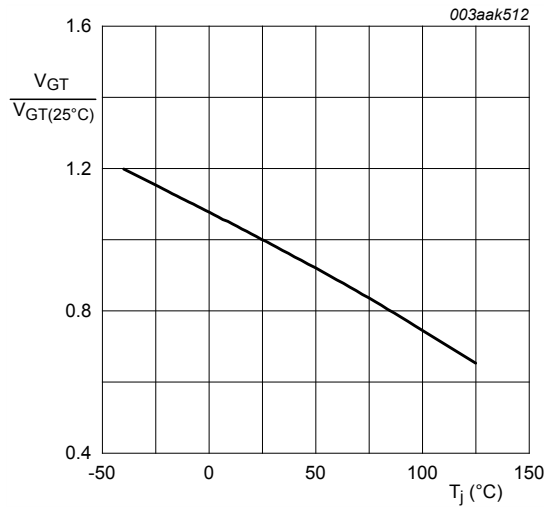
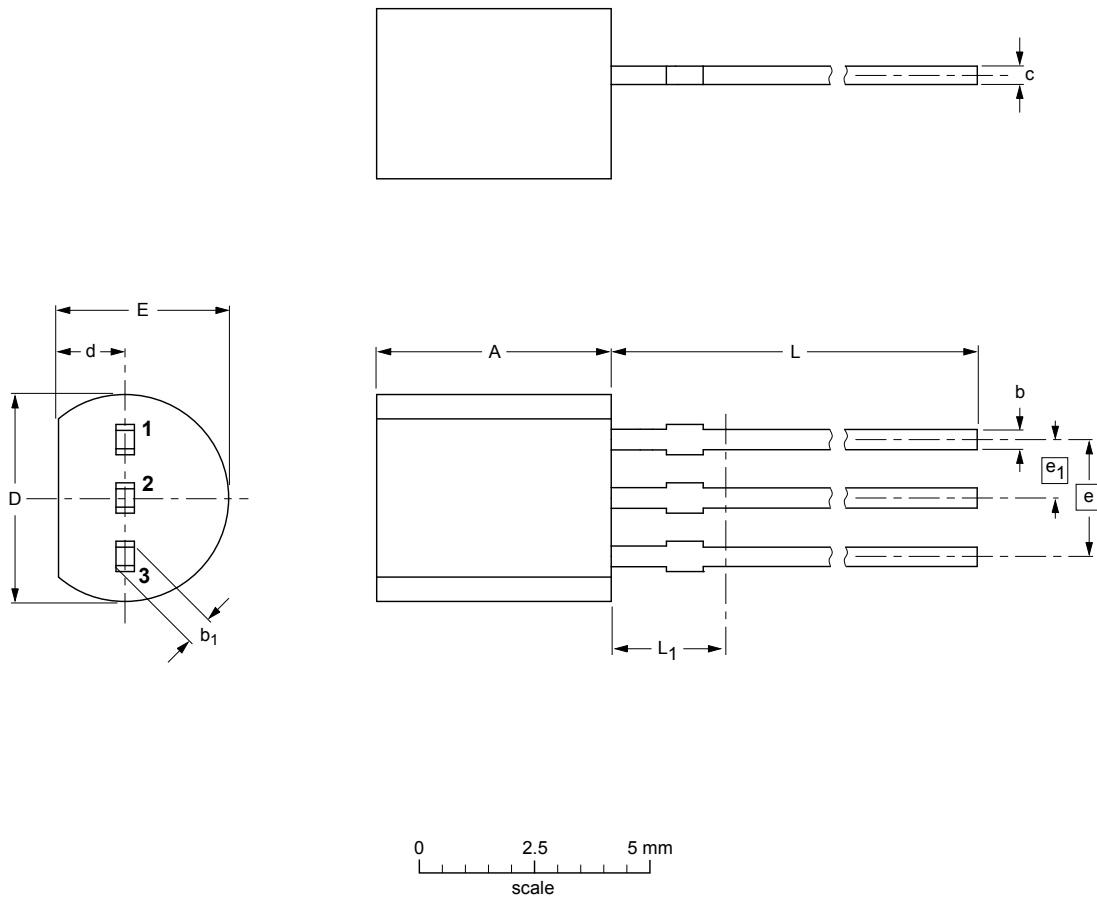


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

7. Package outline

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



DIMENSIONS (mm are the original dimensions)

| UNIT | A | b | b ₁ | c | D | d | E | e | e ₁ | L | L ₁ ⁽¹⁾ max. |
|------|------------|--------------|----------------|--------------|------------|------------|------------|------|----------------|--------------|---------------------------------------|
| mm | 5.2 5.0 | 0.48 0.40 | 0.66 0.55 | 0.45 0.38 | 4.8 4.4 | 1.7 1.4 | 4.2 3.6 | 2.54 | 1.27 | 14.5 12.7 | 2.5 |

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|--------------------|------------|-------|--------|--|------------------------|------------------------|
| | IEC | JEDEC | JEITA | | | |
| SOT54 | | TO-92 | SC-43A | | | -04-06-28- 04-11-16 |

Fig. 12. Package outline TO-92 (SOT54)

8. Legal information

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|--------------------------------|--------------------|---|
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Date of release: 8 November 2012