DLP® 0.55 XGA Series 450 DMD

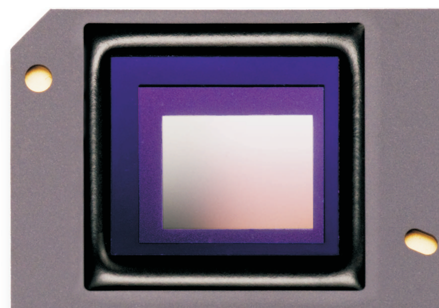
Check for Samples: DLP5500

FEATURES

- 0.55-Inch Micromirror Array Diagonal
  - 1024 × 768 Array of Aluminum, Micrometer-Sized Mirrors (XGA Resolution)
  - 10.8-µm Micromirror Pitch
  - ±12° Micromirror Tilt Angle (Relative to Flat State)
  - Designed for Corner Illumination
- Designed for Use With Broadband Visible Light (420 nm–700 nm):
  - Window Transmission 97% (Single Pass, Through Two Window Surfaces)
  - Micromirror Reflectivity 88%
  - Array Diffraction Efficiency 86%
  - Array Fill Factor 92%
- 16-Bit, Low Voltage Differential Signaling (LVDS) Double Data Rate (DDR) input data bus
- 200 MHz Input Data Clock Rate
- Series 450 Package Characteristics:
  - Thermal Area 18 mm by 12 mm enabling high on screen lumens (>2000 lm)
  - 149 Micro Pin Grid Array Robust electrical connection
  - 32.2 mm by 22.3 mm Package Footprint
  - Package Mates to Amphenol InterCon Systems 450-2.700-L-13.25-149 Socket

APPLICATIONS

- 3D Machine Vision
- 3D Optical Measurement
- Industrial and Medical Imaging
- Medical Instrumentation
- Digital Exposure systems



DESCRIPTION

The DLP5500 Digital Micromirror Device (DMD) is a digitally controlled MOEMS (micro-opto-electromechanical system) spatial light modulator (SLM). When coupled to an appropriate optical system, the DLP5500 can be used to modulate the amplitude, direction, and or phase of incoming (illumination) light.

Architecturally, the DLP5500 is a latchable, electrical-in, optical-out semiconductor device. This architecture makes the DLP5500 well suited for use in applications such as structured lighting, 3D optical metrology, Industrial and Medical imaging, microscopy, and spectroscopy. The compact physical size of the DLP5500 enables integration into portable equipment.

The DLP5500 is one of three components in the DLP 0.55 XGA chip-set (see Figure 1). Proper function and operation of the DLP5500 requires that it be used in conjunction with the other components of the chip-set. The DLPC200 (TI literature number DLPS014) and DLPA200 (TI literature number DLPS015) control and coordinate the data loading and micromirror switching to ensure reliable operation. Refer to DLP 0.55 XGA chip-set data sheet (TI literature number DLPZ004) for further details. DLPR200F is DLPC200 firmware code provided to enable Video and Structured Lighting Applications. To locate the latest version of the DLPR200F, go to www.ti.com and search keyword "DLPR200".

Electrically, the DLP5500 consists of a two-dimensional array of 1-bit CMOS memory cells, organized in a square grid of 1024 memory cell columns by 768 memory cell rows. The CMOS memory array is written to on a column-by-column basis, over a 16-bit Low Voltage Differential Signaling (LVDS) double data rate (DDR) bus. Row addressing is handled via a serial control bus. The specific CMOS memory access protocol is handled by the DLPC200 Digital Controller.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DLP is a registered trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2010–2012, Texas Instruments Incorporated

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION CONTINUED

DLPC200
DLP5500
Port 1 Data Interface
Port 2 Data Interface
USB Interface
Serial Port Interface
User Nonvolatile Memory Interface
User Static Memory Interface
DMD Interface
DMD_DAT_A(1, 3, 5, 7, 9, 11, 13, 15) P/N
SCTRL_A P/N
DMD_CLK_A P/N
DMD_DAT_B(1, 3, 5, 7, 9, 11, 13, 15) P/N
SCTRL_B P/N
DMD_CLK_B P/N
DMD_PWRDN
SCP_DMD_EN
SCP_DMD_RST_DI
SCP_DMD_RST_DO
SCP_DMD_RST_CLK
Data & Control Receiver
CMOS MEMORY ARRAY
MICROMIRROR ARRAY
CFG_MSEL(3:0)
CFG_ASDI
CFG_ASDO
CFG_CSO
CFG_CLK
Configuration Interface
DLPR200F PROM
DLPR200F
V_{3P3V}
V_{SS}
SCP_DMD_RST_DI
SCP_DMD_RST_DO
SCP_DMD_RST_CLK
SCP_DMD_EN
RST_A(3:0)
RST_MODE(1:0)
RST_SEL(1:0)
RST_OE
RST_STB
RST_RST
RST_IRQ
DLPA200 Interface
DLPA200
MBRST(15:0)
V_{1P2V}
V_{1P8V}
V_{2P5V}
V_{3P3V}
V_{VCCA}
V_{CCD_PLL}
V_{CCA_PLL}
V_{SS}
V_{CC}
V_{12V}
V_{BIAS}
V_{OFFSET}
V_{RST}
Sync Out Interface
Illumination Interface
V_{CC}
V_{CC2}
V_{CCI}
V_{SS}

Figure 1. Block Diagram of 0.55 XGA Chipset

Copyright © 2010–2012, Texas Instruments Incorporated

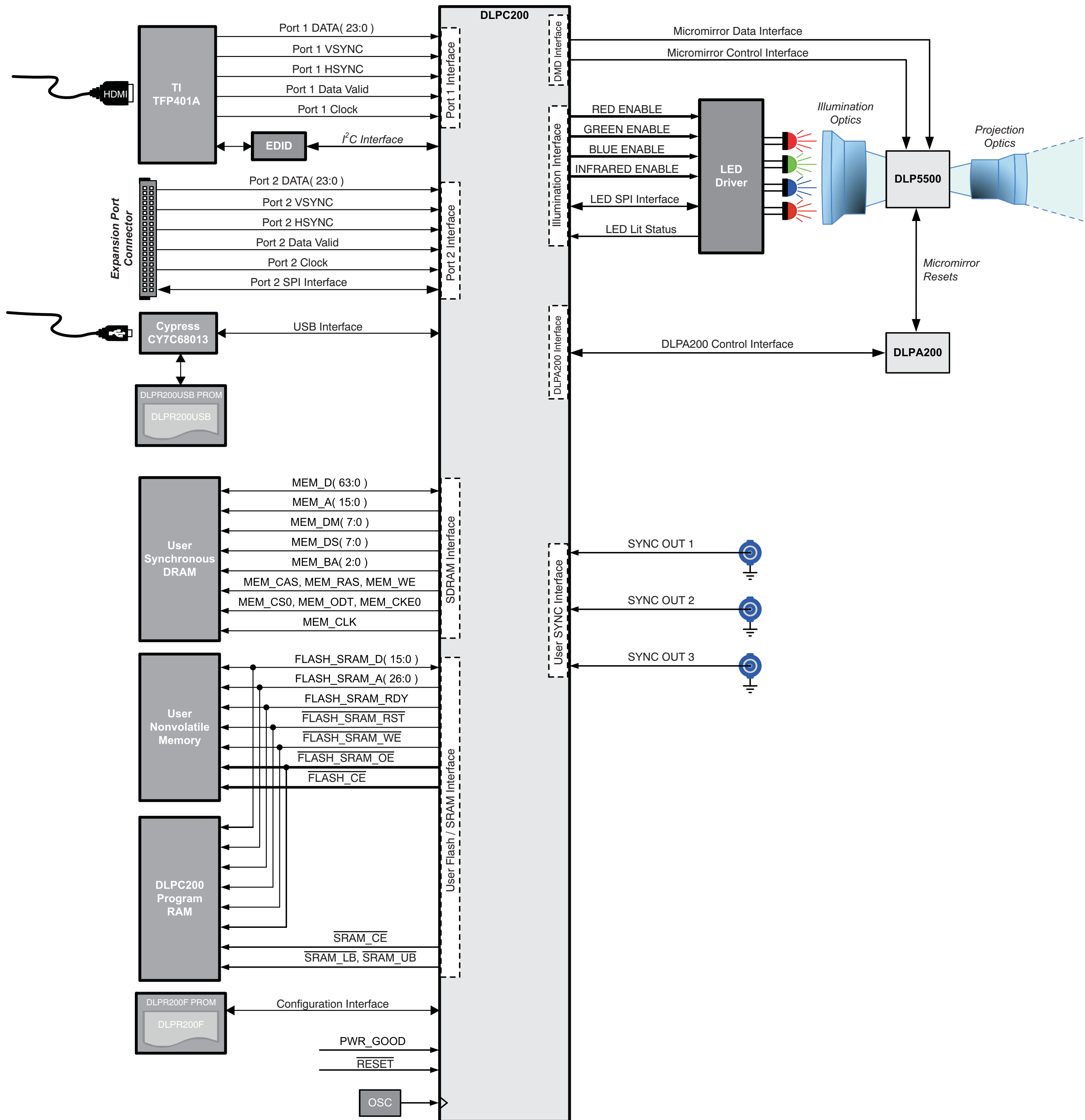


Figure 2. Typical Application

Copyright © 2010–2012, Texas Instruments Incorporated

Optically, the DLP5500 consists of 786,432 highly reflective, digitally switchable, micrometer-sized mirrors (“micromirrors”), organized in a two-dimensional array of 1024 micromirror columns by 768 micromirror rows (Figure 3). Each aluminum micromirror is approximately 10.8 microns in size (refer to “Micromirror Pitch” in Figure 3), and is switchable between two discrete angular positions: –12° and +12°. The angular positions are measured relative to a 0° “flat state”, which is parallel to the array plane (see Figure 4). The tilt direction is perpendicular to the hinge-axis which is positioned diagonally relative to the overall array. The “On State” landed position is directed towards “Row 0, Column 0” corner of the device package (refer to “Micromirror Hinge-Axis Orientation” in Figure 3). In the field of visual displays, the 1024 by 768 “pixel” resolution is referred to as "XGA".

Each individual micromirror is positioned over a corresponding CMOS memory cell. The angular position of a specific micromirror is determined by the binary state (logic 0 or 1) of the corresponding CMOS memory cell contents, after the mirror "clocking pulse" is applied. The angular position (–12° or +12°) of the individual micromirrors changes synchronously with a micromirror “clocking pulse”, rather than being synchronous with the CMOS memory cell data update. Therefore, writing a logic 1 into a memory cell followed by a mirror reset will result in the corresponding micromirror switching to a +12° position. Writing a logic 0 into a memory cell followed by a mirror reset will result in the corresponding micromirror switching to a –12° position.

Operationally, updating the angular position of the micromirror array consists of first updating the contents of the CMOS memory, followed by application of a Mirror Reset to all or a portion of the micromirror array (depending upon the configuration of the system). Mirror Reset pulses are generated by the DLPA200, with application of the pulses being coordinated by the DLPC200 controller.

Around the perimeter of the 1024 by 768 array of micromirrors is a uniform band of “border” micromirrors. The border micromirrors are not user-addressable. The border micromirrors land in the –12° position once power has been applied to the device. There are 10 border micromirrors on each side of the 1024 by 768 active array.

Copyright © 2010–2012, Texas Instruments Incorporated

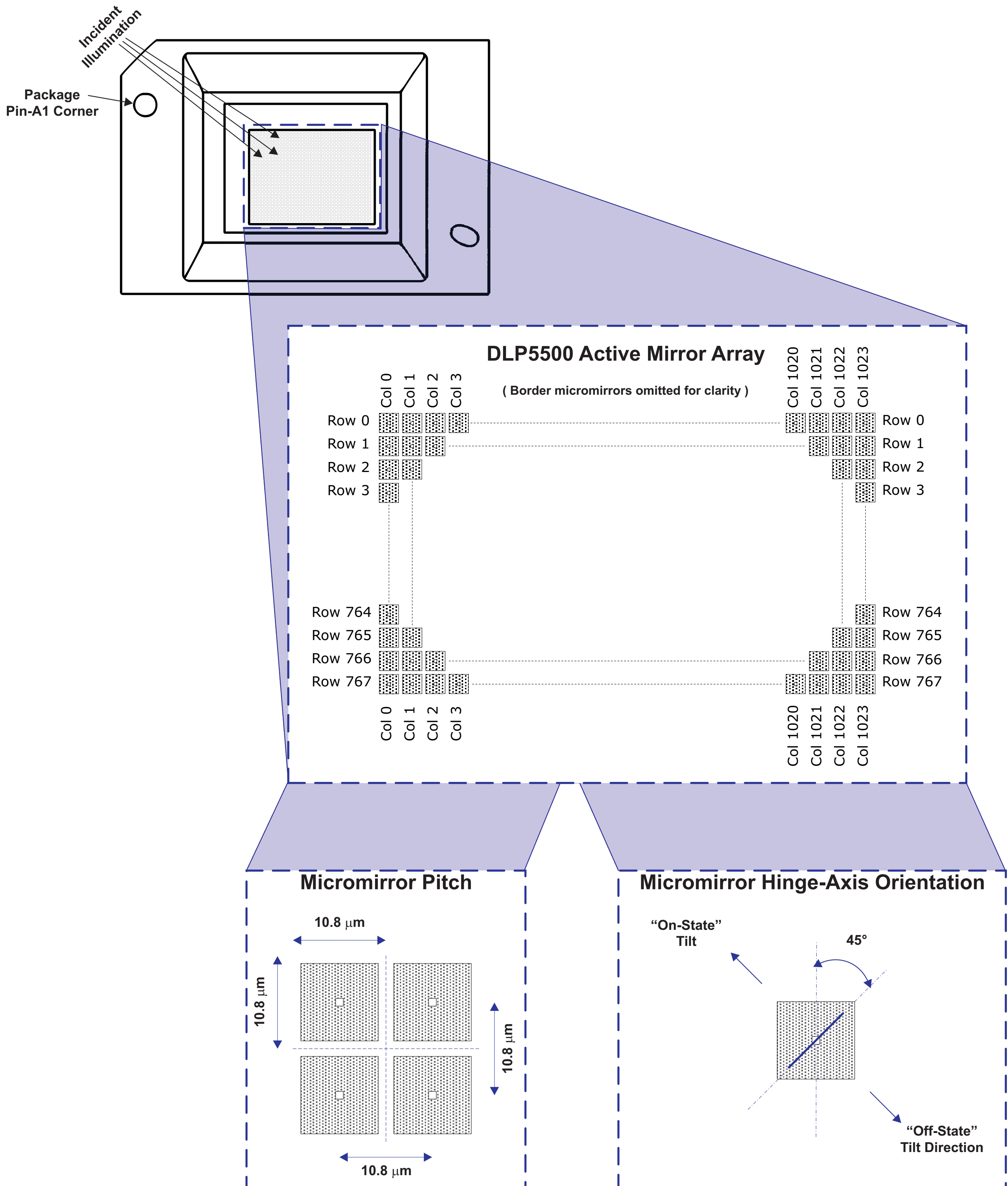


Figure 3. DMD Micromirror Array, Pitch, and Hinge-Axis Orientation

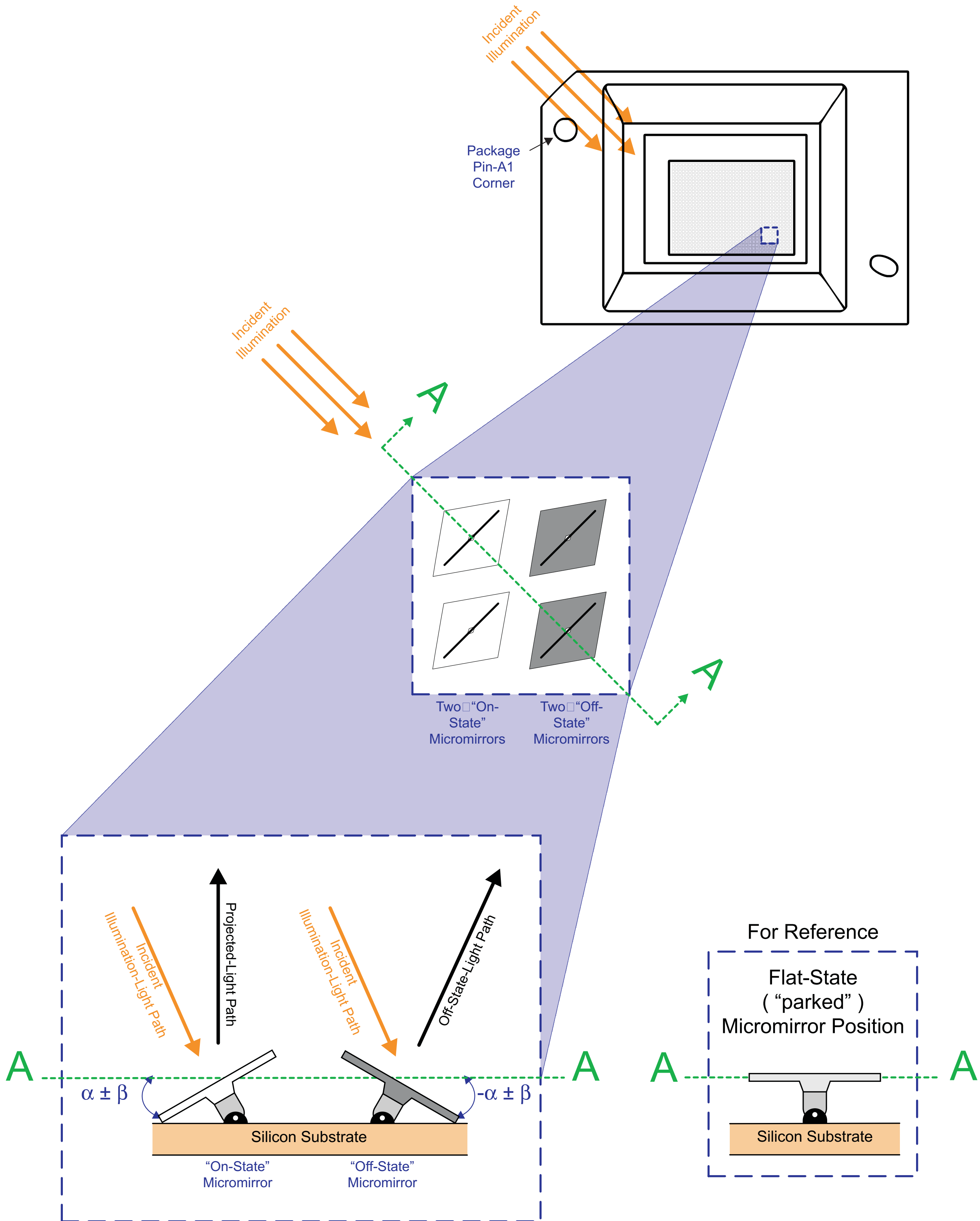


Figure 4. Micromirror Landed Positions and Light Paths

Copyright © 2010–2012, Texas Instruments Incorporated

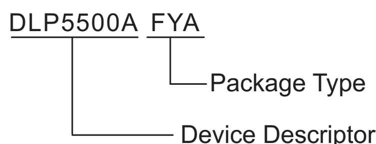
Related Documents

The following documents contain additional information related to the use of the DLP5500 device:

Related Documents

DOCUMENT	TI LITERATURE NUMBER
DLP 0.55 XGA Chip-Set data sheet	DLPZ004
DLPC200 Digital Controller data sheet	DLPS014
DLPA200 DMD Analog Reset Driver	DLPS015
DLP Series-450 DMD and System Mounting Concepts	DLPA015
DLPC200 API Reference Manual	DLPA024
DLPC200 API Programmer's Guide	DLPA014
s4xx DMD Cleaning Application Note	DLPA025
s4xx DMD Handling Application Note	DLPA019

Device Part Number Nomenclature



Device Marking

The device marking consists of the fields shown in Figure 5.

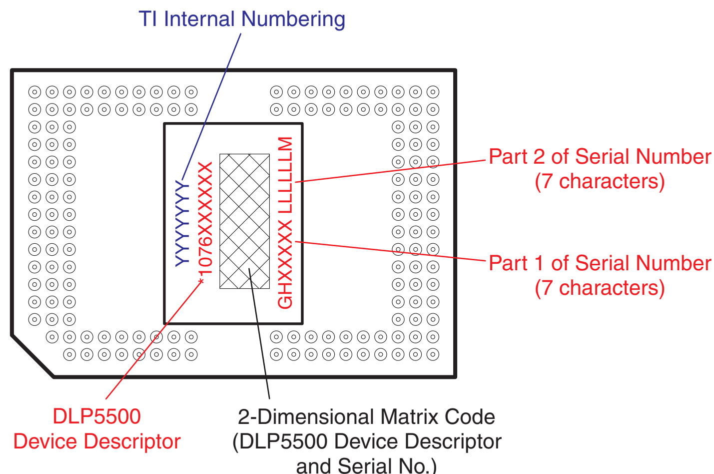


Figure 5. DMD Marking (Device Top View)

Copyright © 2010–2012, Texas Instruments Incorporated

Device Terminals

This section describes the input and output characteristics of signals that interface to the DLP5500, organized by functional groups. Below table includes I/O, Type, Internal Termination, Clock Domain and Data Rate characteristics that are further described in subsequent sections.

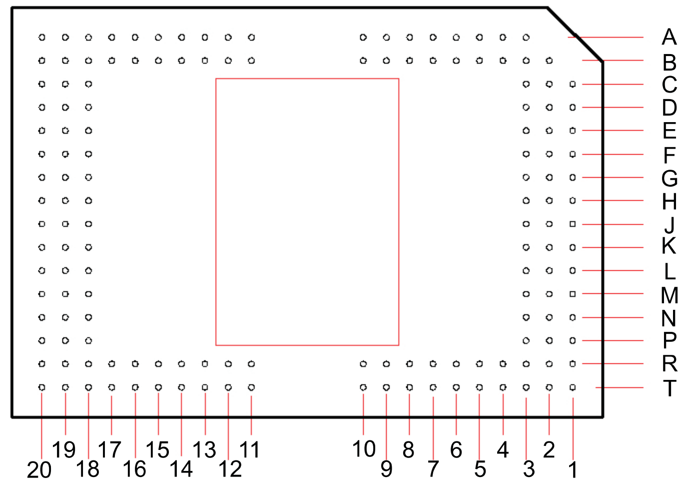


Figure 6. Series 450 Package Terminals (Device Bottom View)

Copyright © 2010–2012, Texas Instruments Incorporated

TERMINAL NAME	PIN See Figure 6	I/O/P	TYPE	INTERNAL TERMINATION	CLOCKED BY	Internal Trace Length (mils)[1]	DATA RATE	DESCRIPTION
Data Inputs								
D_AN1	G20	Input	LVCMOS	Differential Terminated	DCLK_A	715	LVDS	Input data bus A
D_AP1	H20	Input	LVCMOS	Differential Terminated	DCLK_A	744	LVDS	
D_AN3	H19	Input	LVCMOS	Differential Terminated	DCLK_A	688	LVDS	
D_AP3	G19	Input	LVCMOS	Differential Terminated	DCLK_A	703	LVDS	
D_AN5	F18	Input	LVCMOS	Differential Terminated	DCLK_A	686	LVDS	
D_AP5	G18	Input	LVCMOS	Differential Terminated	DCLK_A	714	LVDS	
D_AN7	E18	Input	LVCMOS	Differential Terminated	DCLK_A	689	LVDS	
D_AP7	D18	Input	LVCMOS	Differential Terminated	DCLK_A	705	LVDS	
D_AN9	C20	Input	LVCMOS	Differential Terminated	DCLK_A	687	LVDS	
D_AP9	D20	Input	LVCMOS	Differential Terminated	DCLK_A	715	LVDS	
D_AN11	B18	Input	LVCMOS	Differential Terminated	DCLK_A	715	LVDS	
D_AP11	A18	Input	LVCMOS	Differential Terminated	DCLK_A	732	LVDS	
D_AN13	A20	Input	LVCMOS	Differential Terminated	DCLK_A	686	LVDS	
D_AP13	B20	Input	LVCMOS	Differential Terminated	DCLK_A	715	LVDS	
D_AN15	B19	Input	LVCMOS	Differential Terminated	DCLK_A	700	LVDS	
D_AP15	A19	Input	LVCMOS	Differential Terminated	DCLK_A	719	LVDS	
D_BN1	K20	Input	LVCMOS	Differential Terminated	DCLK_B	716	LVDS	Input data bus B
D_BP1	J20	Input	LVCMOS	Differential Terminated	DCLK_B	745	LVDS	
D_BN3	J19	Input	LVCMOS	Differential Terminated	DCLK_B	686	LVDS	
D_BP3	K19	Input	LVCMOS	Differential Terminated	DCLK_B	703	LVDS	
D_BN5	L18	Input	LVCMOS	Differential Terminated	DCLK_B	686	LVDS	
D_BP5	K18	Input	LVCMOS	Differential Terminated	DCLK_B	714	LVDS	
D_BN7	M18	Input	LVCMOS	Differential Terminated	DCLK_B	693	LVDS	
D_BP7	N18	Input	LVCMOS	Differential Terminated	DCLK_B	709	LVDS	
D_BN9	P20	Input	LVCMOS	Differential Terminated	DCLK_B	687	LVDS	
D_BP9	N20	Input	LVCMOS	Differential Terminated	DCLK_B	715	LVDS	
D_BN11	R18	Input	LVCMOS	Differential Terminated	DCLK_B	702	LVDS	
D_BP11	T18	Input	LVCMOS	Differential Terminated	DCLK_B	719	LVDS	
D_BN13	T20	Input	LVCMOS	Differential Terminated	DCLK_B	686	LVDS	
D_BP13	R20	Input	LVCMOS	Differential Terminated	DCLK_B	715	LVDS	
D_BN15	R19	Input	LVCMOS	Differential Terminated	DCLK_B	680	LVDS	
D_BP15	T19	Input	LVCMOS	Differential Terminated	DCLK_B	700	LVDS	
DCLK_AN	D19	Input	LVCMOS	Differential Terminated	–	700	–	Input data bus A Clock
DCLK_AP	E19	Input	LVCMOS	Differential Terminated	–	728	–	
DCLK_BN	N19	Input	LVCMOS	Differential Terminated	–	700	–	Input data bus B Clock
DCLK_BP	M19	Input	LVCMOS	Differential Terminated	–	728	–	
Data Control Inputs								
SCTRL_AN	F20	Input	LVCMOS	Differential Terminated	DCLK_A	716	LVDS	
SCTRL_AP	E20	Input	LVCMOS	Differential Terminated	DCLK_A	731	LVDS	
SCTRL_BN	L20	Input	LVCMOS	Differential Terminated	DCLK_B	707	LVDS	
SCTRL_BP	M20	Input	LVCMOS	Differential Terminated	DCLK_B	722	LVDS	
Serial Communication and Configuration								
SCP_CLK	A8	Input	LVCMOS	pull-down	–	–	–	
SCP_DO	A9	Output	LVCMOS	–	SCP_CLK	–	–	
SCP_DI	A5	Input	LVCMOS	pull-down	SCP_CLK	–	–	
$\overline{\text{SCP_EN}}$	B7	Input	LVCMOS	pull-down	SCP_CLK	–	–	
$\overline{\text{PWRDN}}$	B9	Input	LVCMOS	pull-down	–	–	–	
MODE_A	A4	Input	LVCMOS	pull-down	–	–	–	

(1) Internal Trace Length (mils) refers to the Package electrical trace length. See the DLP 0.55 XGA Chip-Set Data Sheet (TI literature number DLPS012) for details regarding signal integrity considerations for end-equipment designs.

Copyright © 2010–2012, Texas Instruments Incorporated

TERMINAL NAME	PIN See Figure 6	I/O/P	TYPE	INTERNAL TERMINATION	CLOCKED BY	Internal Trace Length (mils)(1)	DATA RATE	DESCRIPTION
Micromirror Bias Reset								
MBRST0	C3	Input	Analog	–	–	–	–	Micromirror Bias Reset "MBRST" signals "clock" micromirrors into state of LVCMOS memory cell associated with each mirror.
MBRST1	D2	Input	Analog	–	–	–	–	
MBRST2	D3	Input	Analog	–	–	–	–	
MBRST3	E2	Input	Analog	–	–	–	–	
MBRST4	G3	Input	Analog	–	–	–	–	
MBRST5	E1	Input	Analog	–	–	–	–	
MBRST6	G2	Input	Analog	–	–	–	–	
MBRST7	G1	Input	Analog	–	–	–	–	
MBRST8	N3	Input	Analog	–	–	–	–	
MBRST9	M2	Input	Analog	–	–	–	–	
MBRST10	M3	Input	Analog	–	–	–	–	
MBRST11	L2	Input	Analog	–	–	–	–	
MBRST12	J3	Input	Analog	–	–	–	–	
MBRST13	L1	Input	Analog	–	–	–	–	
MBRST14	J2	Input	Analog	–	–	–	–	
MBRST15	J1	Input	Analog	–	–	–	–	
Power								
V_{CC}	B11,B12,B13,B16,R12,R13,R16,R17	Power	Analog	–	–	–	–	Power for LVCMOS Logic
V_{CCI}	A12,A14,A16,T12,T14,T16	Power	Analog	–	–	–	–	Power supply for LVDS Interface
V_{CC2}	C1,D1,M1,N1	Power	Analog	–	–	–	–	Power for High Voltage CMOS Logic
V_{SS}	A6,A11,A13,A15,A17,B4,B5,B8,B14,B15,B17,C2,C18,C19,F1,F2,F19,H1,H2,H3,H18,J18,K1,K2,L19,N2,P18,P19,R4,R9,R14,R15,T7,T13,T15,T17	Power	Analog	–	–	–	–	Common return for all power inputs
Reserved Signals (Not for use in system)								
RESERVED_R7	R7	input	LVCMOS	pull-down	–	–	–	Pins should be connected to V_{SS}
RESERVED_R8	R8	input	LVCMOS	pull-down	–	–	–	
RESERVED_T8	T8	input	LVCMOS	pull-down	–	–	–	
RESERVED_B6	B6	input	LVCMOS	pull-down	–	–	–	
NO_CONNECT	A3, A7, A10, B2, B3, B10, E3, F3, K3, L3, P1, P2, P3, R1, R2, R3, R5, R6, R10, R11, T1, T2, T3, T4, T5, T6, T9, T10, T11	–	–	–	–	–	–	DO NOT CONNECT

 Copyright © 2010–2012, Texas Instruments Incorporated

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted). Stresses beyond those listed under " Absolute Maximum Ratings” may cause permanent damage to the device. The Absolute Maximum Ratings are stress ratings only, and functional performance of the device at these or any other conditions beyond those indicated under “ Recommended Operating Conditions” is not implied. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability.

PARAMETER		CONDITIONS	MIN	Nom	MAX	UNIT
Electrical						
V_{CC}	Voltage applied to V_{CC} (1) (2)		–0.5		4	V
V_{CCI}	Voltage applied to V_{CCI} (1) (2)		–0.5		4	V
$\|V_{ID}\|$	Maximum differential voltage, Damage can occur to internal resistor if exceeded, See Figure 10				700	mV
	Delta supply voltage $\|V_{CC} – V_{CCI}\|$				.3	V
V_{CC2}	Voltage applied to V_{OFFSET} (1) (2) (3)		–0.5		9	V
V_{MBRST}	Voltage applied to MBRST[0:15] Input Pins		-28		28	V
	Voltage applied to all other input terminals (1)		–0.5		V_{CC} + 0.3	V
	Current required from a high-level output	V_{OH} = 2.4 V			–20	mA
	Current required from a low-level output	V_{OL} = 0.4 V			15	mA
Environmental						
	Storage temperature range (4) (5)		-40		80	°C
	Storage humidity (4) (5)	Non-Condensing	0		95	% RH
	Illumination power density (4) (6)	< 420 nm (7)			2	mW/cm^2
		420 to 700 (8)				
		> 700 nm			10	
	Electrostatic discharge immunity for LVCMOS pins (9)				2000	V
	Electrostatic discharge immunity for MBRST[0:15] pins				250	

(1) All voltages referenced to V_{SS} (ground).
(2) Voltages V_{CC}, V_{CCI}, and V_{CC2} are required for proper DMD operation.
(3) Exceeding the recommended allowable absolute voltage difference between V_{CC} and V_{CCI} may result in excess current draw. The difference between V_{CC} and V_{CCI}, | V_{CC} - V_{CCI}|, should be less than .3V.
(4) Optimal, long-term performance of the Digital Micromirror Device (DMD) can be affected by various application parameters, including illumination spectrum, illumination power density, micromirror landed duty cycle, ambient temperature (both storage and operating), case temperature, ambient humidity (both storage and operating), and power on or off duty cycle. TI recommends that application-specific effects be considered as early as possible in the design cycle. Contact your local Texas Instruments representative for additional information related to optimizing the DMD performance.
(5) Simultaneous exposure to high storage temperature and high storage humidity may affect device reliability.
(6) Total integrated illumination power density, above or below the indicated wavelength threshold.
(7) The maximum operating conditions for operating temperature and illumination power density for wavelengths < 420 nm shall not be implemented simultaneously.
(8) Limited only by the resulting micromirror array temperature .See the Thermal Characteristics for information related to calculating the micromirror array temperature.
(9) Tested in accordance with JESD22-A114-B Electrostatic Discharge (ESD) sensitivity testing Human Body Model (HBM).

Copyright © 2010–2012, Texas Instruments Incorporated

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the Recommended Operating Conditions. No level of performance is implied when operating the device above or below the Recommended Operating Conditions limits.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Electrical						
V_{CC}	LVCMOS interface supply voltage(1)(2)		3.0	3.3	3.6	V
V_{CCI}	LVCMOS logic supply voltage(1)(2)		3.0	3.3	3.6	V
V_{CC2}	Mirror electrode and HVCMOS supply voltage (1)(2)		8.25	8.5	8.75	V
V_{MBRST}			-27		26.5	V
f_{DCLK_*}	DCLK_A and DCLK_B clock frequency			150		MHz
f_{SCP_CLK}	SCP_CLK Frequency				500	KHz
Mechanical						
	Static load applied to each electrical interface area no. 1 and no. 2, See (3) Figure 7				55	N
	Static load applied to the thermal interface area, See(4) Figure 7				111	N
Environmental						
	Device Operating Temperature	Operating Temperature - Micromirror Array Temperature(5)(6)	10		70	°C
	Operating Case Temperature(7)(3)			26		°C
	Operating Humidity(7)	Non-Condensing		60		% RH
	Operating Device Temperature Gradient(8)				10	°C
	Operating Landed Duty-Cycle(7)(3)			25		%

(1) All voltages referenced to V_{SS} (ground).
(2) Voltages V_{CC}, V_{CCI}, and V_{CC2}, are required for proper DMD operation.
(3) Load should be uniformly distributed across the entire Electrical Interface area #1 and #2.
(4) Load should be uniformly distributed across Thermal Interface Area. Refer to the for size and location of the datum-A surfaces.
(5) Refer to Thermal Characteristics for Thermal Test Point Locations, Package Thermal Resistance, and Device Temperature Calculation.
(6) In some applications, the total DMD heat load can be dominated by the amount of incident light energy absorbed. Refer to the Thermal Characteristics for further details.
(7) Optimal, long-term performance of the Digital Micromirror Device (DMD) can be affected by various application parameters, including illumination spectrum, illumination power density, micromirror landed duty cycle, ambient temperature (both storage and operating), case temperature, ambient humidity (both storage and operating), and power on or off duty cycle. TI recommends that application-specific effects be considered as early as possible in design cycle. Contact your local Texas Instruments representative for additional information related to optimizing the DMD performance.
(8) As measured between any two points on the exterior of the package, or as predicted between any two points inside the micromirror array cavity. See the Thermal Characteristics for information related to calculating the micromirror temperature.

Copyright © 2010–2012, Texas Instruments Incorporated

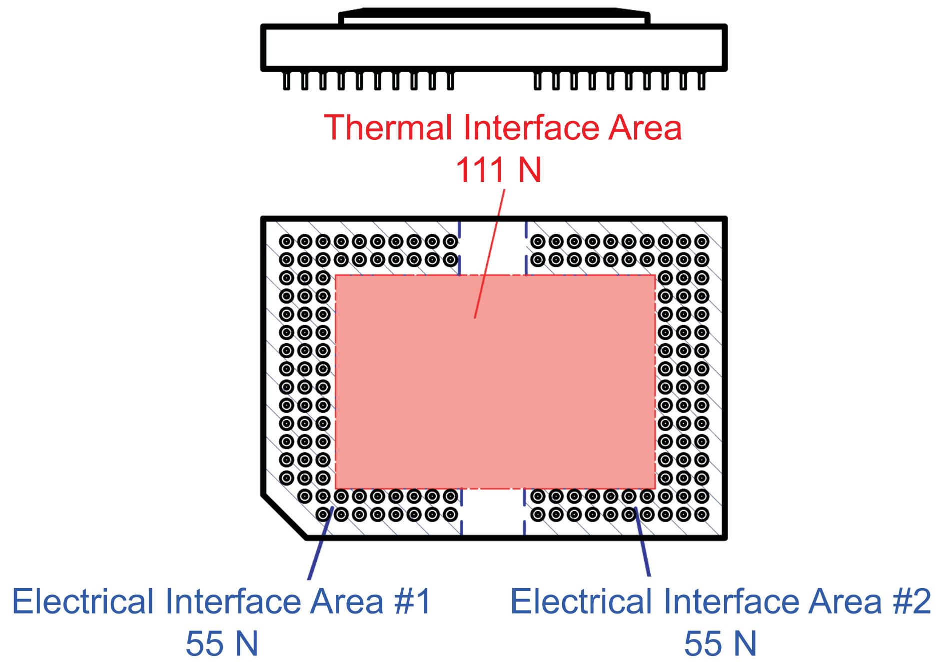


Figure 7. System Interface Loads

Copyright © 2010–2012, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER (Under RECOMMENDED OPERATING CONDITIONS)		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage[1], See Figure 8	V_{CC} = 3.0 V,	I_{OH} = –20 mA	2.4			V
V_{OL}	Low-level output voltage[1], See Figure 8	V_{CC} = 3.6 V,	I_{OH} = 15 mA			0.4	V
I_{OZ}	High impedance output current[1]	V_{CC} = 3.6 V				10	µA
I_{OH}	High-level output current [1]	V_{OH} = 2.4 V, V_{CC} ≥ 3.0 V				–20	mA
		V_{OH} = 1.7 V, V_{CC} ≥ 2.25 V				–15	
I_{OL}	Low-level output current [1]	V_{OL} = 0.4 V, V_{CC} ≥ 3.0 V				15	mA
		V_{OL} = 0.4 V, V_{CC} ≥ 2.25 V				14	
V_{IH}	High-level input voltage[1]			1.7		VCC + .3	V
V_{IL}	Low-level input voltage[1]			-0.3		0.7	V
I_{IL}	Low-level input current[1]	V_{CC} = 3.6 V,	V_I = 0 V			–60	µA
I_{IH}	High-level input current[1]	V_{CC} = 3.6 V,	V_I = V_{CC}			200	µA
I_{CC}	Current into V_{CC} terminal	V_{CC} = 3.6 V,				750	mA
I_{CCI}	Current into V_{OFFSET} terminal[2]	V_{CCI} = 3.6 V				450	mA
I_{CC2}	Current into V_{CC2} terminal	V_{CC2} = 8.75V				25	mA
Z_{IN}	Internal Differential Impedance			95		105	Ω
Z_{LINE}	Line Differential Impedance (PWB or Trace)			90	100	110	Ω
C_I	Input capacitance [1]	f = 1 MHz				10	pF
C_O	Output capacitance [1]	f = 1 MHz				10	pF
C_{IM}	Input capacitance for MBRST[0:15] pins	f = 1 MHz		160		210	pF

(1) Applies to LVCMOS pins only.
(2) Exceeding the maximum allowable absolute voltage difference between V_{CC} and V_{CCI} may result in excess current draw. (Refer to Absolute Maximum Ratings for details)

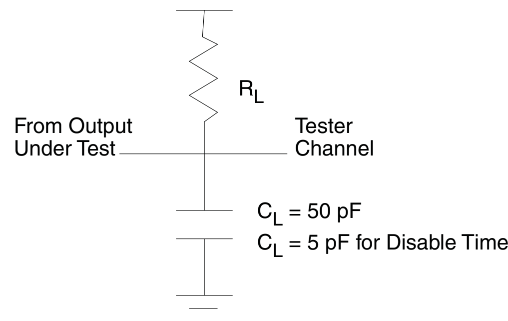


Figure 8. Measurement Condition for LVCMOS Output

Copyright © 2010–2012, Texas Instruments Incorporated

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

LVDS TIMING PARAMETERS See Figure 9		MIN	NOM	MAX	UNIT
t_c	Clock Cycle DLCK_A or DCLKC_B		4.0		ns
t_w	Pulse Width DCLK_A or DCLK_B		1.25		ns
t_s	Setup Time, D_A[0:15] before DCLK_A	.35			ns
t_s	Setup Time, D_B[0:15] before DCLK_B	.35			ns
t_h	Hold Time, D_A[0:15] after DCLK_A	.35			ns
t_h	Hold Time, D_B[0:15] after DCLK_B	.35			ns
t_{skew}	Channel B relative to Channel A	-1.25		1.25	ns
LVDS Waveform Requirements **See Figure 10**					
$\|V_{ID}\|$	Input Differential Voltage (absolute difference)	100	400	600	mV
V_{CM}	Common Mode Voltage		1200		mV
V_{LVDS}	LVDS Voltage	0		2000	mV
t_r	Rise Time (20% to 80%)	100		400	ps
t_r	Fall Time (80% to 20%)	100		400	ps
Serial Control Bus Timing Parameters **See Figure 11 and Figure 12**					
f_{SCP_CLK}	SCP Clock Frequency	50		500	KHz
t_{SCP_SKEW}	Time between valid SCP_DI and rising edge of SCP_CLK	-300		300	ns
t_{SCP_DELAY}	Time between valid SCP_DO and rising edge of SCP_CLK			2600	ns
$t_{\overline{SCP_EN}}$	Time between falling edge of $\overline{\text{SCP_EN}}$ and the first rising edge of SCP_CLK	30			ns
t_{r_SCP}	Rise time for SCP signals			200	ns
t_{fP}	Fall time for SCP signals			200	ns

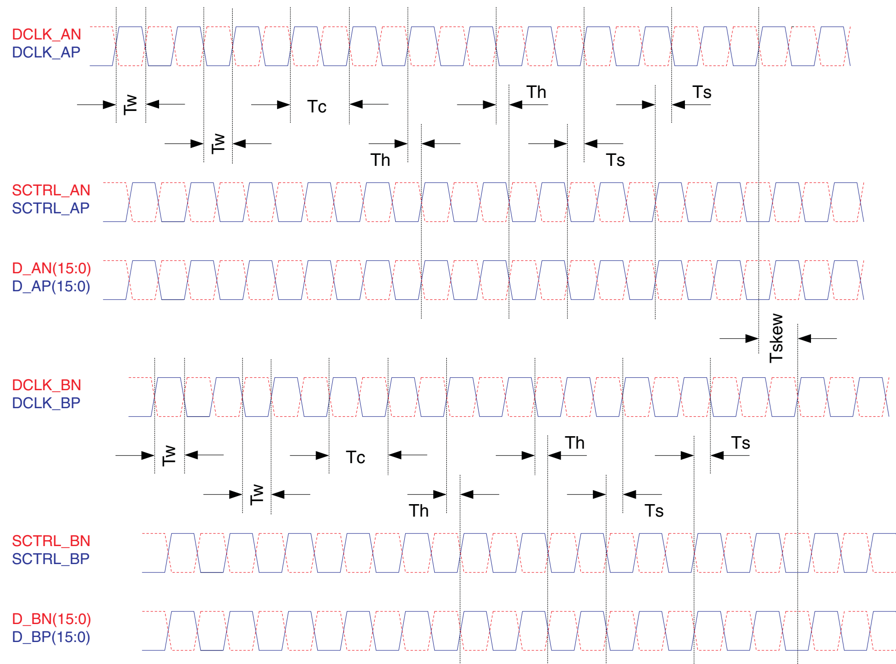


Figure 9. LVDS Timing Waveforms

Copyright © 2010–2012, Texas Instruments Incorporated

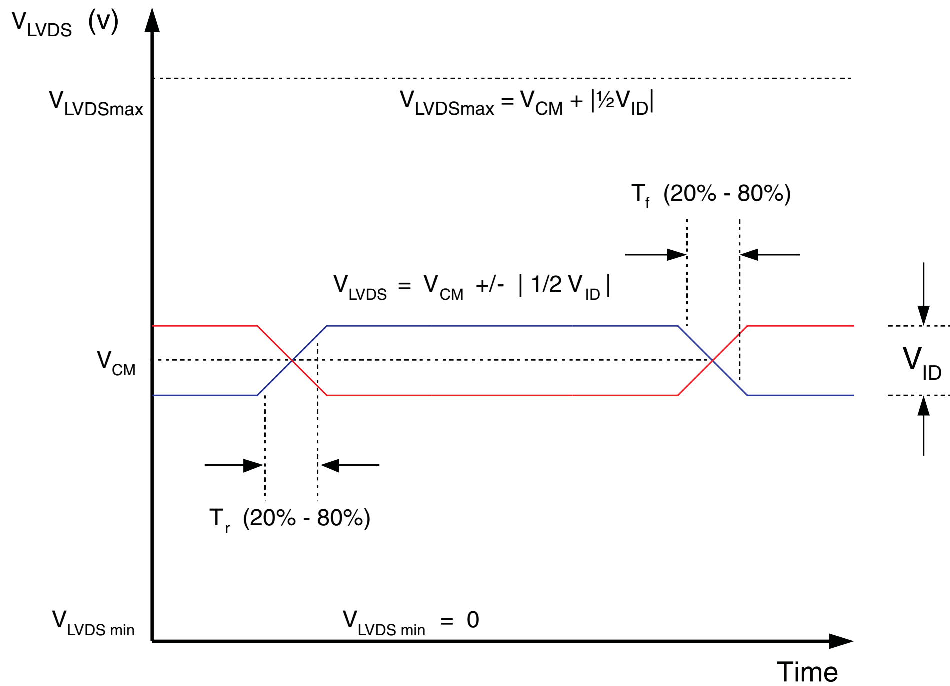


Figure 10. LVDS Waveform Requirements

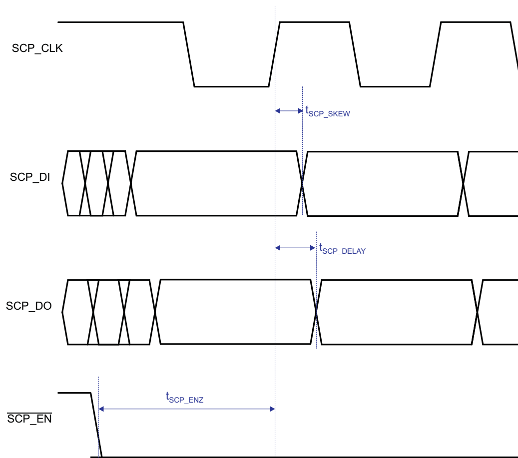


Figure 11. Serial Communications Bus Timing Parameters

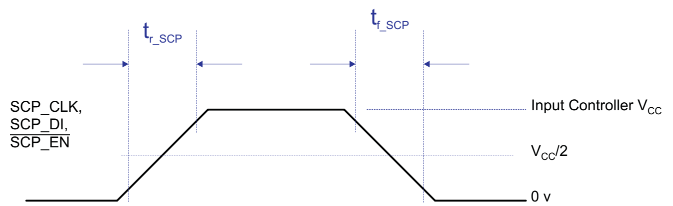


Figure 12. Serial Communications Bus Waveform Requirements

DMD Power-Up and Power-Down Procedures

Repeated failure to adhere to the prescribed power-up and power-down procedures may affect device reliability. The DLP5500 power-up and power-down procedures are defined by the DLPC200 Datasheet (TI Literature number DLPS012) and the .55 XGA Chipset Datasheet (TI Literature number DLPZ004). These procedures must be followed to ensure reliable operation of the device.

 Copyright © 2010–2012, Texas Instruments Incorporated

Micromirror Array Physical Characteristics

Physical characteristics of the micromirror array are provided in . Additional details are provided in the **Package Mechanical Characteristics** section at the end of this document.

Table 1. Micromirror Array Physical Characteristics

PARAMETER	VALUE	UNITS
Number of active micromirror columns[1]	1024	micromirrors
Number of active micromirror rows [1]	768	micromirrors
Micromirror pitch [1]	10.8	microns
Micromirror active array height [1]	768	micromirrors
	8.294	millimeters
Micromirror active array width [1]	1024	micromirrors
	11.059	millimeters
Micromirror array border[2]	10	mirrors or side

(1) See Figure 3
(2) The mirrors that form the array border are hard-wired to tilt in the –12° ("Off") direction once power is applied to the DMD (see Figure 3 and Figure 4).

Micromirror Array Optical Characteristics

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-off's between numerous component and system design parameters. See the following Application Notes for additional details, considerations, and guidelines:

- Single-Panel DLP™ Projection System Optics Application Report (TI literature number DLPA002)

Table 2. Micromirror Array Optical Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Micromirror tilt angle, α	DMD "parked" state[1][2][3], see Figure 4		0		degrees
	DMD "landed" state[1][4][5]see Figure 4		12		
Micromirror tilt angle variation, β [1][4][6][7][8]	See Figure 4	–1		1	degrees
Micromirror Cross Over Time[9]			16	22	us
Micromirror Switching Time[10]			140		us
Non Operating micromirrors[11]	Non-adjacent micromirrors			10	micromirrors
	adjacent micromirrors			0	
Orientation of the micromirror axis-of-rotation[12]	See Figure 3	44	45	46	degrees

(1) Measured relative to the plane formed by the overall micromirror array
(2) "Parking" the micromirror array returns all of the micromirrors to an essentially flat (0˚) state (as measured relative to the plane formed by the overall micromirror array).
(3) When the micromirror array is "parked", the tilt angle of each individual micromirror is uncontrolled.
(4) Additional variation exists between the micromirror array and the package datums, as shown in the **Package Mechanical Characteristics** section at the end of this document.
(5) When the micromirror array is "landed", the tilt angle of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of "1" will result in a micromirror "landing" in an nominal angular position of "+12 degrees". A binary value of 0 will result in a micromirror "landing" in an nominal angular position of "-12 degrees".
(6) Represents the "landed" tilt angle variation relative to the Nominal "landed" tilt angle.
(7) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(8) For some applications, it is critical to account for the micromirror tilt angle variation in the overall System Optical Design. With some System Optical Designs, the micromirror tilt angle variations within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some System Optical Designs, the micromirror tilt angle variation between devices may result in colorimetry variations and/or system contrast variations.
(9) Micromirror Cross Over time is primarily a function of the natural response time of the micromirrors.
(10) Micromirror switching is controlled and coordinated by the DLPC200 (TI Literature number DLPS014) AND DLPA200 (TI Literature number DLPS015). Nominal Switching time depends on the system implementation and represents the time for the entire micromirror array to be refreshed.
(11) Non-operating micromirror is defined as a micromirror that is unable to transition nominally from the -12 degree position to +12 degree or vice versa.
(12) Measured relative to the package datums "B" and "C", shown in the **Package Mechanical Characteristics** section at the end of this document.

Copyright © 2010–2012, Texas Instruments Incorporated

Table 2. Micromirror Array Optical Characteristics (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Micromirror array optical efficiency(13)(14)	420 nm to 700 nm, with all micromirrors in the ON state		68		%
Mirror metal specular reflectivity	400 nm - 700 nm		89.4		%
Illumination Overfill(15)			10		%
Window material			Corning Eagle 2000 or Corning Eagle XG		
Window refractive index	at 546.1 nm		1.5119		
Window flatness(16)	Per 25 mm			4	fringes
Window Artifact Size	Within the Window Aperture(17)(18)			400	um
Window aperture			See (17)		

(13) The minimum or maximum DMD optical efficiency observed in a specific application depends on numerous application-specific design variables, such as:
(a) Illumination wavelength, bandwidth or line-width, degree of coherence
(b) Illumination angle, plus angle tolerance
(c) Illumination and projection aperture size, and location in the system optical path
(d) Illumination overfill of the DMD micromirror array
(e) Aberrations present in the illumination source and/or path
(f) Aberrations present in the projection path
(g) Etc.

The specified nominal DMD optical efficiency is based on the following use conditions:
(a) Visible illumination (420 nm – 700 nm)
(b) Input illumination optical axis oriented at 24° relative to the window normal
(c) Projection optical axis oriented at 0° relative to the window normal
(d) f/3.0 illumination aperture
(e) f/2.4 projection aperture

Based on these use conditions, the nominal DMD optical efficiency results from the following four components:
(a) Micromirror array fill factor: nominally 92%
(b) Micromirror array diffraction efficiency: nominally 86%
(c) Micromirror surface reflectivity: nominally 88%
(d) Window transmission: nominally 97% (single pass, through two surface transitions)

(14) Does not account for the effect of micromirror switching duty cycle, which is application dependant. Micromirror switching duty cycle represents the percentage of time that the micromirror is actually reflecting light from the optical illumination path to the optical projection path. This duty cycle depends on the illumination aperture size, the projection aperture size, and the micromirror array update rate.

(15) The active area of the DLP3000 is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illumination the area outside the active array can create artifacts from the mechanical features that surround the active array and other surface anomalies that may be visible on the projected image. The illumination optical system should be designed to limit light flux incident anywhere outside the active array less than 10% of the average flux level in the active area. Depending on the particular system's optical architecture and assembly tolerances, the amount of overfill light on the outside of the active array may cause visible artifacts.

(16) At a wavelength of 632.8 nm.

(17) Refer to the **Package Mechanical Characteristics** section at the end of this document for details regarding the size and location of the window aperture.

(18) Refers only to non-cleanable artifacts. Refer to DMD S4xx Glass Cleaning Procedure (TI Literature number DLPA025) and DMD S4xx Handling Specifications (TI Literature number DLPA014) for recommend handling and cleaning processes.

 Copyright © 2010–2012, Texas Instruments Incorporated

Thermal Characteristics

Achieving optimal DMD performance requires proper management of the maximum DMD case temperature, the maximum temperature of any individual micromirror in the active array, the maximum temperature of the window aperture, and the temperature gradient between case temperature and the predicted micromirror array temperature. (see Figure 13).

Refer to the RECOMMEND OPERATING CONDITIONS for applicable temperature limits.

Package Thermal Resistance

The DMD is designed to conduct absorbed and dissipated heat to the back of the Series 450 package where it can be removed by an appropriate heat sink. The heat sink and cooling system must be capable of maintaining the package within the specified operational temperatures, refer to Figure 13. The total heat load on the DMD is typically driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array.

Package Thermal Resistance

	Min	Nom	Max	Units
Active Micromirror Array resistance to TC2			0.6	ºC/W

Case Temperature

The temperature of the DMD case can be measured directly. For consistency, a Thermal Test Point locations TC1 and TC2 are defined, as shown in Figure 13.

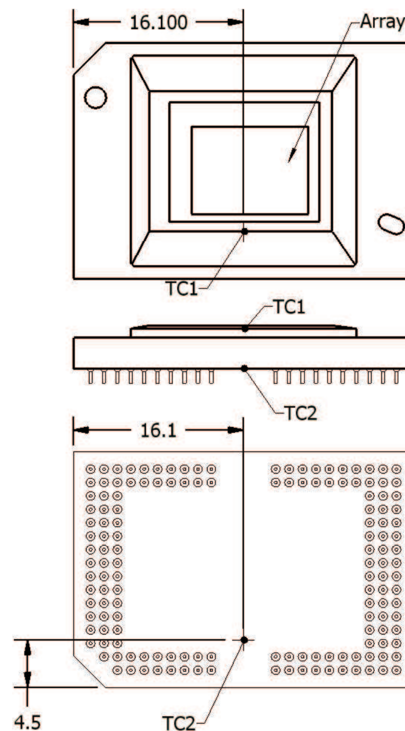


Figure 13. Thermal Test Point Location

Copyright © 2010–2012, Texas Instruments Incorporated

Micromirror Array Temperature Calculation for Uniform Illumination

Micromirror array temperature cannot be measured directly; therefore it must be computed analytically from measurement points (Figure 13), the package thermal resistance, the electrical power, and the illumination heat load. The relationship between micromirror array temperature and the case temperature are provided by the following equations:

$T_{Array} = T_{Ceramic} + (Q_{Array} \times R_{Array\text{-}To\text{-}Ceramic})$

$Q_{Array} = Q_{ELE} + Q_{ILL}$

Where the following elements are defined as:

T_{Array} = computed micromirror array temperature (°C)

$T_{Ceramic}$ = Ceramic temperature (°C) (TC2 Location Figure 13)

Q_{Array} = Total DMD array power (electrical + absorbed) (measured in Watts)

$R_{Array\text{-}To\text{-}Ceramic}$ = thermal resistance of DMD package from array to TC2 (°C/Watt) (see Package Thermal Resistance)

Q_{ELE} = Nominal electrical power (Watts)

Q_{ILL} = Absorbed illumination energy (Watts)

An example calculation is provided below based on a traditional DLP Video projection system. The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. The nominal electrical power dissipation to be used in the calculation is 2.0 Watts. Thus, Q_{ELE} = 2.0 Watts. The absorbed power from the illumination source is variable and depends on the operating state of the mirrors and the intensity of the light source. Based on modeling and measured data from DLP projection system $Q_{ILL} = C_{L2W} \times SL$.

Where:

C_{L2W} is a Lumens to Watts constant, and can be estimated at 0.00274 Watt/Lumen

SL = Screen Lumens nominally measured to be 2000 lumens

Qarray = 2.0 + (0.00274 x 2000) = 7.48 watts, Estimated total power on micromirror Array

$T_{Ceramic}$ = 55°C, assumed system measurement

Finally, T_{Array} (micromirror active array temperature) is

$\mathbf{T_{Array}}$= 55°C + (7.48 watts x 0.6 °C/watt) = **59.5°C**

For additional explanation of DMD Mechanical and Thermal calculations and considerations please refer to DLP Series-450 DMD and System Mounting Concepts (TI Literature number DLPA015).

Copyright © 2010–2012, Texas Instruments Incorporated

REVISION HISTORY

Changes from Original (April 2010) to Revision A **Page**

- Added Additional Related Documents 7
- Changed V_{REF} to V_{CC1} 11
- Added $|V_{ID}|$ to the absolute max table 11
- Added V_{MBRST} to the absolute max table 11
- Changed the Illumination power density Max value of < 420 mm From: 2 To: 20 mW/cm^2 11
- Clarified Note6 measurement point 11

Changes from Revision A (June 2010) to Revision B **Page**

- Changed the window refractive index NOM spec From: 1.5090 To: 1.5119 18
- Added table note "At a wavelength of 632.8 nm" 18

Changes from Revision B (September 2011) to Revision C **Page**

- Added the Package Footprint and Socket information in the Features list 1
- Deleted redundant information from the Description 4
- Corrected the document reference in Related Documents section 7
- Changed Storage temperature range and humidity values in ABSOLUTE MAXIMUM RATINGS 11
- Changed the Illumination power density Max value of < 420 mm From: 20 To: 2 mW/cm^2 11
- Added Operating Case Temperature, Operating Humidity, Operating Device Temperature Gradient and Operating Landed Duty-Cycle to RECOMMENDED OPERATING CONDITIONS. 12
- Added Mirror metal specular reflectivity and Illumination overfill values to "Micromirror Array Optical Characteristics" table 18
- Corrected the C_{L2W}, Qarray and T_{array} values in Micromirror Array Temperature Calculation for Uniform Illumination. 20

Changes from Revision C (June 2012) to Revision D **Page**

- Changed the Device Part Number Nomenclature From: DLP5500FYA To: DLP5500AFYA 7

Copyright © 2010–2012, Texas Instruments Incorporated

DWG NO 2512194 SH 1

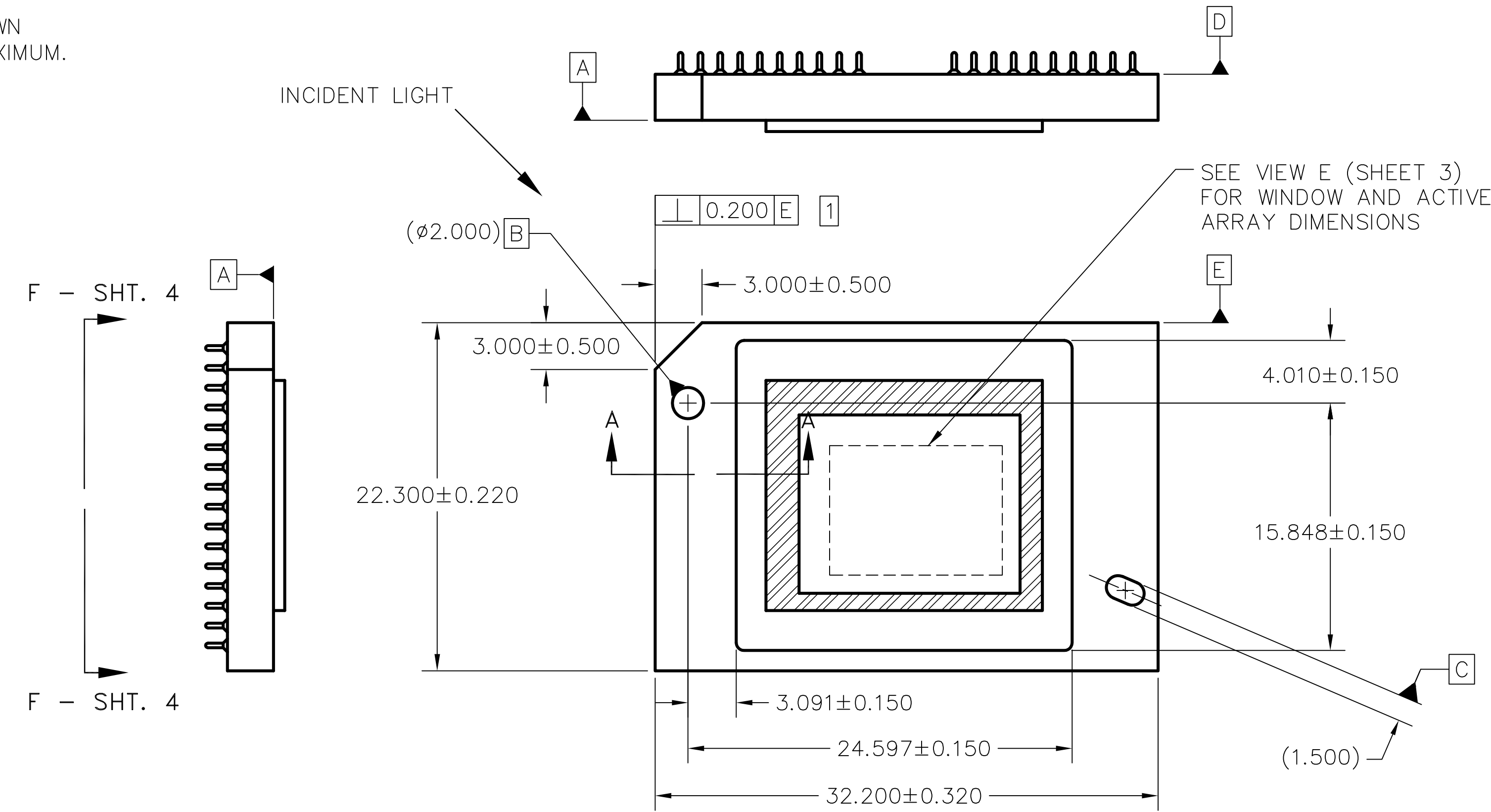
© COPYRIGHT 2012 TEXAS INSTRUMENTS UN-PUBLISHED, ALL RIGHTS RESERVED.

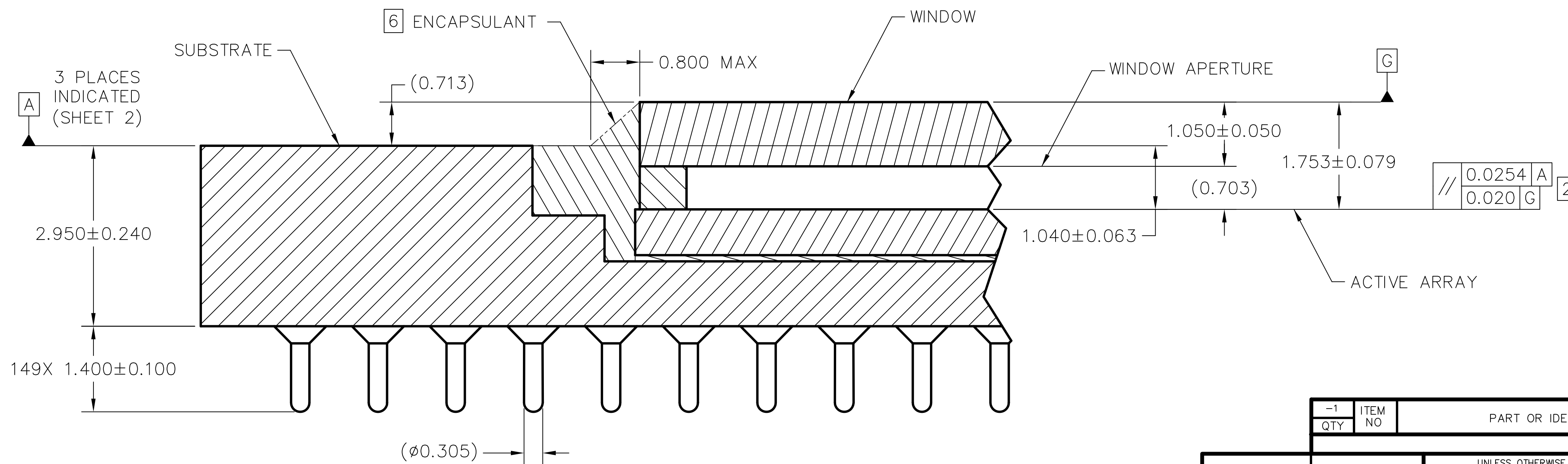
REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	ECO 2121693, INITIAL RELEASE	01/17/2012	F. ARMSTRONG
B	ECO 2123271, CHG TO LARGE SYMBOLIZATION PAD	03/16/2012	F. ARMSTRONG

NOTES: UNLESS OTHERWISE SPECIFIED:

1. SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE
2. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY
3. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.8 DEGREES
4. SUBSTRATE SYMBOLIZATION PAD, AND PLATING AT BOTTOM OF DATUMS B AND C HOLES TO BE ELECTRICALLY CONNECTED TO VSS PLANE WITHIN THE SUBSTRATE
5. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE AREA
6. MAXIMUM ENCAPSULANT PROFILE SHOWN
7. ENCAPSULANT ALLOWED ON THE SURFACE OF THE CERAMIC IN THE AREA SHOWN IN VIEW B (SHEET 2). ENCAPSULANT SHALL NOT EXCEED 0.200 THICKNESS MAXIMUM.





SECTION A–A
SCALE 20/1

–1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

PARTS LIST

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES: ANGLES ± 1°
  2 PLACE DECIMALS ±0.25
  3 PLACE DECIMALS ±0.50
- REMOVE ALL BURRS AND SHARP EDGES
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5–1994
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

NEXT ASSY	USED ON
NONE	0314DA

APPLICATION

THIRD ANGLE PROJECTION

	NAME	DATE
DWN	F. ARMSTRONG	01/17/12
ENGR	F. ARMSTRONG	01/17/12
QA	P. KONRAD	01/19/12
CQE	M. DORAK	01/19/12

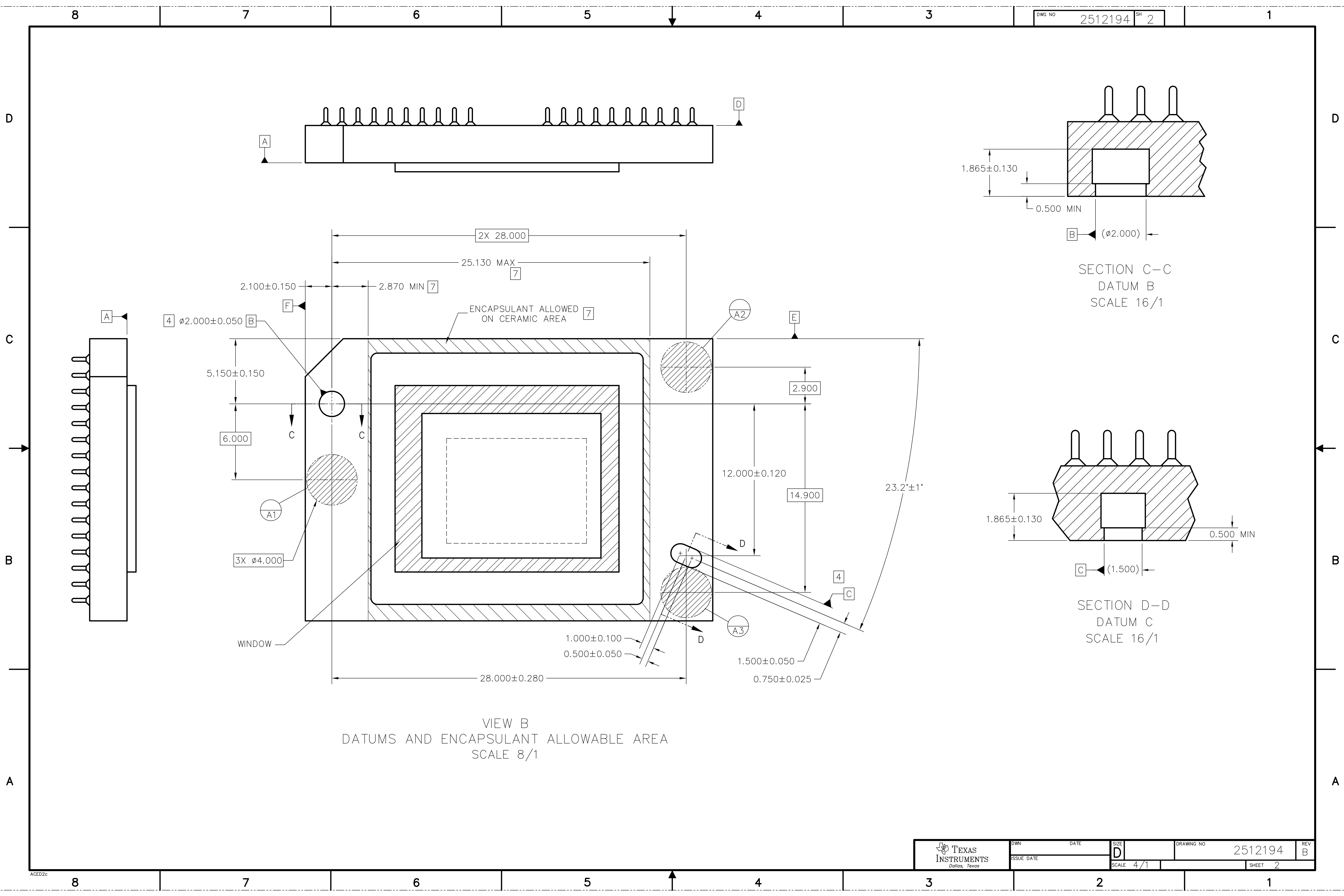
TEXAS INSTRUMENTS
Dallas, Texas

ICD, MECHANICAL, DMD
.55" XGA 2xLVDS V2 SERIES 450

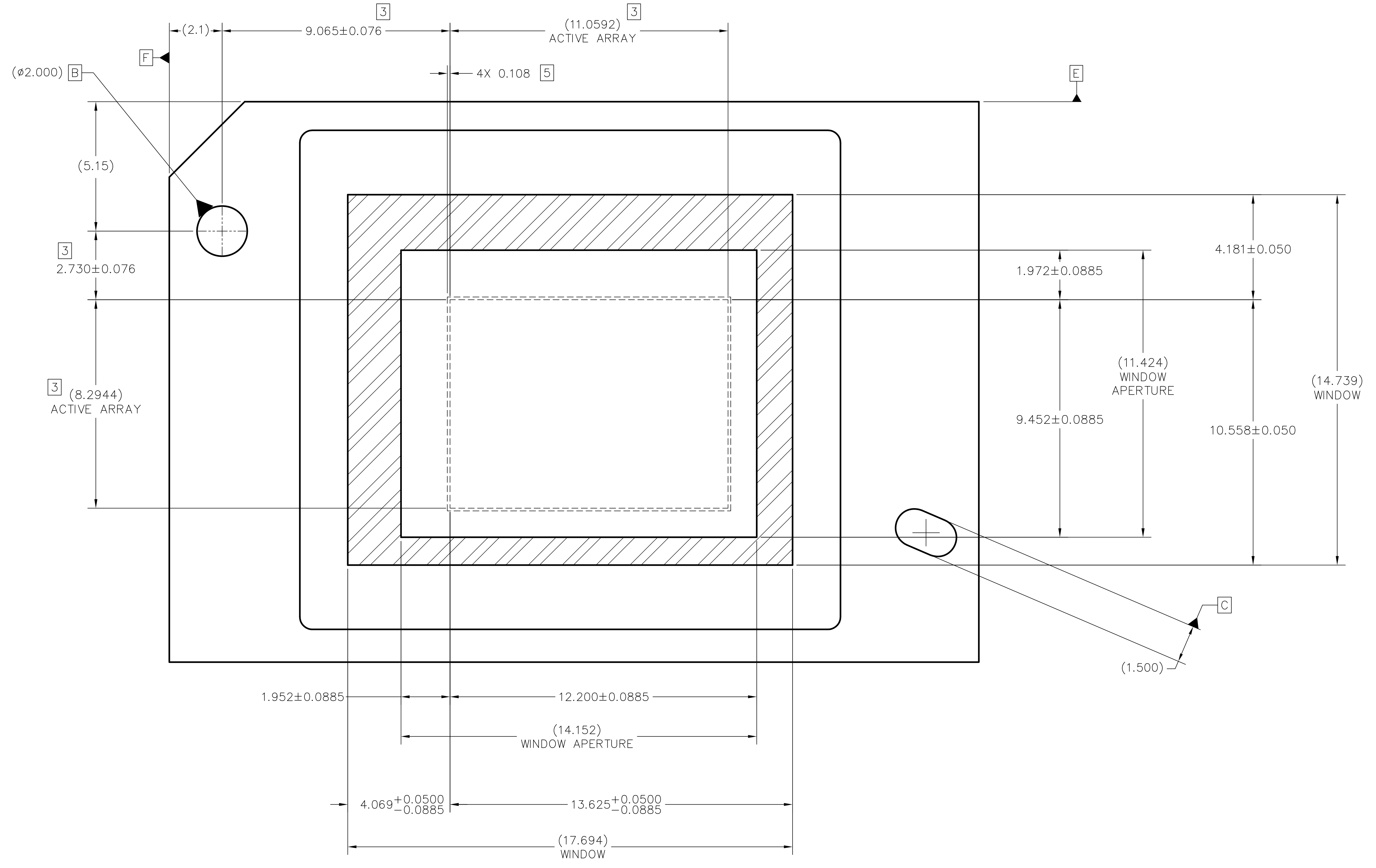
SIZE D | DRAWING NO 2512194 | REV B

SCALE 4/1 | SHEET 1 OF 4

ACED1g



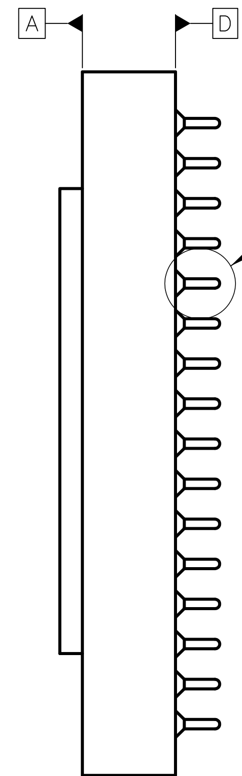
DWG NO 2512194 SH 2
2X 28.000
25.130 MAX 7
2.100±0.150
2.870 MIN 7
ENCAPSULANT ALLOWED ON CERAMIC AREA 7
4 ø2.000±0.050 B
5.150±0.150
6.000
2.900
12.000±0.120
14.900
23.2°±1°
3X ø4.000
WINDOW
1.000±0.100
0.500±0.050
28.000±0.280
1.500±0.050
0.750±0.025
VIEW B
DATUMS AND ENCAPSULANT ALLOWABLE AREA
SCALE 8/1
1.865±0.130
0.500 MIN
(ø2.000)
SECTION C–C
DATUM B
SCALE 16/1
(1.500)
SECTION D–D
DATUM C
SCALE 16/1
TEXAS INSTRUMENTS
Dallas, Texas
SIZE D
SCALE 4/1
DRAWING NO 2512194
REV B
SHEET 2



VIEW E (SHEET 1)
DMD WINDOW AND ACTIVE ARRAY
SCALE 12:1

TEXAS INSTRUMENTS
Dallas, Texas

DWG NO 2512194 SH 3
SIZE D SCALE 4/1
DRAWING NO 2512194 REV B
SHEET 3



VIEW F–F (SHEET 1)
PINS AND SYMBOLIZATION PAD
SCALE 8/1

(A1, A2, & B1 OMITTED)

452

149X ø0.305 +0.050/−0.025 PINS

⌖	Ø0.500	D	E	F
	Ø0.250	D		

SYMBOLIZATION PAD 4

19.145

9X 1.270 = 11.430

9X 1.270 = 11.430

1.625

1.625

3.895±0.250

14.510±0.250

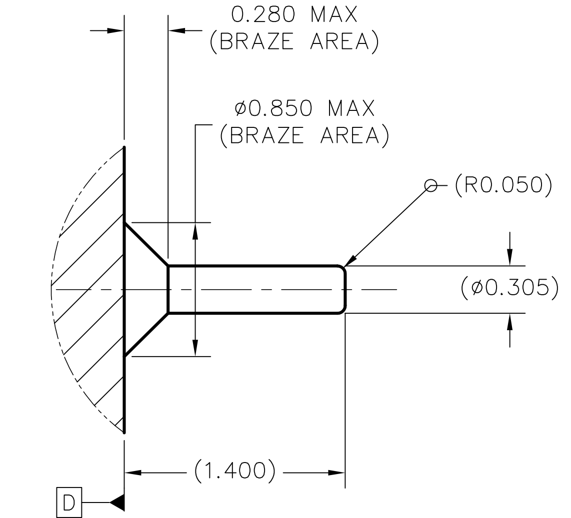
15X 1.27 = 19.050

10.000±0.250

11.100±0.250

A B C D E F G H J K L M N P R T

20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1



DETAIL G (149 PLACES)
PIN & BRAZE DIMENSIONS
SCALE 40/1

TEXAS INSTRUMENTS Dallas, Texas	DWN	DATE	SIZE D	DRAWING NO 2512194	REV B
	ISSUE DATE		SCALE 4/1	SHEET 4	

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DLP5500AFYA	ACTIVE	CPGA	FYA	149	5	TBD	Call TI	Call TI			Samples
DLP5500FYA	ACTIVE	CPGA	FYA	149		TBD	Call TI	Call TI			Samples
DLPA200PFC	ACTIVE	TQFP	PFC	80	5	Pb-Free (RoHS)	Call TI	Level-2-260C-1 YEAR			Samples
DLPC200ZEW	ACTIVE	BGA	ZEW	780	5	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR			Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2013, Texas Instruments Incorporated