12-Bit, 800kHz Sampling CMOS ANALOG-TO-DIGITAL CONVERTER

Check for Samples: ADS7810

FEATURES

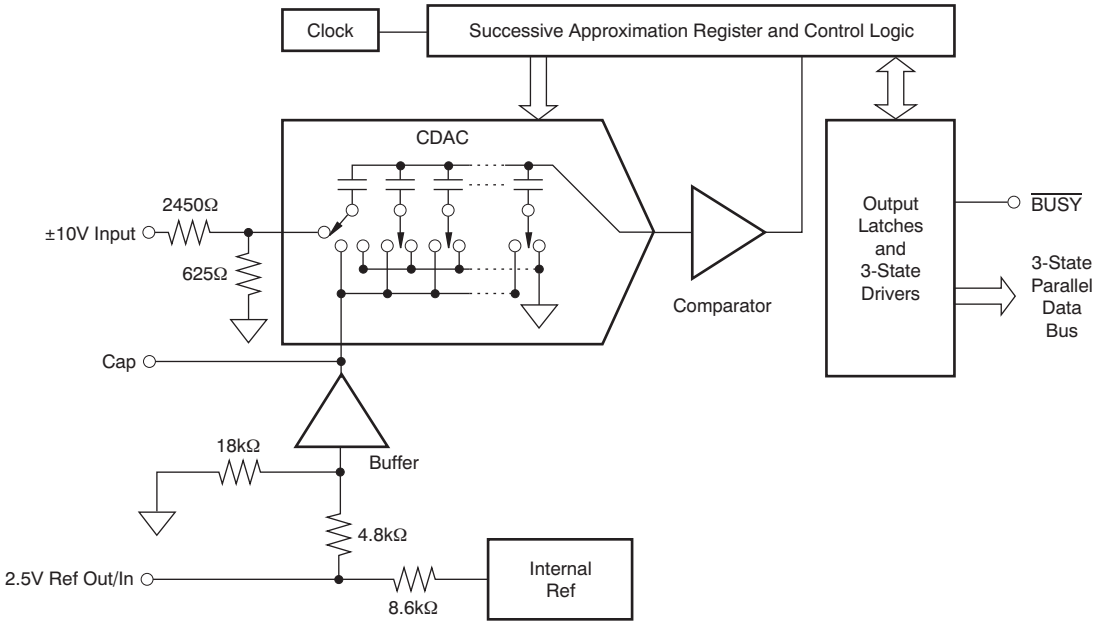
- **1.25μs Throughput Time**
- **Standard ±10V Input Range**
- **69dB Min SINAD With 250kHz Input**
- **±3 LSB Max INL and ±3 LSB Max DNL**
- **Internal Reference**
- **Complete With S/H, REF, CLOCK, ETC.**
- **Parallel Data w/Latches**
- **28-PIN SOIC Package**

DESCRIPTION

The ADS7810 is a complete 12-bit sampling analog-to-digital converter (A/D) using state-of-the-art CMOS structures. It contains a complete 12-bit capacitor-based SAR A/D with inherent S/H, reference, clock, interface for microprocessor use, and 3-state output drivers.

The ADS7810 is specified at an 800kHz sampling rate, and ensured over the full temperature range. Laser-trimmed scaling resistors provide the industry-standard ±10V input range, while an innovative design allows operation from ±5V supplies.

The 28-pin ADS7810 is available in a plastic SOIC fully specified for operation over the industrial –40°C to +70°C range.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or see the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

	ADS7810	UNIT
Analog inputs: V_{IN}	±25	V
	$+V_{ANA}$ +0.3 to AGND2 –0.3	V
	Indefinite Short to AGND2 Momentary Short to $+V_{ANA}$	V
Ground voltage differences: DGND, AGND1, AGND2	±0.3	V
$+V_{ANA}$	+7	V
$+V_{DIG}$ to $+V_{ANA}$	+0.3	V
$+V_{DIG}$	+7	V
$–V_{ANA}$	–7	V
Digital inputs	–0.3 to $+V_{DIG}$ +0.3	V
Maximum junction temperature	+165	°C
Internal power dissipation	825	mW

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

At T_A = –40°C to +70°C, f_S = 800kHz, $+V_{DIG}$ = $+V_{ANA}$ = +5V, $–V_{ANA}$ = –5V, using internal reference and the 50Ω input resistor shown in Figure 16, unless otherwise specified.

PARAMETER		TEST CONDITIONS	ADS7810U			ADS7819UB[1]			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION					12			12	Bits
ANALOG INPUT									
Voltage range		+In – (–In)		±10			±10		V
Impedance				3.1			3.1		kΩ
Capacitance				5			5		pF
THROUGHPUT SPEED									
Conversion cycle		$t_3 + t_4$		1020			1020		ns
Complete cycle		Acquire and convert			1250			1250	ns
Throughput rate			800			800			kHz
DC ACCURACY									
Integral linearity error					±3			±2	LSB
Differential linearity error					±3			±3	LSB
No missing codes				Ensured			Ensured		
Transition noise[2]				0.1			0.1		LSB
Full-scale error[3][4]					±1			±0.75	%
Full-scale error drift				±12			±12		ppm/°C
Full-scale error[3][4]		Ext. 2.5000V Ref			±1			± 1	%
Full-scale error drift		Ext. 2.5000V Ref		±12			±12		ppm/°C
Bipolar zero error[3]					±8			±4	LSB
Bipolar zero error drift				±2			±2		ppm/°C
Power-supply sensitivity ($+V_{DIG}$ = $+V_{ANA}$ = V_D)		+4.75V < V_D < +5.25V			±5			±5	LSB
		–5.25V < $–V_{ANA}$ < –4.75V			±0.5			±0.5	LSB
AC ACCURACY									
Spurious-free dynamic range		f_{IN} = 250kHz	74	82		77	84		dB[5]
Total harmonic distortion		f_{IN} = 250kHz		–80	–74		–82	–77	dB
Signal-to-(noise+distortion)		f_{IN} = 250kHz	67	71		69	71		dB
Signal-to-noise		f_{IN} = 250kHz	66	71		70	71		dB
Usable bandwidth[6]				1.5			1.5		MHz
SAMPLING DYNAMICS									
Aperture delay				20			20		ns
Aperture jitter				10			10		ps
Transient response		Full-scale step		200			200		ns
Overvoltage recovery[7]				250			250		ns
REFERENCE									
Internal reference voltage			2.48	2.5	2.52	2.48	2.5	2.52	V
Internal reference dc source current (external load should be static)				100			100		µA
Internal reference drift				8			8		ppm/°C
External reference voltage range for specified linearity			2.3	2.5	2.7	2.3	2.5	2.7	V
External reference current drain		Ext. 2.5000V Ref			100			100	µA
DIGITAL INPUTS									
Logic levels	V_{IL}		–0.3		+0.8	–0.3		+0.8	V
	V_{IH}		+2.4		V_D + 0.3	+2.4		V_D + 0.3	V
	I_{IL}	V_{IL} = 0V			±10			±10	µA
	I_{IH}	V_{IH} = 5V			±10			±10	v

(1) Shaded cells indicate same specifications as the ADS7810U.
(2) Typical rms noise at worst-case transitions and temperatures.
(3) Measured with 50Ω in series with analog input. Adjustable to zero with external potentiometer.
(4) Full-scale error is the worst case of –Ful-Scale or +Full-Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error.
(5) All specifications in dB are referred to a full-scale ±10V input.
(6) Usable bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB, or 10 bits of accuracy.
(7) Recovers to specified performance after 2 x FS input over voltage.

ELECTRICAL CHARACTERISTICS (continued)

At T_A = –40°C to +70°C, f_S = 800kHz, $+V_{DIG}$ = $+V_{ANA}$ = +5V, $–V_{ANA}$ = –5V, using internal reference and the 50Ω input resistor shown in Figure 16, unless otherwise specified.

PARAMETER		TEST CONDITIONS	ADS7810U			ADS7819UB[1]			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL OUTPUTS									
Data format				Parallel 12 bits			Parallel 12 bits		
Data coding				Binary twos complement			Binary twos complement		
	V_{OL}	I_{SINK} = 1.6mA			+0.4			+0.4	V
	V_{OH}	I_{SOURCE} = 500µA	+2.8			+2.8			V
Leakage current		High-Z state, V_{OUT} = 0V to V_{DIG}			±5			±5	µA
Output capacitance		High-Z state			15			15	pF
DIGITAL TIMING									
Bus access time					62			62	ns
Bus relinquish time					83			83	ns
POWER SUPPLIES									
Specified performance	$+V_{DIG}$ = $+V_{ANA}$		+4.75	+5	+5.25	+4.75	+5	+5.25	V
	$–V_{ANA}$		–5.25	–5	–4.75	–5.25	–5	–4.75	V
	$+I_{DIG}$			+16			+16		mA
	$+I_{ANA}$			+16			+16		mA
	$–I_{ANA}$			–13			–13		mA
Derated performance	$+V_{DIG}$ = $+V_{ANA}$		+4.5	+5	+5.5	+4.5	+5	+5.5	V
	$–V_{ANA}$		–5.5	–5	–4.5	–5.5	–5	–4.5	V
Power dissipation		f_S = 800kHz		225	275		225	275	mW
TEMPERATURE RANGE									
Specified performance			–40		+70	–40		+70	°C
Derated performance			–55		+125	–55		+125	°C
Storage			–65		+150	–65		+150	°C
Thermal resistance (θ_{JA})	Plastic DIP			75			75		°C/W
	SOIC			75			75		°C/W

TIMING INFORMATION

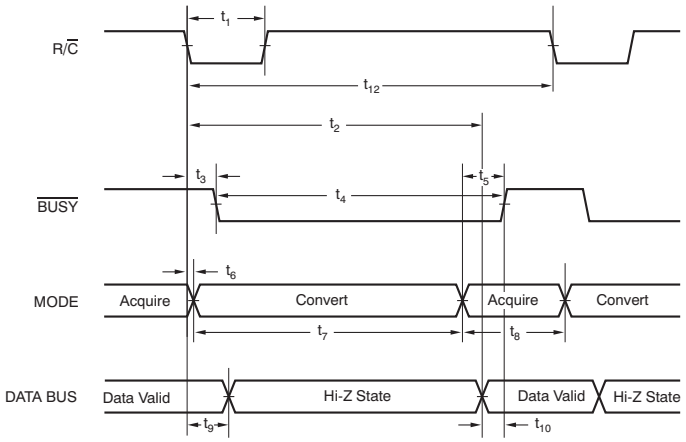


Figure 1. Conversion Timing with Outputs Enabled After Conversion ($\overline{CS}$ Tied Low)

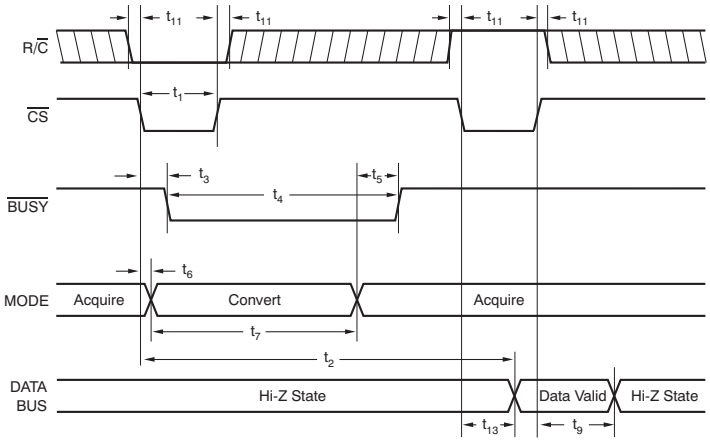


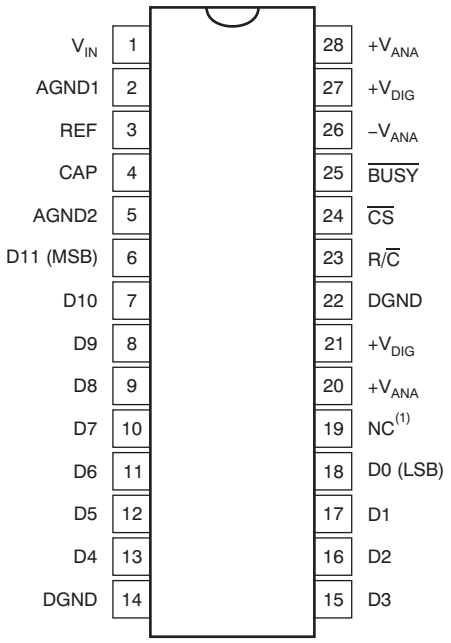
Figure 2. Using $\overline{CS}$ to Control Conversion and Read Timing

TIMING REQUIREMENTS (T_{MIN} to T_{MAX})

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_1	Convert pulse width	40			ns
t_2	Data valid delay after R/$\overline{C}$ low		955	1095	ns
t_3	$\overline{BUSY}$ delay from R/$\overline{C}$ low		70	125	ns
t_4	$\overline{BUSY}$ low		950	1080	ns
t_5	$\overline{BUSY}$ delay after end of conversion		90		ns
t_6	Aperture delay		20		ns
t_7	Conversion time		910	1020	ns
t_8	Acquisition time		200	230	ns
t_7, t_8	Throughput time		1110	1250	ns
t_9	Bus relinquish time	10	50	83	ns
t_{10}	$\overline{BUSY}$ delay after data valid	20	65	120	ns
t_{11}	R/$\overline{C}$ to $\overline{CS}$ setup time	10			ns
t_{12}	Time between conversions	1250			ns
t_{13}	Bus access time	10	25	62	ns

PIN CONFIGURATION

DW PACKAGE
SOIC-28
(TOP VIEW)



(1) Not internally connected.

PIN ASSIGNMENTS

PIN		DIGITAL I/O	DESCRIPTION
NO.	NAME		
1	V_{IN}		Analog input. Connect via 50Ω to analog input. Full-scale input range is ±10V.
2	AGND1		Analog ground. Used internally as ground reference point. Minimal current flow.
3	REF		Reference input/output. Outputs internal reference of +2.5V nominal. Can also be driven by external system reference. In both cases, decouple to ground with a 0.1μF ceramic capacitor.
4	CAP		Reference buffer output. 10μF tantalum capacitor to ground. Nominally +2V.
5	AGND2		Analog ground.
6	D11 (MSB)	O	Data bit 11. Most significant bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low, or when a conversion is in progress.
7	D10	O	Data bit 10. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low, or when a conversion is in progress.
8	D9	O	Data bit 9. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low, or when a conversion is in progress.
9	D8	O	Data bit 8. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low, or when a conversion is in progress.
10	D7	O	Data bit 7. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low, or when a conversion is in progress.
11	D6	O	Data bit 6. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low, or when a conversion is in progress.
12	D5	O	Data bit 5. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low, or when a conversion is in progress.
13	D4	O	Data bit 4. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low, or when a conversion is in progress.
14	DGND		Digital ground.
15	D3	O	Data bit 3. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low, or when a conversion is in progress.

PIN ASSIGNMENTS (continued)

PIN		DIGITAL I/O	DESCRIPTION
NO.	NAME		
16	D2	O	Data bit 2. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low, or when a conversion is in progress.
17	D1	O	Data bit 1. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low, or when a conversion is in progress.
18	D0 (LSB)	O	Data bit 0. Least significant bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is high, or when R/$\overline{C}$ is low, or when a conversion is in progress.
19	NC		Not internally connected.
20	$+V_{ANA}$		Analog positive supply input. Nominally +5V. Connect directly to pins 21, 27, and 28.
21	$+V_{DIG}$		Digital supply input. Nominally +5V. Connect directly to pins 20, 27, and 28.
22	DGND		Digital ground.
23	R/$\overline{C}$	I	Read/Convert input. With $\overline{CS}$ low, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. With $\overline{CS}$ low and no conversion in progress, a rising edge on R/$\overline{C}$ enables the output data bits.
24	$\overline{CS}$	I	Chip select. With R/$\overline{C}$ low, a falling edge on $\overline{CS}$ will initiate a conversion. With R/$\overline{C}$ high and no conversion in progress, a falling edge on $\overline{CS}$ will enable the output data bits.
25	$\overline{BUSY}$	O	Busy output. Falls when a conversion is started, and remains low until the conversion is completed and the data are latched into the output register. With $\overline{CS}$ low and R/$\overline{C}$ high, output data will be valid when $\overline{BUSY}$ rises, so that the rising edge can be used to latch the data.
26	$-V_{ANA}$		Analog negative supply input. Nominally –5V. Decouple to ground with 0.1μF ceramic and 10vF tantalum capacitors.
27	$+V_{DIG}$		Digital supply input. Nominally +5V. Connect directly to pins 20, 21, and 28.
28	$+V_{ANA}$		Analog positive supply input. Nominally +5V. Connect directly to pins 20, 21, and 27, and decouple to ground with 0.1μF ceramic and 10μF tantalum capacitors.

TYPICAL CHARACTERISTICS

At T_A = +25°C, f_S =800kHz, $+V_{DIG}$ = $+V_{ANA}$ = +5V, $-V_{ANA}$ = –5V, using internal reference and the 50Ω input resistors as shown in Figure 16, unless otherwise specified.

FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 252kHz, –0.5dB)

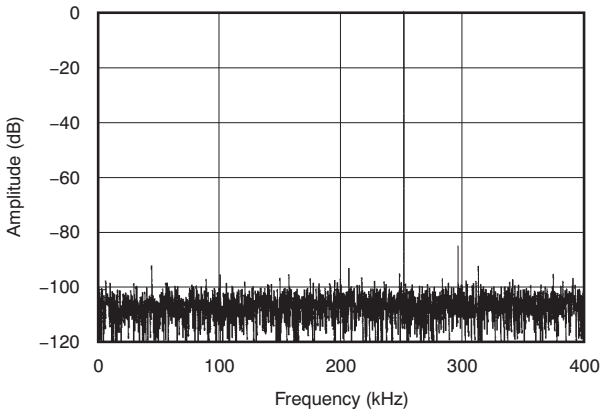


Figure 3.

FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 502kHz, –0.5dB)

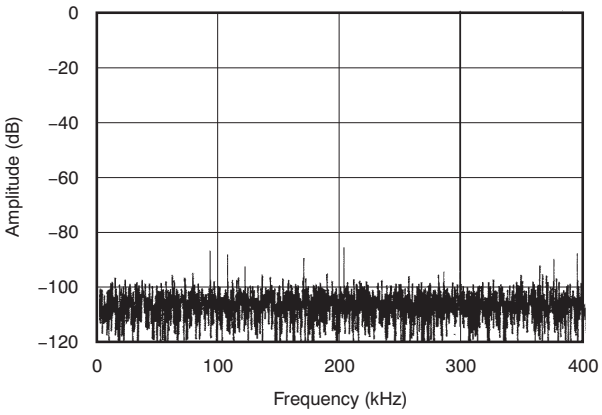


Figure 4.

FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 1002kHz, –0.5dB)

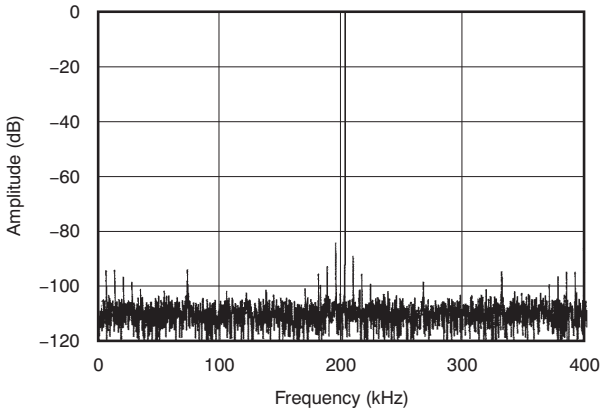


Figure 5.

FREQUENCY SPECTRUM
(4096 Point $f1_{IN}$ = 232kHz, –6.5dB; $f2_{IN}$ = 272kHz, –6.5dB)

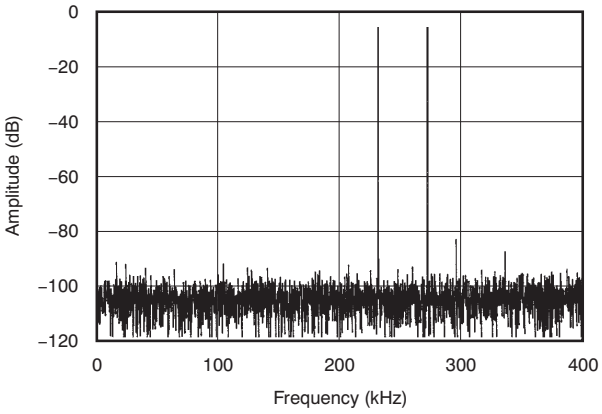


Figure 6.

SIGNAL-TO-(NOISE + DISTORTION)
vs INPUT FREQUENCY (f_{IN} = –0.5dB)

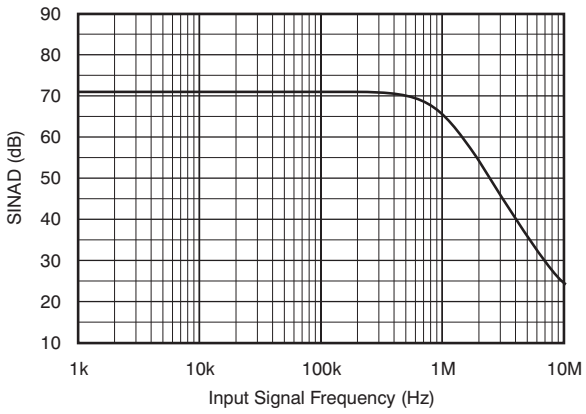


Figure 7.

AC PARAMETERS vs TEMPERATURE
(f_{IN} = 250kHz, –0.5dB)

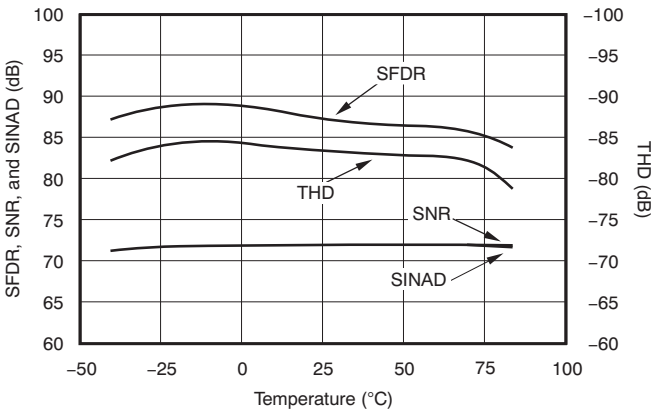


Figure 8.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, f_S =800kHz, $+V_{DIG}$ = $+V_{ANA}$ = +5V, $-V_{ANA}$ = –5V, using internal reference and the 50Ω input resistors as shown in Figure 16, unless otherwise specified.

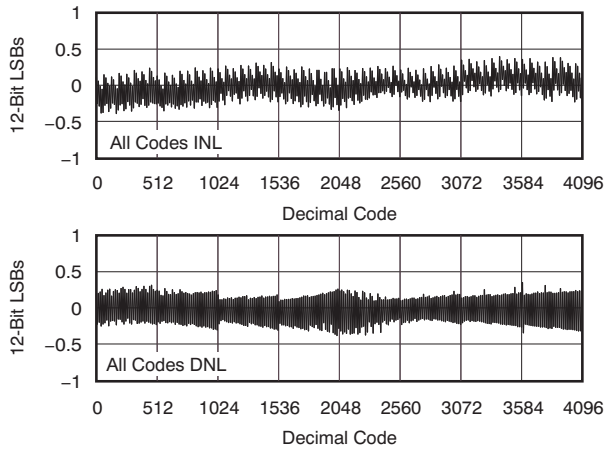


Figure 9.

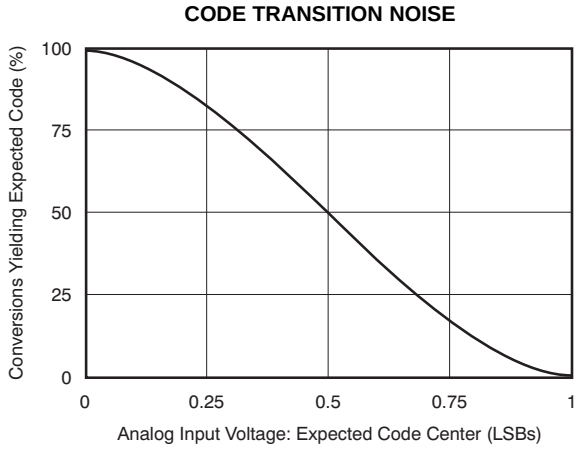


Figure 10.

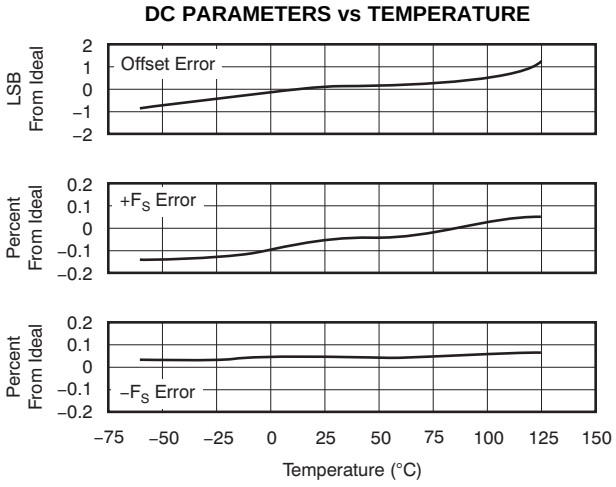


Figure 11.

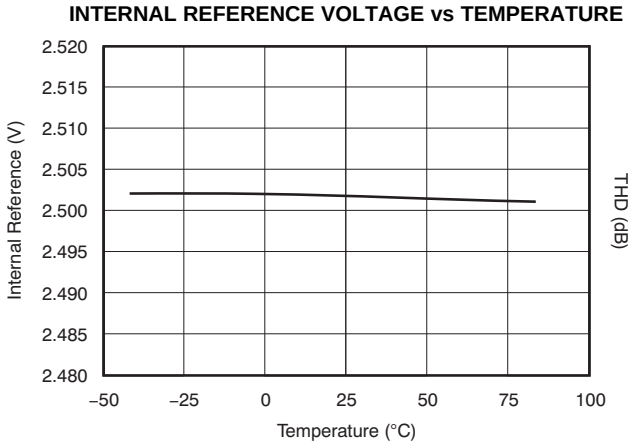


Figure 12.

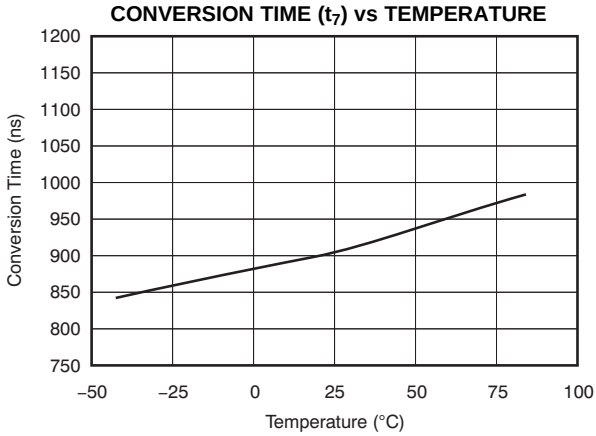


Figure 13.

APPLICATION INFORMATION

BASIC OPERATION

Figure 14 shows a basic circuit to operate the ADS7810. Taking R/$\overline{C}$ (pin 23) low for a minimum of 40ns will initiate a conversion. $\overline{BUSY}$ (pin 25) will go low and stay low until the conversion is completed and the output registers are updated. Data will be output in binary twos complement with the MSB on D11 (pin 6). $\overline{BUSY}$ going high can be used to latch the data. All convert commands will be ignored while $\overline{BUSY}$ is low.

The ADS7810 will begin tracking the input signal at the end of the conversion. Allowing 1.25μs between convert commands assures accurate acquisition of a new signal.

STARTING A CONVERSION

The combination of $\overline{CS}$ (pin 24) and R/$\overline{C}$ (pin 23) low for a minimum of 40ns puts the sample/hold of the ADS7810 in the hold state and starts a conversion. $\overline{BUSY}$ (pin 25) will go low and stay low until the conversion is completed and the internal output register has been updated. All new convert commands during $\overline{BUSY}$ low will be ignored.

The ADS7810 will begin tracking the input signal at the end of the conversion. Allowing 1.25μs between convert commands assures accurate acquisition of a new signal. Refer to Table 1 for a summary of $\overline{CS}$, R/C, and $\overline{BUSY}$ states, and Figure 1 and Figure 2 for timing parameters.

$\overline{CS}$ and R/$\overline{C}$ are internally OR'd and level triggered. There is not a requirement which input goes low first when initiating a conversion. If it is critical that $\overline{CS}$ or R/$\overline{C}$ initiate the conversion, be sure the less critical input is low at least 10ns prior to the initiating input.

To reduce the number of control pins, $\overline{CS}$ can be tied low using R/$\overline{C}$ to control the read and convert modes. Note that the parallel output will be active whenever R/$\overline{C}$ is HIGH and no conversion is in progress. See the *Reading Data* section and refer to Table 1 for control line functions for 'read' and 'convert' modes.

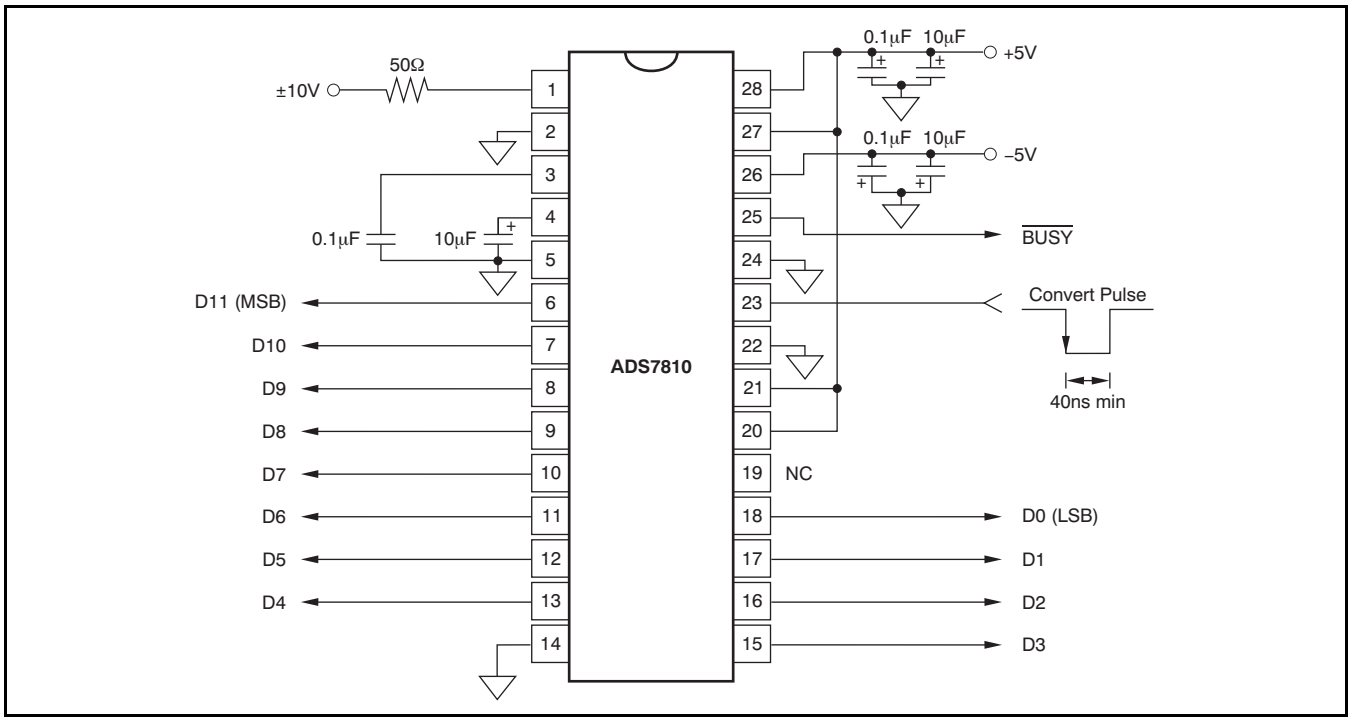


Figure 14. Basic Operation

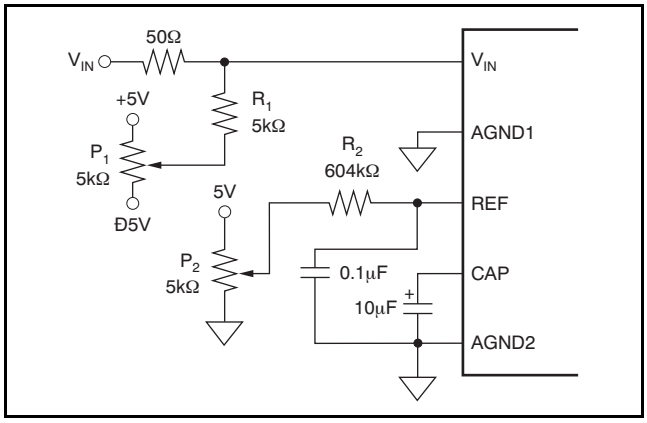
READING DATA

The ADS7810 outputs full parallel data in binary twos complement data format. The parallel output will be active when R/$\overline{C}$ (pin 23) is high, $\overline{CS}$ (pin 24) is low, and no conversion is in progress. Any other combination will 3-state the parallel output. Valid conversion data can be read in a full parallel, 12-bit word on D11-D0 (pins 6-13 and 15- 18). Refer to Table 2 for ideal output codes.

After the conversion is completed and the output registers have been updated, $\overline{BUSY}$ (pin 25) will go high. Valid data from the most recent conversion will be available on D11-D0 (pins 6-13 and 15-18). $\overline{BUSY}$ going high can be used to latch the data. Refer to Timing Requirements as well as Figure 1 and Figure 2.

NOTE: For the best performance, the external data bus connected to D11-D0 should not be active during a conversion. The switching noise of the external asynchronous data signals can cause digital feedthrough degrading the converter performance.

The number of control lines can be reduced by tying $\overline{CS}$ low while using R/$\overline{C}$ to initiate conversions and activate the output mode of the converter. See Figure 1.



Note: Use 1% metal film resistors. Trim offset at 0V first, then trim gain at 10V.

Figure 15. Circuit Diagram with External Hardware Trim

INPUT RANGES

The ADS7810 offers a standard ±10V input range. Figure 15 and Figure 16 show the necessary circuit connections for the ADS7810 with and without external trim. Offset and full-scale error(1) specifications are tested and ensured with the 50Ω resistor shown in Figure 16. This external resistor makes it possible to trim the offset ±50mV using a trim pot or trim DAC. This resistor may be left out if the offset and gain errors will be corrected in software or if they are negligible in regards to the particular application. See the *Calibration* section of the data sheet for details.

The nominal input impedance of 3.125kW results from the combination of the internal resistor network shown on the front page of the product data sheet and external 50Ω resistor. The input resistor divider network provides inherent overvoltage protection ensured to at least ±25V. The 50Ω, 1% resistor does not compromise the accuracy or drift of the converter. It has little influence relative to the internal resistors, and tighter tolerances are not required.

NOTE: The values shown for the internal resistors are for reference only. The exact values can vary by ±30%. This is true of all resistors internal to the ADS7810. Each resistive divider is trimmed so that the proper division is achieved.

(1) Full-scale error includes offset and gain errors measured at both +FS and –FS.

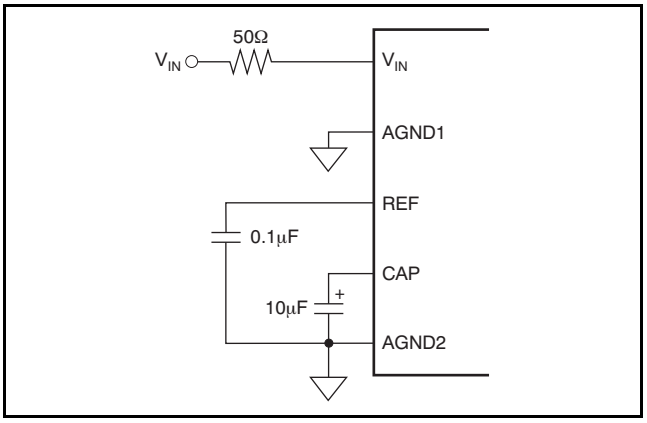


Figure 16. Circuit Diagram without External Hardware Trim

Table 1. Control Line Functions for 'Read' and 'Convert'

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	OPERATION
1	X	X	None. Databus in Hi-Z state.
↓	0	1	Initiates conversion. Databus remains in Hi-Z state.
0	↓	1	Initiates conversion. Databus enters Hi-Z state.
0	1	↑	Conversion completed. Valid data from the most recent conversion on the databus.
↓	1	1	Enables databus with valid data from the most recent conversion.
↓	1	0	Conversion in progress. Databus in Hi-Z state, enabled when the conversion is completed.
0	↑	0	Conversion in progress. Databus in Hi-Z state, enabled when the conversion is completed.
0	0	↑	Conversion completed. Valid data from the most recent conversion in the output register, but output pins D11-D0 are 3-stated.
X	X	0	New convert commands ignored. Conversion in progress.

Table 2. Ideal Input Voltages and Output Codes

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT	
Full-Scale Range	±10V	BINARY TWOS COMPLEMENT	
Least Significant Bit (LSB)	4.88mV	BINARY CODE	HEX CODE
+Full-Scale (10V – 1LSB)	9.995V	0111 1111 1111	7FF
Midscale	0V	0000 0000 0000	000
One LSB below Midscale	–4.88mV	1111 1111 1111	FFF
–Full-Scale	–10V	1000 0000 0000	800

CALIBRATION

The ADS7810 can be trimmed in hardware or software. The offset should be trimmed before the gain since the offset directly affects the gain.

Hardware Calibration

To calibrate the offset and gain of the ADS7810, install the proper resistors and potentiometers as shown in Figure 15. The calibration range is ±50mV for bipolar zero and ±120mV for full scale.

Potentiometer P_1 and resistor R_1 form the offset adjust circuit and P_2 and R_2 the gain adjust circuit. The exact values are not critical. R_1 and R_2 should not be made any larger than the value shown. They can easily be made smaller to provide increased adjustment range. Reducing these below 15% of the indicated values could begin to adversely affect the operation of the converter.

P_1 and P_2 can also be made larger to reduce power dissipation. However, larger resistances will push the useful adjustment range to the edges of the potentiometer. P_1 should probably not exceed 20kΩ and P_2 100kΩ in order to maintain reasonable sensitivity.

Software Calibration

To calibrate the offset and gain of the ADS7810, no external resistors are required. See the *No Calibration* section for details on the effects of the external resistor.

No Calibration

See Figure 16 for circuit connections. Note that the actual voltage dropped across the 50Ω resistor is nearly two orders of magnitude lower than the voltage dropped across the internal resistor divider network. This should be taken into consideration when choosing the accuracy and drift specifications of the external resistors. In most applications, 1% metal-film resistors will be sufficient.

The external 50Ω resistor shown in Figure 16 may not be necessary in some applications. This resistor provides trim capability for the offset and compensates for a slight gain adjustment internal to the ADS7810. Not using the 50Ω resistor will cause a small gain error but will have no effect on the inherent offset error. Figure 17 shows typical transfer function characteristics with and without the 50Ω resistor in the circuit.

REFERENCE

The ADS7810 can operate with its internal 2.5V reference or an external reference. By applying an external reference to pin 3, the internal reference can be bypassed. The reference voltage at REF is buffered internally and output on CAP (pin 4).

REF

REF (pin 3) is an input for an external reference or the output for the internal 2.5V reference. A 0.1μF capacitor should be connected as close to the REF pin as possible. The capacitor and the output resistance of REF create a low pass filter to band limit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference degrading the SNR and SINAD. The internal reference should not be used to sink or source currents greater than 100mA. In addition, all external loads should be static.

The range for the external reference is 2.3V to 2.7V and determines the actual LSB size. Increasing the reference voltage will increase the full-scale range and the LSB size of the converter which can improve the SNR.

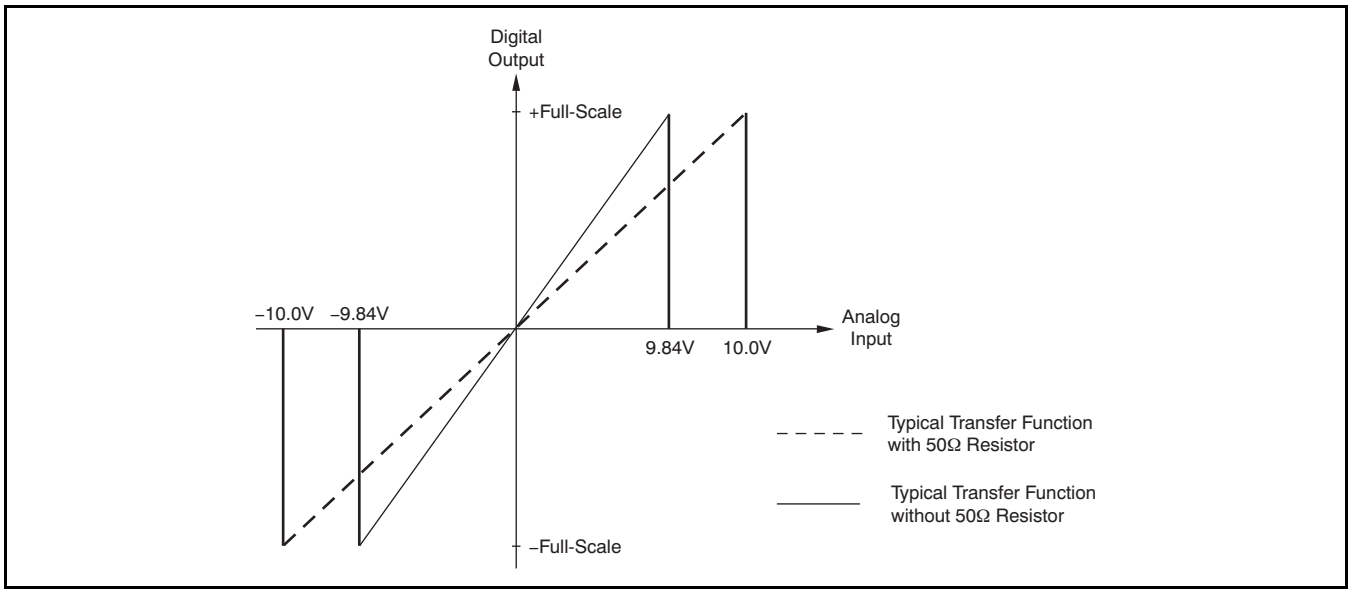


Figure 17. Comparison of the ADS7810 Transfer Function with and without the 50Ω Series Resistor on V_{IN}

CAP

CAP (pin 4) is the output of the internal reference buffer. A 10μF tantalum capacitor should be placed as close to the CAP as possible to provide optimum switching currents for the CDAC throughout the conversion cycle and compensation for the output of the buffer. Using a capacitor any smaller than 1μF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 10μF will have little effect on improving performance. The voltage on the CAP pin is approximately 2V when using the internal reference, or 80% of an externally supplied reference.

LAYOUT

POWER

The ADS7810 uses the majority of its power for analog and static circuitry, and it should be considered as an analog component. For optimum performance, tie the analog and digital +5V power pins to the same +5V power supply and tie the analog and digital grounds together.

For best performance, the ±5V supplies can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If ±12V or ±15V supplies are present, simple regulators can be used. The +5V power for the A/D should be separate from the +5V used for the system's digital logic. Connecting $+V_{DIG}$ (pin 27) directly to a digital supply can reduce converter performance due to switching noise from the digital logic.

Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both V_{DIG} and V_{ANA} should be tied to the same +5V source.

GROUNDING

Three ground pins are present on the ADS7810. DGND (pin 22) is the digital supply ground. AGND2 (pin 5) is the analog supply ground. AGND1 (pin 2) is the ground which all analog signals internal to the A/D are referenced. AGND1 is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the ADS should be tied to the analog ground plane, separated from the system digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the *system* ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The resistive front end of the ADS7810 attenuates this charge and reduces its magnitude significantly—reducing the burden on the external input amplifier or buffer.

However, keep in mind that maintaining signal integrity at voltage swings of ±10V and frequencies of several hundred kilohertz is extremely challenging. In addition, the external input amplifier must drive the ADS7810 mainly during its sample period—roughly 200ns. This will require a highspeed, precision amplifier which can swing to greater than ±10V.

For signals where the predominant frequencies are below 200kHz, the OPA671 operational amplifier should be adequate for most applications. In some cases or where input frequencies are higher, a composite configuration of the OPA671 and BUF634 (in its wide bandwidth mode) may be the best choice. See the BUF634 data sheet for more information.

The resistive front end of the ADS7810 also provides an ensured ±25V over voltage protection. In most cases, this eliminates the need for external input protection circuitry.

INTERMEDIATE LATCHES

The ADS7810 does have 3-state outputs for the parallel port, but intermediate latches should be used if the bus will be active during conversions. If the bus is not active during conversions, the 3-state outputs can be used to isolate the A/D from other peripherals on the same bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS7810 has an internal LSB size of 610mV. Transients from fast switching signals on the parallel port, even when the A/D is 3-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance.

REVISION HISTORY

Changes from Original (March, 1998) to Revision A **Page**

- Updated document format to meet current standards 1
- Updated *Features* list item indicating max INL and DNL specifications 1
- Changed indicated temperature range in *Description* section 1
- Updated *Ordering Information* table 2
- Changed temperature range for Electrical Characteristics measurement conditions 3
- Changed ADS7810U integral linearity error to ±3 LSB 3
- Changed ADS7810UB integral linearity error to ±3 LSB 3
- Changed differential linearity error for both ADS7810U and ADS7810UB to ±3 LSB 3
- Changed ADS7810U full-scale error to ±3 LSB 3
- Changed ADS7810UB full-scale error to ±3 LSB 3
- Changed ADS7810U full-scale error with ext.2.5V Ref to ±1 LSB 3
- Changed ADS7810UB full-scale error with ext.2.5V Ref to ±1 LSB 3
- Changed temperature range for Electrical Characteristics measurement conditions 4
- Changed specified temperature range to –40°C to +70°C 4

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
ADS7810U	NRND	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS7810U B	
ADS7810UB	NRND	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS7810U B	
ADS7810UBE4	NRND	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS7810U B	
ADS7810UE4	NRND	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS7810U B	

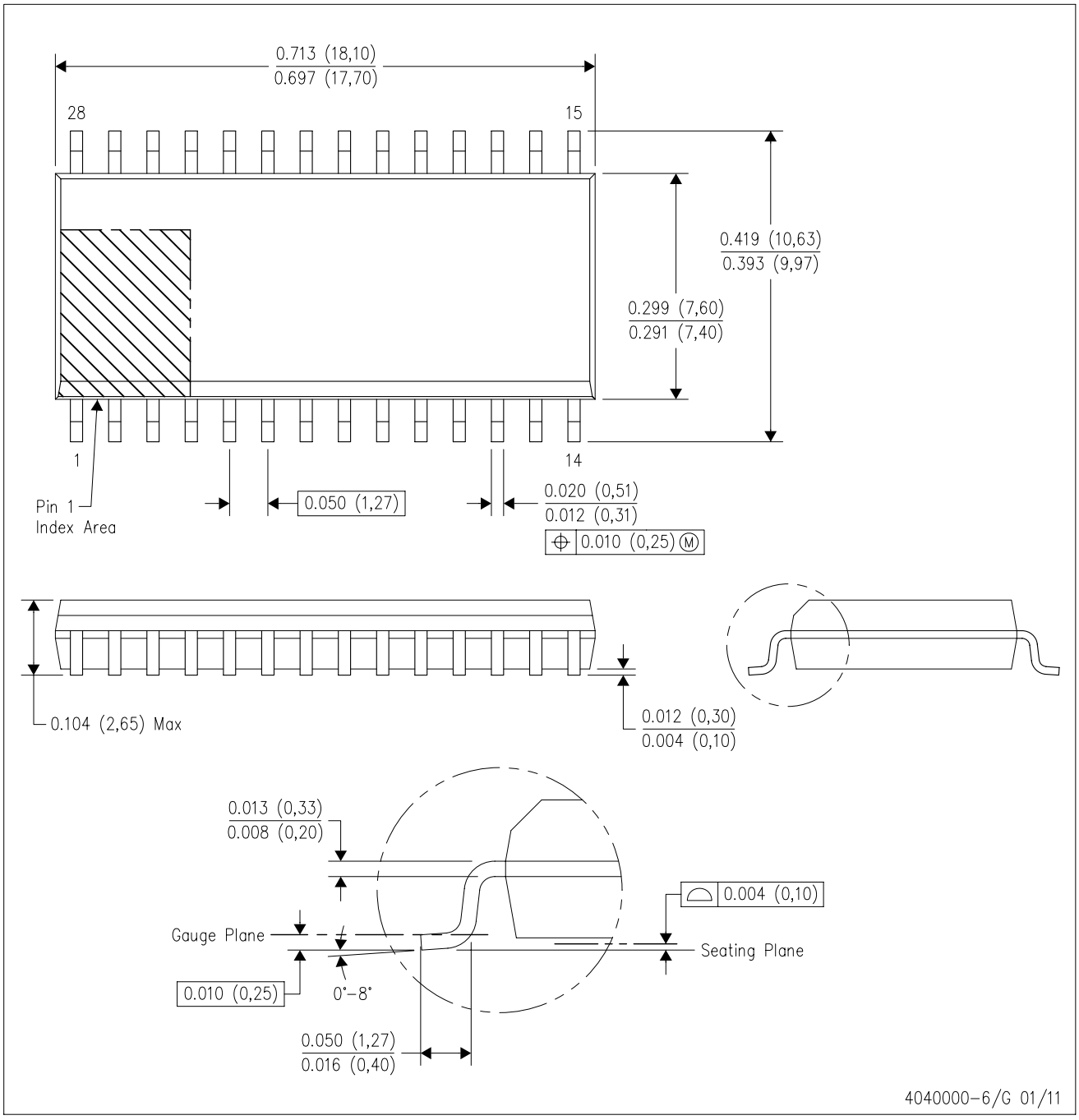
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

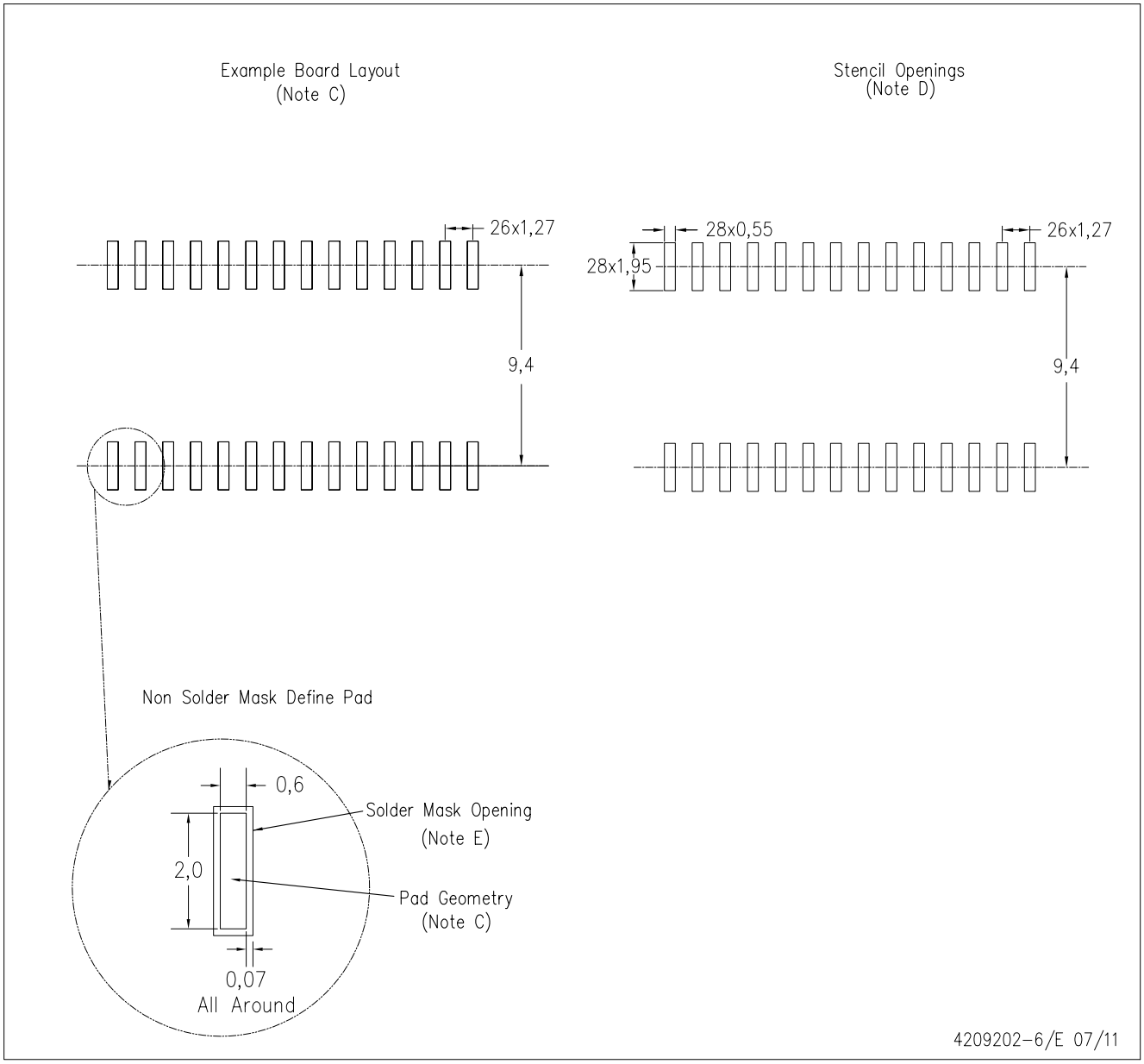
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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