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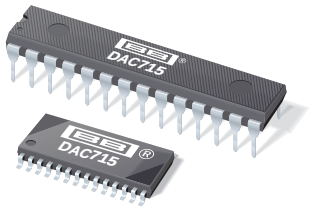


DAC715

16-BIT DIGITAL-TO-ANALOG CONVERTER with 16-Bit Bus Interface

FEATURES

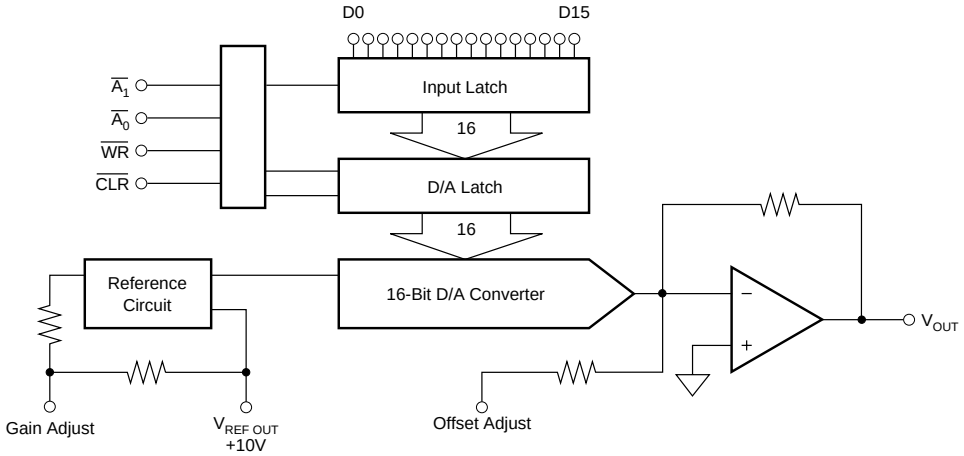
- HIGH-SPEED 16-BIT PARALLEL DOUBLE-BUFFERED INTERFACE
- VOLTAGE OUTPUT: 0 to +10V
- 13-, 14-, 15-BIT LINEARITY GRADES
- 16-BIT MONOTONIC OVER TEMPERATURE (L GRADE)
- POWER DISSIPATION: 600mW max
- GAIN AND OFFSET ADJUST: Convenient for Auto-Cal D/A Converters
- 28-LEAD DIP AND SOIC PACKAGES

DESCRIPTION

The DAC715 is a complete monolithic digital-to-analog converter including a +10V temperature compensated reference, current-to-voltage amplifier, 16-bit parallel interface that is double buffered, and an asynchronous clear function which immediately sets the output voltage to one-half of full-scale.

The output voltage range is 0 to +10V while operating from ±12V or ±15V supplies. The gain and bipolar offset adjustments are designed so that they can be set via external potentiometers or external D/A converters. The output amplifier is protected against short circuit to ground.

The 28-pin DAC715 is available in a 0.3" plastic DIP and wide-body plastic SOIC package. The DAC715P, U, PB, and UB are specified over the –40°C to +85°C temperature range while the DAC715PK, UK, PL, and UL are specified over the 0°C to +70°C range.



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SBAS046

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, V_{CC} = ±15V, and after a 10-minute warm-up, unless otherwise noted.

	DAC715P, U			DAC715PB, UB			DAC715PK, UK			DAC715PL, UL			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT													
RESOLUTION			16			*			*			*	Bits
DIGITAL INPUTS													
Input Code		Binary Two's Complement			*			*			*		
Logic Levels[1]: V_{IH}	+2.0		$+V_{CC}$ – 1.4	*		*	*		*	*		*	V
V_{IL}	0		+0.8	*		*	*		*	*		*	V
I_{IH} (V_I = +2.7V)			±10			*			*			*	µA
I_{IL} (V_I = +0.4V)			±10			*			*			*	µA
TRANSFER CHARACTERISTICS													
ACCURACY													
Linearity Error			±4			±2			±2			±2	LSB
T_{MIN} to T_{MAX}			±8			±4			±2			±2	LSB
Differential Linearity Error			±4			±2			±2			±1	LSB
T_{MIN} to T_{MAX}			±8			±4			±2			±1	LSB
Monotonicity Over Temp	13			14			15			16			Bits
Gain Error[3]			±0.1			±0.1			*			*	%
T_{MIN} to T_{MAX}			±0.2			±0.15			*			*	%
Offset Error[3]			±0.1			*			*			*	% FSR[2]
T_{MIN} to T_{MAX}			±0.2			*			*			*	% FSR
Power Supply Sensitivity Of Full Scale			±0.003			*			*			*	% FSR/%V_{CC}
			±30			*			*			*	PPM FSR/%V_{CC}
DYNAMIC PERFORMANCE													
Settling Time (to ±0.003%FSR, 5kΩ ll 500pF Load)[4]													
10V Output Step		6	10		*	*		*	*		*	*	µs
1 LSB Output Step[5]		4			*			*			*		µs
Output Slew Rate		10			*			*			*		V/µs
Total Harmonic Distortion + Noise													
0dB, 1001Hz, f_S = 100kHz		0.005			*			*			*		%
–20dB, 1001Hz, f_S = 100kHz		0.03			*			*			*		%
–60dB, 1001Hz, f_S = 100kHz		3.0			*			*			*		%
SINAD													
1001Hz, f_S = 100kHz		87			*			*			*		dB
Digital Feedthrough[5]		2			*			*			*		nV-s
Digital-to-Analog Glitch Impulse[5]		15			*			*			*		nV-s
Output Noise Voltage (includes Reference)		120			*			*			*		nV$\sqrt{Hz}$
ANALOG OUTPUT													
Output Voltage Range													
$+V_{CC}$, $-V_{CC}$ = ±11.4V	0 to +10			*			*			*			V
Output Current	±5			*			*			*			mA
Output Impedance		0.1			*			*			*		Ω
Short Circuit to ACOM													
Duration		Indefinite			*			*			*		
REFERENCE VOLTAGE													
Voltage	+9.975	+10.000	+10.025	*	*	*	*	*	*	*	*	*	V
T_{MIN} to T_{MAX}	+9.960		+10.040	*		*	*		*	*		*	V
Output Resistance		1			*			*			*		Ω
Source Current	2			*			*			*			mA
Short Circuit to ACOM, Duration		Indefinite			*			*			*		
POWER SUPPLY REQUIREMENTS													
Voltage: $+V_{CC}$	+11.4	+15	+16.5	*	*	*	*	*	*	*	*	*	V
$-V_{CC}$	–16.5	–15	–11.4	*	*	*	*	*	*	*	*	*	V
Current (no load, ±15V Supplies)													
$+V_{CC}$		13	15		*	*		*	*		*	*	mA
$-V_{CC}$		22	25		*	*		*	*		*	*	mA
Power Dissipation		525	600		*	*		*	*		*	*	mW
TEMPERATURE RANGE													
Specification All Grades													
	–40		+85	*		*	0		+70	*		*	°C
Storage	–60		+150	*		*	*		*	*		*	°C
Thermal Resistance θ_{JA}													
DIP Package		75			*			*			*		°C/W
SOIC Package		75			*			*			*		°C/W

* Specifications are the same as grade to the left.

NOTES: (1) Digital inputs are TTL and +5V CMOS compatible over the specification temperature range. (2) FSR means Full Scale Range. For example, for a 0 to +10V output, FSR = 10V. (3) Errors externally adjustable to zero. (4) Maximum represents greater than the 3σ limit. Not 100% tested for this parameter. (5) For the worst case code changes: $FFFF_H$ to 0000_H and 0000_H to $FFFF_H$. These are Binary Two's Complement (BTC) codes. (6) Typical supply voltages times maximum currents.

ABSOLUTE MAXIMUM RATINGS(1)

$+V_{CC}$ to COMMON	0V, +17V
$-V_{CC}$ to COMMON	0V, –17V
$+V_{CC}$ to $-V_{CC}$	34V
Digital Inputs to COMMON	–1V to $+V_{CC}$
External Voltage Applied to BPO and Range Resistors	$\pm V_{CC}$
$V_{REF\ OUT}$	Indefinite Short to COMMON
V_{OUT}	Indefinite Short to COMMON
Power Dissipation	750mW
Storage Temperature	–60°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PACKAGE INFORMATION

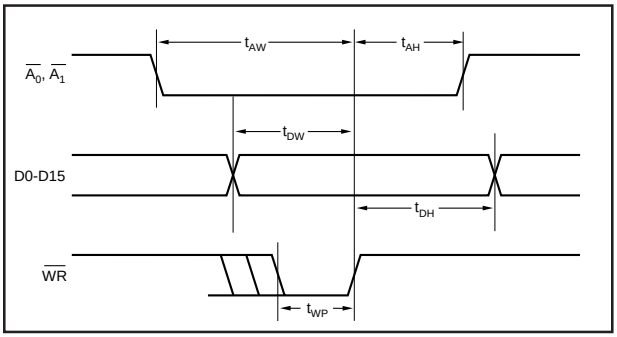
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
DAC715P	Plastic DIP	246
DAC715U	Plastic SOIC	217
DAC715PB	Plastic DIP	246
DAC715UB	Plastic SOIC	217
DAC715PK	Plastic DIP	246
DAC715UK	Plastic SOIC	217
DAC715PL	Plastic DIP	246
DAC715UL	Plastic SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

PRODUCT	PACKAGE	TEMPERATURE RANGE	DIFFERENTIAL LINEARITY ERROR MAX at +25°C
DAC715P	Plastic DIP	–40°C to +85°C	±4LSB
DAC715U	Plastic SOIC	–40°C to +85°C	±4LSB
DAC715PB	Plastic DIP	–40°C to +85°C	±2LSB
DAC715UB	Plastic SOIC	–40°C to +85°C	±2LSB
DAC715PK	Plastic DIP	0°C to 70°C	±2LSB
DAC715UK	Plastic SOIC	0°C to 70°C	±2LSB
DAC715PL	Plastic DIP	0°C to 70°C	±1LSB
DAC715UL	Plastic SOIC	0°C to 70°C	±1LSB

TIMING DIAGRAM



TIMING SPECIFICATIONS

T_A = –40°C to +85°C, $+V_{CC}$ = +12V or +15V, $-V_{CC}$ = –12V or –15V.

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{DW}	Data Valid to End of $\overline{WR}$	50		ns
t_{AW}	$\overline{A_0}$, $\overline{A_1}$ Valid to End of $\overline{WR}$	50		ns
t_{AH}	$\overline{A_0}$, $\overline{A_1}$ Hold after End of $\overline{WR}$	10		ns
t_{DH}	Data Hold after end of $\overline{WR}$	10		ns
t_{WP}(1)	Write Pulse Width	50		ns
t_{CP}	CLEAR Pulse Width	200		ns

NOTES: (1) For single-buffered operation, t_{WP} is 80ns min. Refer to page 10.

TRUTH TABLE

$\overline{A_0}$	$\overline{A_1}$	$\overline{WR}$	$\overline{CLR}$	DESCRIPTION
0	1	$1 \rightarrow 0 \rightarrow 1$	1	Load Input Latch
1	0	$1 \rightarrow 0 \rightarrow 1$	1	Load D/A Latch
1	1	$1 \rightarrow 0 \rightarrow 1$	1	No Change
0	0	0	1	Latches Transparent
X	X	1	1	No Change
X	X	X	0	Reset D/A Latch

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

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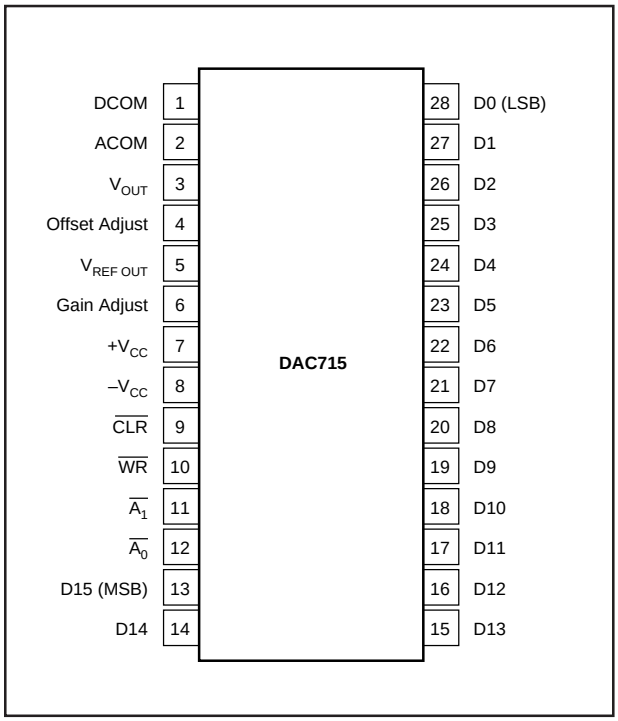
PIN CONFIGURATION



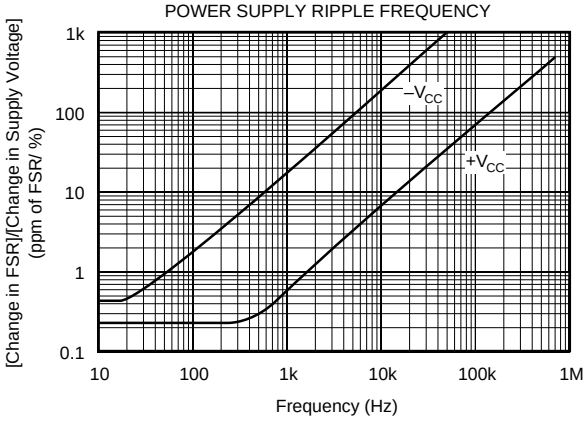
PIN DESCRIPTIONS

PIN	LABEL	DESCRIPTION
1	DCOM	Digital Ground
2	ACOM	Analog Ground
3	V_{OUT}	0 to +10V D/A Output
4	Offset Adjust	Offset Adjust
5	$V_{REF\ OUT}$	Voltage Reference Output
6	Gain Adjust	Gain Adjust
7	$+V_{CC}$	+12V to +15V Supply
8	$-V_{CC}$	–12V to –15V Supply
9	$\overline{CLR}$	CLEAR. Sets D/A output to Half Scale (Active Low)
10	$\overline{WR}$	Write (Active Low)
11	$\overline{A_1}$	Enable for D/A latch (Active Low)
12	$\overline{A_0}$	Enable for Input latch (Active Low)
13	D15	Data Bit 15 (Most Significant Bit)
14	D14	Data Bit 14
15	D13	Data Bit 13
16	D12	Data Bit 12
17	D11	Data Bit 11
18	D10	Data Bit 10
19	D9	Data Bit 9
20	D8	Data Bit 8
21	D7	Data Bit 7
22	D6	Data Bit 6
23	D5	Data Bit 5
24	D4	Data Bit 4
25	D3	Data Bit 3
26	D2	Data Bit 2
27	D1	Data Bit 1
28	D0	Data Bit 0 (Least Significant Bit)

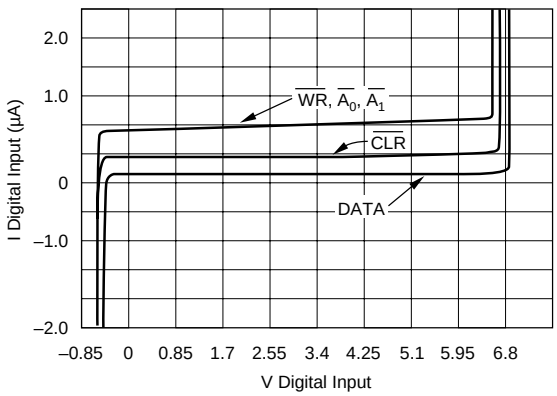
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, and V_{CC} = ±15V, unless otherwise noted.

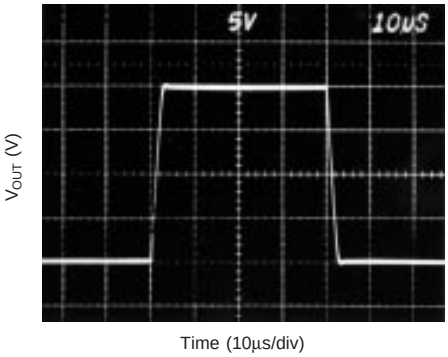
POWER SUPPLY REJECTION vs
POWER SUPPLY RIPPLE FREQUENCY



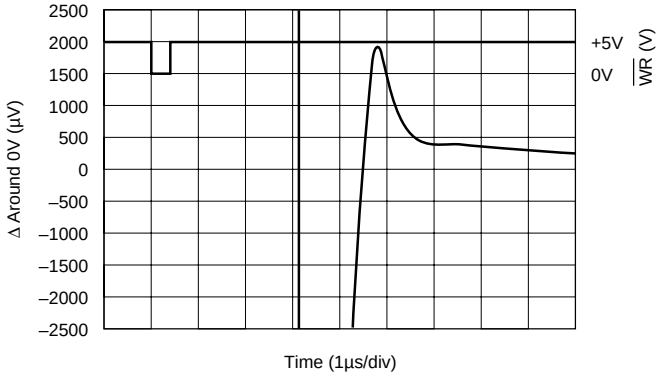
LOGIC vs V LEVEL



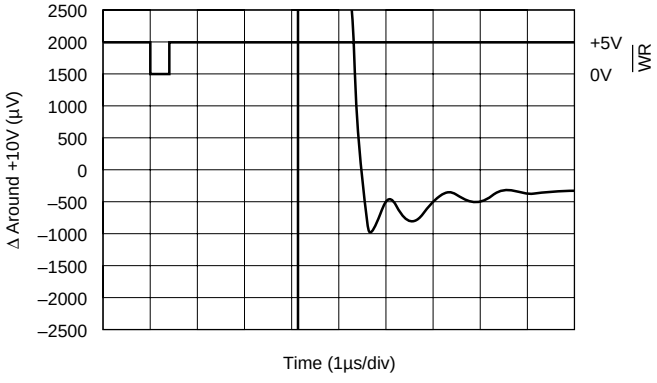
FULL-SCALE OUTPUT SWING



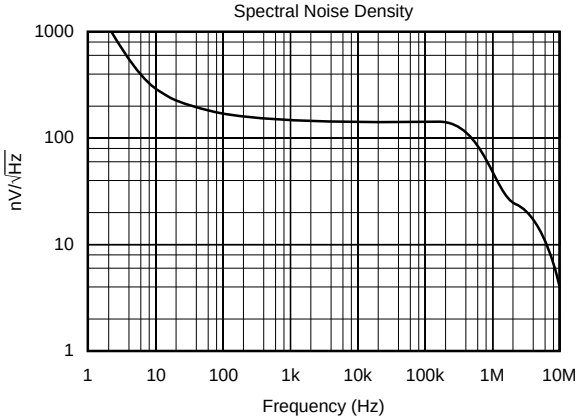
SETTLING TIME, +10V TO 0V



SETTLING TIME, 0V TO +10V



Spectral Noise Density



DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of the analog output from a straight line drawn between the end points of the transfer characteristic.

DIFFERENTIAL LINEARITY ERROR

Differential linearity error (DLE) is the deviation from 1LSB of an output change from one adjacent state to the next. A DLE specification of ±1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the digital input code changes from one code word to the adjacent code word. If the DLE is more positive than –1LSB, the D/A is said to be monotonic.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital input values. Monotonicity of DAC715 is guaranteed over the specification temperature range to 13-, 14-, 15-, and 16-bits for performance grades DAC715P/U, DAC715PB/UB, DAC715PK/UK, and DAC715PL/UL respectively.

SETTLING TIME

Settling time is the total time (including slew time) for the D/A output to settle to within an error band around its final value after a change in input. Settling times are specified to within ±0.003% of Full Scale Range (FSR) for an output step change of 10V and 1LSB. The 1LSB change is measured at the Major Carry ($FFFF_H$ to 0000_H, and 0000_H to $FFFF_H$: BTC codes), the input transition at which worst-case settling time occurs.

TOTAL HARMONIC DISTORTION

Total harmonic distortion is defined as the ratio of the square root of the sum of the squares of the values of the harmonics to the value of the fundamental frequency. It is expressed in % of the fundamental frequency amplitude at sampling rate f_S.

SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)

SINAD includes all the harmonic and outstanding spurious components in the definition of output noise power in addition to quantizing and internal random noise power. SINAD is expressed in dB at a specified input frequency and sampling rate, f_S.

DIGITAL-TO-ANALOG GLITCH IMPULSE

The amount of charge injected into the analog output from the digital inputs when the inputs change state. It is measured at half scale at the input codes where as many as possible switches change state—from $FFFF_H$ to 0000_H.

DIGITAL FEEDTHROUGH

When the D/A is not selected, high frequency logic activity on the digital inputs is coupled through the device and shows up as output noise. This noise is digital feedthrough.

OPERATION

The DAC715 is a monolithic integrated-circuit 16-bit D/A converter complete with 16-bit D/A switches and ladder network, voltage reference, output amplifier and microprocessor bus interface.

INTERFACE LOGIC

The DAC715 has double-buffered data latches. The input data latch holds a 16-bit data word before loading it into the second latch, the D/A latch. This double-buffered organization permits simultaneous update of several D/A converters. All digital control inputs are active low. Refer to the block diagram shown in Figure 1.

All latches are level-triggered. Data present when the enable inputs are logic “0” will enter the latch. When the enable inputs return to logic “1”, the data is latched.

The $\overline{CLR}$ input resets both the input latch and the D/A latch to give a half scale output.

LOGIC INPUT COMPATIBILITY

The DAC715 digital inputs are TTL compatible (1.4V switching level), low leakage, and high impedance. Thus the inputs are suitable for being driven by any type of 5V logic family, such as CMOS logic. An equivalent circuit for the digital inputs is shown in Figure 2.

The inputs will float to logic “0” if left unconnected. It is recommended that any unused inputs be connected to DCOM to improve noise immunity.

Digital inputs remain high impedance when power is off.

INPUT CODING

The DAC715 is designed to accept binary two’s complement (BTC) input codes. For unipolar analog output configuration, a digital input of $7FFF_H$ gives a full scale output, 8000_H gives a zero output, and 0000_H gives half scale output.

INTERNAL REFERENCE

The DAC715 contains a +10V reference. The reference output may be used to drive external loads, sourcing up to 2mA. The load current should be constant, otherwise the gain of the converter will vary.

OUTPUT VOLTAGE SWING

The output amplifier of the DAC715 is committed to a 0 to +10V output range. It will provide a 0 to +10V output swing while operating on ±11.4V or higher voltage supplies.

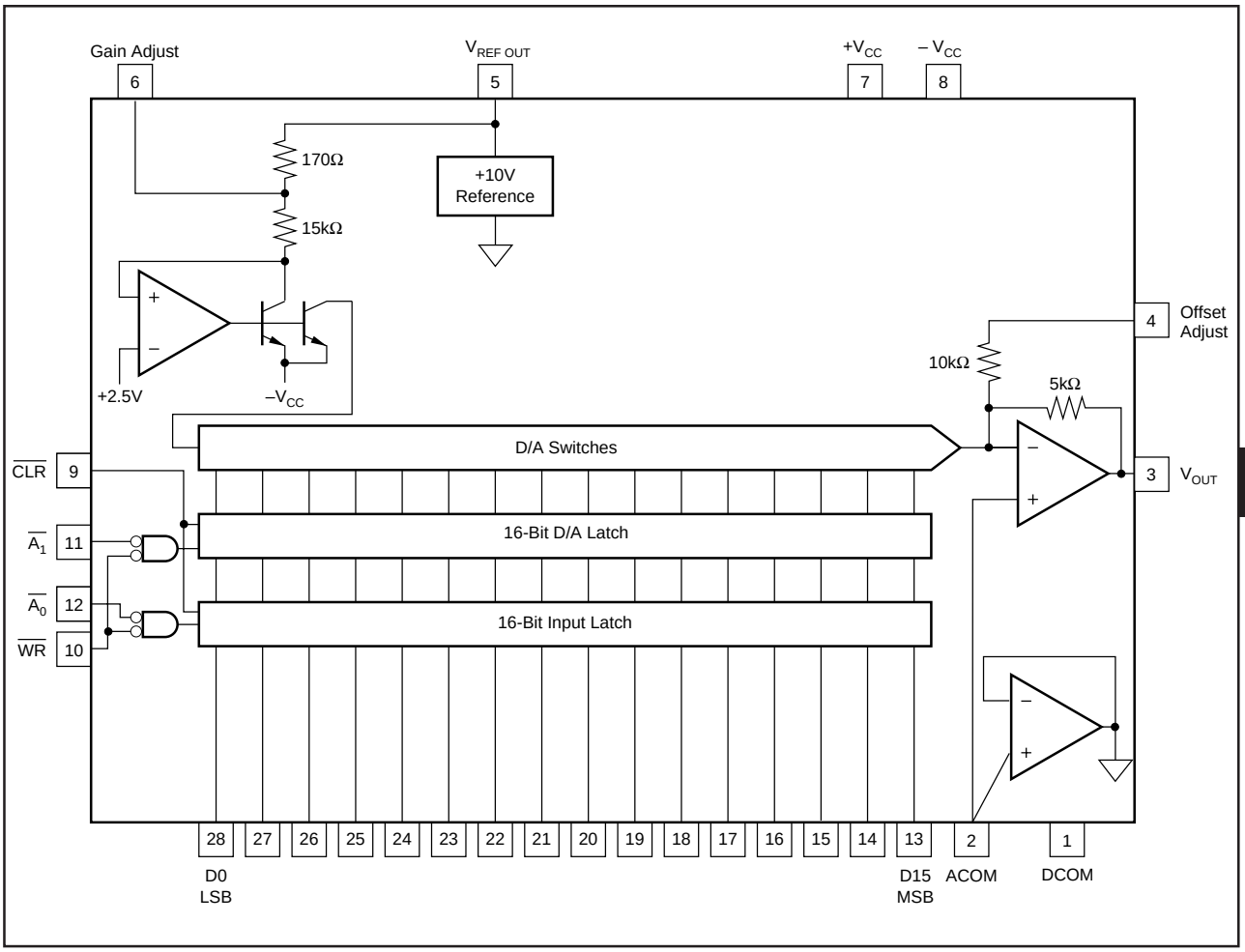


FIGURE 1. DAC715 Block Diagram.

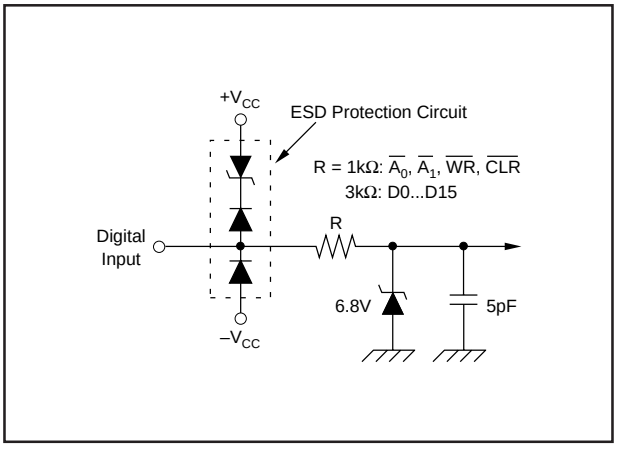


FIGURE 2. Equivalent Circuit of Digital Inputs.

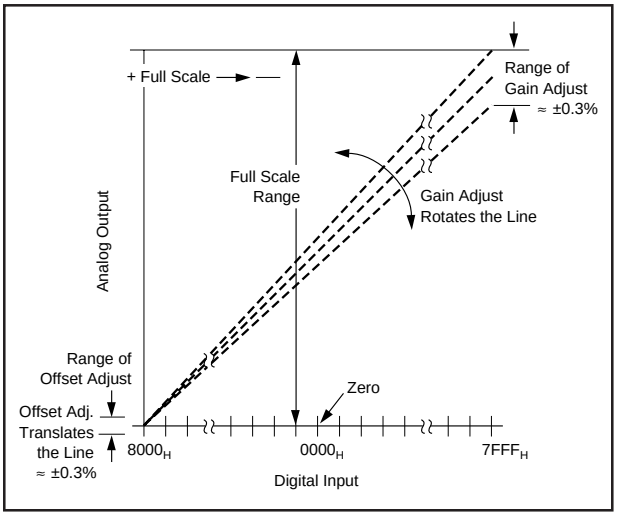


FIGURE 3. Relationship of Offset and Gain Adjustments.

GAIN AND OFFSET ADJUSTMENTS

Figure 3 illustrates the relationship of offset and gain adjustments for a unipolar connected D/A converter. Offset should be adjusted first to avoid interaction of adjustments. See Table I for calibration values and codes. These adjustments have a minimum range of ±0.3%.

Offset Adjustment

Apply the digital input code that produces zero output voltage and adjust the offset potentiometer or the offset adjust D/A converter for 0V.

DAC715 CALIBRATION VALUES 1 LEAST SIGNIFICANT BIT = 152µV		
DIGITAL INPUT CODE BINARY TWO'S COMPLEMENT, BTC	ANALOG OUTPUT (V)	DESCRIPTION
$7FFF_H$	9.999847	Full Scale –1LSB
4000_H	7.5	3/4 Scale
0001_H	5.000152	Half Scale + 1LSB
0000_H	5	Half Scale
$FFFF_H$	4.999847	Half Scale – 1LSB
$C000_H$	2.5	1/4 Scale
8000_H	0	Zero

TABLE I. Digital Input and Analog Output Voltage Calibration Values.

Gain Adjustment

Apply the digital input that gives the maximum positive voltage output. Adjust the gain potentiometer or the gain adjust D/A converter for this positive full scale voltage.

INSTALLATION

GENERAL CONSIDERATIONS

Due to the high-accuracy of the DAC715, system design problems such as grounding and contact resistance become very important. A 16-bit converter with a 10V full-scale range has a 1LSB value of 152µV. With a load current of 5mA, series wiring and connector resistance of only 60mΩ will cause a voltage drop of 300µV. To understand what this means in terms of a system layout, the resistivity of a typical 1 ounce copper-clad printed circuit board is 1/2 mΩ per square. For a 5mA load, a 10 milliinch wide printed circuit conductor 60 milliinches long will result in a voltage drop of 150µV.

The analog output of DAC715 has an LSB size of 152µV (–96dB). The noise floor of the D/A must remain below this level in the frequency range of interest. The DAC715's noise spectral density (which includes the noise contributed by the internal reference) is shown in the Typical Performance Curves section.

Wiring to high-resolution D/A converters should be routed to provide optimum isolation from sources of RFI and EMI. The key to elimination of RF radiation or pickup is small loop area. Signal leads and their return conductors should be kept close together such that they present a small capture cross-section for any external field. Wire-wrap construction is not recommended.

POWER SUPPLY AND REFERENCE CONNECTIONS

Power supply decoupling capacitors should be added as shown in Figure 4. Best performance occurs using a 1 to 10µF tantalum capacitor at $-V_{CC}$. Applications with less critical settling time may be able to use 0.01µF at $-V_{CC}$ as well as at $+V_{CC}$. The capacitors should be located close to the package.

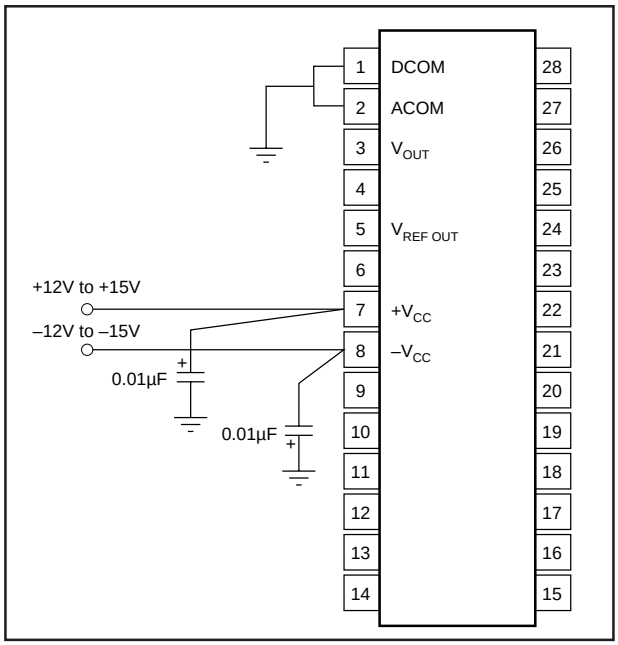


FIGURE 4. Power Supply Connections.

The DAC715 has separate ANALOG COMMON and DIGITAL COMMON pins. The current through DCOM is mostly switching transients and are up to 1mA peak in amplitude. The current through ACOM is typically 5µA for all codes.

Use separate analog and digital ground planes with a single interconnection point to minimize ground loops. The analog pins are located adjacent to each other to help isolate analog from digital signals. Analog signals should be routed as far as possible from digital signals and should cross them at right angles. A solid analog ground plane around the D/A package, as well as under it in the vicinity of the analog and power supply pins, will isolate the D/A from switching currents. It is recommended that DCOM and ACOM be connected directly to the ground planes under the package.

If several DAC715s are used or if DAC715 shares supplies with other components, connecting the ACOM and DCOM lines together once at the power supplies rather than at each chip may give better results.

LOAD CONNECTIONS

Since the reference point for V_{OUT} and $V_{REF\ OUT}$ is the ACOM pin, it is important to connect the D/A converter load directly to the ACOM pin. Refer to Figure 5.

Lead and contact resistances are represented by R_1 through R_3. As long as the load resistance R_L is constant, R_1 simply introduces a gain error and can be removed by gain adjustment of the D/A or system-wide gain calibration. R_2 is part of R_L if the output voltage is sensed at ACOM.

In some applications it is impractical to return the load to the ACOM pin of the D/A converter. Sensing the output voltage at the SYSTEM GROUND point is reasonable, because there is no change in DAC715 ACOM current, provided that

R_3 is a low-resistance ground plane or conductor. In this case you may wish to connect DCOM to SYSTEM GROUND as well.

GAIN AND OFFSET ADJUST

Connections Using Potentiometers

GAIN and OFFSET adjust pins provide for trim using external potentiometers. 15-turn potentiometers provide sufficient resolution. Range of adjustment of these trims is at least ±0.3% of Full Scale Range. Refer to Figure 6.

Using D/A Converters

The GAIN ADJUST and OFFSET ADJUST circuits of the DAC715 have been arranged so that these points may be easily driven by external D/A converters. Refer to Figure 7. 12-bit D/A converters provide an OFFSET adjust resolution and a GAIN adjust resolution of 30µV to 50µV per LSB step.

Nominal values of GAIN and OFFSET occur when the D/A converters outputs are at approximately half scale, 0V.

DIGITAL INTERFACE

BUS INTERFACE

The DAC715 has a 16-bit double-buffered data interface with control lines for easy connection to a 16-bit bus. The double-buffered feature permits update of several D/As simultaneously.

A_0 is the enable control for the DATA INPUT LATCH. A_1 is the enable for the D/A LATCH. $\overline{WR}$ is used to strobe data into latches enabled by A_0, and $\overline{A_1}$. Refer to the block diagram of Figure 1 and to Timing Diagram on page 3.

$\overline{CLR}$ sets the INPUT DATA LATCH and D/A LATCH to $\overline{0000}_H$ (5V at the D/A output).

SINGLE-BUFFERED OPERATION

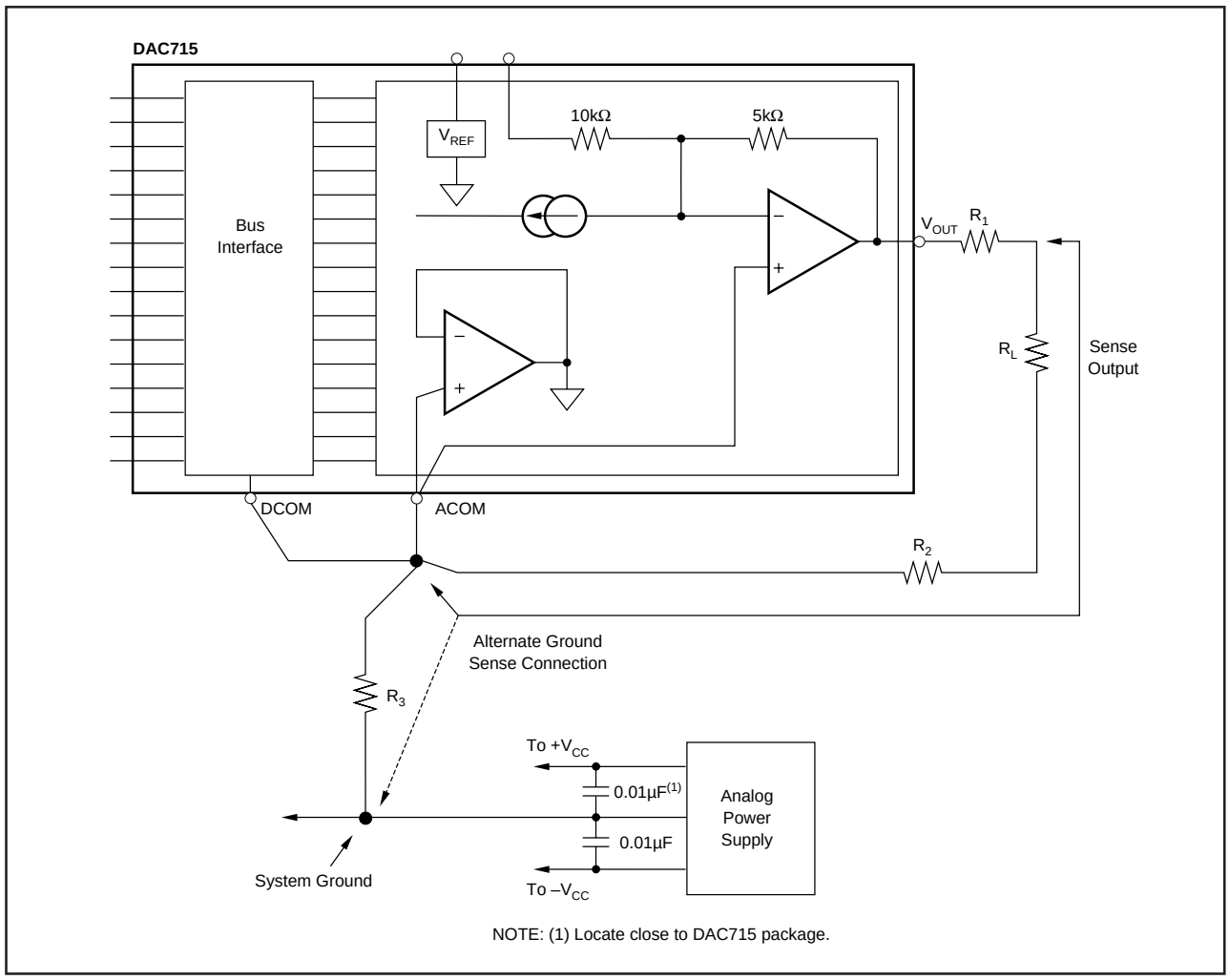


FIGURE 5. System Ground Considerations for High-Resolution D/A Converters.

To operate the DAC715 interface as a single-buffered latch, the DATA INPUT LATCH is permanently enabled by connecting A_0 to DCOM. If A_1 is not used to enable the D/A, it should be connected to DCOM also. For this mode of operation, the width of WR will need to be at least 80ns minimum to pass data through the DATA INPUT LATCH and into the D/A LATCH.

The digital interface of the DAC715 can be made transparent by asserting A_0, A_1, and WR LOW, and asserting CLR HIGH.

TRANSPARENT INTERFACE

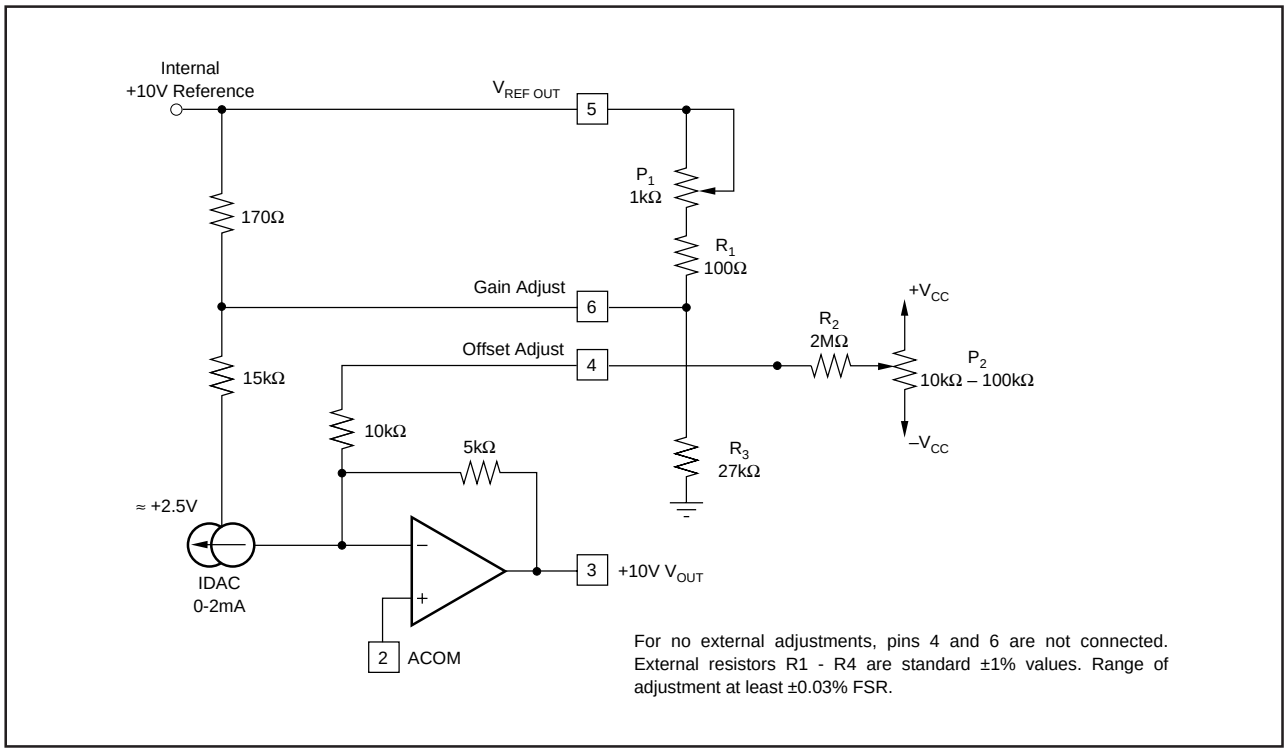


FIGURE 6. Manual Offset and Gain Adjust Circuits.

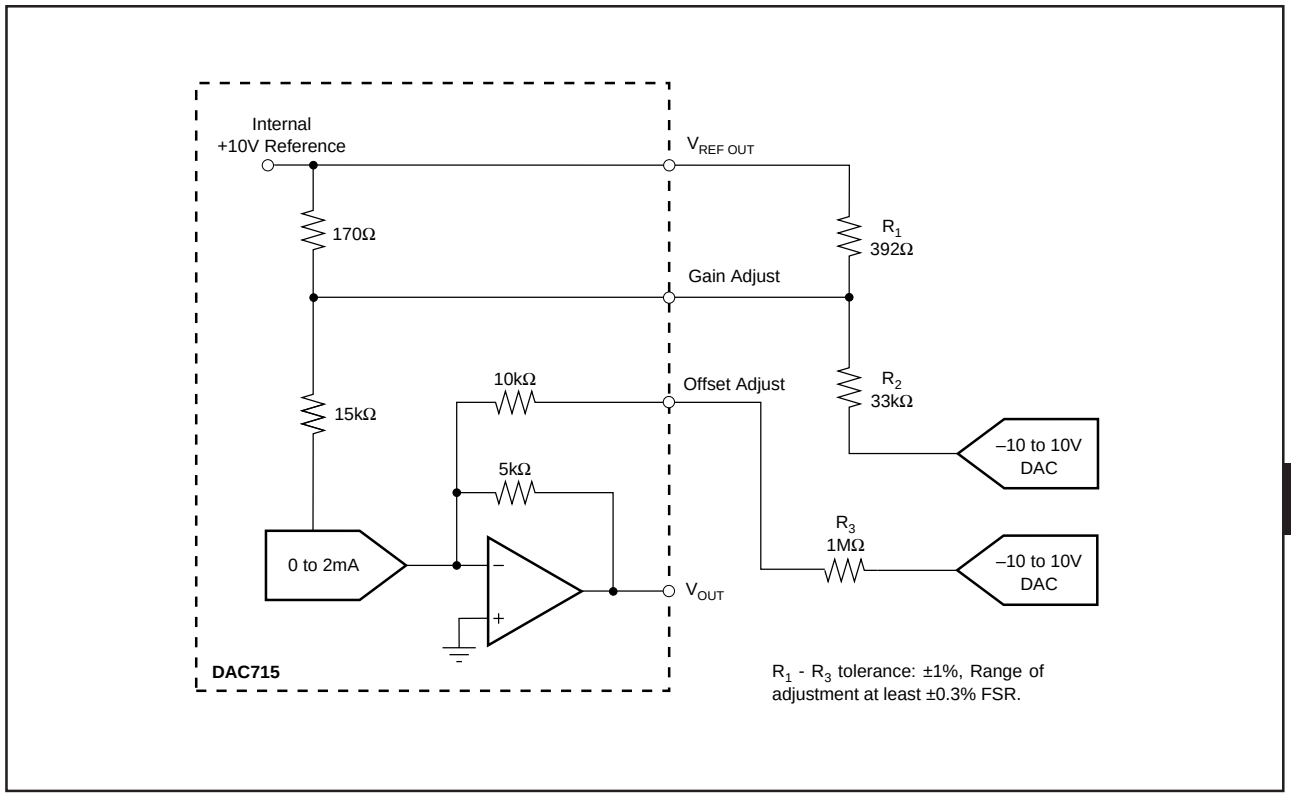


FIGURE 7. Gain and Offset Adjustment Using D/A Converters.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC715P	NRND	PDIP	NT	28	13	TBD	Call TI	Call TI	-40 to 85	DAC715P L	
DAC715PB	NRND	PDIP	NT	28	13	TBD	Call TI	Call TI	-40 to 85	DAC715P B	
DAC715PBG4	NRND	PDIP	NT	28	13	TBD	Call TI	Call TI	-40 to 85	DAC715P B	
DAC715PG4	NRND	PDIP	NT	28	13	TBD	Call TI	Call TI	-40 to 85	DAC715P L	
DAC715PK	NRND	PDIP	NT	28	13	TBD	Call TI	Call TI	0 to 70	DAC715P K	
DAC715PKG4	NRND	PDIP	NT	28	13	TBD	Call TI	Call TI	0 to 70	DAC715P K	
DAC715PL	NRND	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	DAC715P L	
DAC715PLG4	NRND	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	DAC715P L	
DAC715U	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC715U	Samples
DAC715UB	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC715U B	Samples
DAC715UBG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC715U B	Samples
DAC715UG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC715U	Samples
DAC715UK	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	DAC715U K	Samples
DAC715UKG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	DAC715U K	Samples
DAC715UL	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	DAC715U L	Samples
DAC715ULG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	DAC715U L	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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