

## 16-Bit, 500kSPS, *microPower* Sampling ANALOG-TO-DIGITAL CONVERTER

 Check for Samples: [ADS8323](#)

### FEATURES

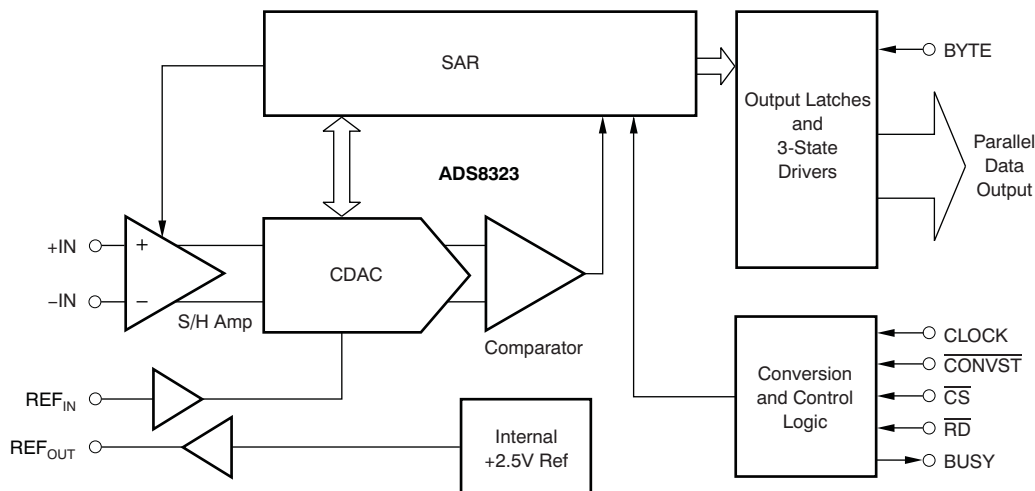
- HIGH-SPEED PARALLEL INTERFACE
- 500kSPS SAMPLING RATE
- LOW POWER: 85mW at 500kSPS
- BIPOLAR INPUT RANGE
- TQFP-32 PACKAGE

### APPLICATIONS

- HIGH-SPEED DATA ACQUISITION
- OPTICAL POWER MONITORING
- MOTOR CONTROL
- ATE

### DESCRIPTION

The ADS8323 is a 16-bit, 500kSPS analog-to-digital converter (ADC) with an internal 2.5V reference. The device includes a 16-bit, capacitor-based successive approximation register (SAR) ADC with inherent sample-and-hold. The ADS8323 offers a full 16-bit interface, or an 8-bit option where data are read using two read cycles. The ADS8323 is available in a TQFP-32 package and is specified over the industrial  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  temperature range.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	NO MISSING CODES ERROR (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	TRANSPORT MEDIA, QUANTITY
ADS8323Y	±8	14	TQFP-32	PBS	-40°C to +85°C		Tape and reel, 250 Tape and reel, 2000
ADS8323YB	±6	15	TQFP-32	PBS	-40°C to +85°C		Tape and reel, 250 Tape and reel, 2000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature range (unless otherwise noted).

	ADS8323	UNIT
Supply voltage, DGND to DV <sub>DD</sub>	-0.3 to 6	V
Supply voltage, AGND to AV <sub>DD</sub>	-0.3 to 6	V
Analog input voltage range	AGND - 0.3 to AVDD + 0.3	V
Reference input voltage	AGND - 0.3 to AVDD + 0.3	V
Digital input voltage range	DGND - 0.3 to DVDD + 0.3	V
Ground voltage differences, AGND to DGND	±0.3	V
Voltage differences, DVDD to AGND	-0.3 to 6	V
Power dissipation	850	mW
Operating virtual junction temperature range, T <sub>J</sub>	-40 to +150	°C
Operating free-air temperature range, T <sub>A</sub>	-40 to +85	°C
Storage temperature range	-65 to +150	°C

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

### RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	MIN	NOM	MAX	UNIT
<b>POWER SUPPLY</b>				
AV <sub>DD</sub> <sup>(1)</sup>	4.75	5.0	5.25	V
DV <sub>DD</sub> <sup>(1)</sup>	4.75	5.0	5.25	V
<b>ANALOG/REFERENCE INPUTS</b>				
Differential analog input voltage, IN+ to IN-	-REF <sub>IN</sub>		+REF <sub>IN</sub>	V
External reference voltage	1.5	2.5	2.55	V

(1) The voltage difference between AV<sub>DD</sub> and DV<sub>DD</sub> terminals cannot exceed 0.3V to maintain performance specifications.

### DISSIPATION RATINGS

PACKAGE	T <sub>A</sub> ≤ +25°C POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = +25°C <sup>(1)</sup>	T <sub>A</sub> = +70°C POWER RATING	T <sub>A</sub> = +85°C POWER RATING
TQFP-32	1636mW	13.09mW/°C	1047mW	850mW

(1) This is the inverse of the traditional junction-to-ambient thermal resistance (R<sub>θJA</sub>). Thermal resistances are not production tested and are for informational purposes only.

## ELECTRICAL CHARACTERISTICS

At  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $+DV_{\text{DD}} = +AV_{\text{DD}} = +5\text{V}$ ,  $V_{\text{REF}} = +2.5\text{V}$ ,  $f_{\text{SAMPLE}} = 500\text{kSPS}$ , and  $f_{\text{CLK}} = 20 \cdot f_{\text{SAMPLE}}$ , unless otherwise specified.

PARAMETER	TEST CONDITIONS	ADS8323Y			ADS8323YB <sup>(1)</sup>			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>RESOLUTION</b>								
Resolution			16			16		Bits
<b>ANALOG INPUT</b>								
Full-scale input span <sup>(2)</sup>	+IN – (–IN)	$-V_{\text{REF}}$		$+V_{\text{REF}}$	$-V_{\text{REF}}$		$+V_{\text{REF}}$	V
Absolute input range	+IN	–0.3		$AV_{\text{DD}} + 0.3$	–0.3		$AV_{\text{DD}} + 0.3$	V
	–IN	–0.3		$AV_{\text{DD}} + 0.3$	–0.3		$AV_{\text{DD}} + 0.3$	V
Capacitance			25			25		pF
Leakage current			$\pm 1$			$\pm 1$		nA
<b>SYSTEM PERFORMANCE</b>								
No missing codes		14			15			Bits
Integral linearity error			$\pm 4$	$\pm 8$		$\pm 3$	$\pm 6$	LSB <sup>(3)</sup>
Differential linearity error			$\pm 3$			$\pm 1$		LSB
Offset error			$\pm 1$	$\pm 2$		$\pm 0.5$	$\pm 1.0$	mV
Gain error <sup>(4)</sup>			$\pm 0.25$	$\pm 0.50$		$\pm 0.12$	$\pm 0.25$	%FSR
Common-mode rejection ratio	At dc		70			70		dB
	$V_{\text{IN}} = 1V_{\text{PP}}$ at 1MHz		50			50		dB
Noise			60			60		$\mu\text{V}_{\text{RMS}}$
Power-supply rejection ratio	At FFFFh output code		$\pm 3$			$\pm 3$		LSBs
<b>SAMPLING DYNAMICS</b>								
Conversion time				1.6			1.6	$\mu\text{s}$
Acquisition time		350			350			ns
Throughput rate				500			500	kSPS
Aperture delay			10			10		ns
Aperture jitter			30			30		ps
Small-signal bandwidth			20			20		MHz
Step response			100			100		ns
Overvoltage recovery			150			150		ns
<b>DYNAMIC CHARACTERISTICS</b>								
Total harmonic distortion <sup>(5)</sup>	$V_{\text{IN}} = 5V_{\text{PP}}$ at 100kHz		–90			–93		dB
SINAD	$V_{\text{IN}} = 5V_{\text{PP}}$ at 100kHz		81			83		dB
Spurious free dynamic range	$V_{\text{IN}} = 5V_{\text{PP}}$ at 100kHz		94			96		dB
<b>REFERENCE OUTPUT</b>								
Voltage	$I_{\text{OUT}} = 0$	2.475	2.50	2.525	2.48	2.50	2.52	V
Source current	Static load			10			10	$\mu\text{A}$
Drift	$I_{\text{OUT}} = 0$		25			25		ppm/ $^{\circ}\text{C}$
Line regulation	$4.75\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$		0.6			0.6		mV
<b>REFERENCE INPUT</b>								
Range		1.5		2.55	1.5		2.55	V

(1) Shaded cells indicate different specifications from ADS8322Y.

(2) Ideal input span; does not include gain or offset error.

(3) LSB means least significant bit, with  $V_{\text{REF}}$  equal to  $+2.5\text{V}$ ;  $1\text{LSB} = 76\mu\text{V}$ .

(4) Measured relative to an ideal, full-scale input [+In – (–In)] of  $4.9999\text{V}$ . Thus, gain error includes the error of the internal voltage reference.

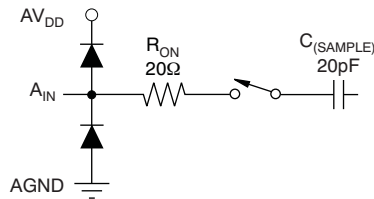
(5) Calculated on the first nine harmonics of the input frequency.

**ELECTRICAL CHARACTERISTICS (continued)**

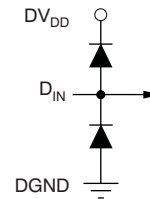
At  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $+DV_{DD} = +AV_{DD} = +5\text{V}$ ,  $V_{REF} = +2.5\text{V}$ ,  $f_{SAMPLE} = 500\text{kSPS}$ , and  $f_{CLK} = 20 \cdot f_{SAMPLE}$ , unless otherwise specified.

PARAMETER	TEST CONDITIONS	ADS8323Y			ADS8323YB <sup>(1)</sup>			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>DIGITAL INPUT/OUTPUT</b>								
Logic family			CMOS			CMOS		
Logic levels:								
$V_{IH}$	$I_{IH} \leq +5\mu\text{A}$	3.0		$+DV_{DD}$	3.0		$+DV_{DD}$	V
$V_{IL}$	$I_{IL} \leq -5\mu\text{A}$	-0.3		0.8	-0.3		0.8	V
$V_{OH}$	$I_{OH} = -1.6\text{mA}$	4.0			4.0			V
$V_{OL}$	$I_{OL} = +1.6\text{mA}$			0.4			0.4	V
Data format		Binary twos complement			Binary twos complement			
<b>POWER-SUPPLY REQUIREMENTS</b>								
Power-supply voltage								
$+AV_{DD}$		4.75	5	5.25	4.75	5	5.25	V
$+DV_{DD}$		4.75	5	5.25	4.75	5	5.25	V
Supply current	$f_{SAMPLE} = 500\text{kSPS}$		17	25		17	25	mA
Power dissipation	$f_{SAMPLE} = 500\text{kSPS}$		85	125		85	125	mW
<b>TEMPERATURE RANGE</b>								
Specified performance		-40		+85	-40		+85	$^{\circ}\text{C}$

**EQUIVALENT INPUT CIRCUITS**



Diode Turn-On Voltage: 0.35V  
Equivalent Analog Input Circuit



Equivalent Digital Input Circuit

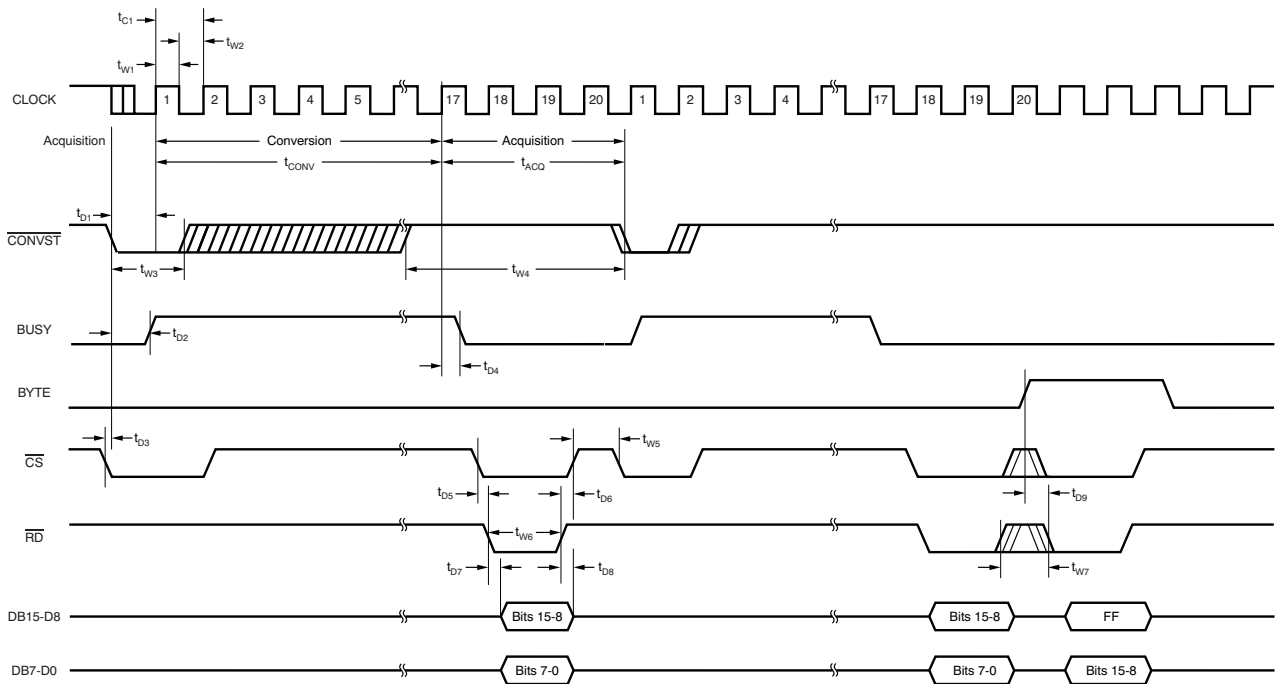


### PIN ASSIGNMENTS

TERMINAL		I/O <sup>(1)</sup>	DESCRIPTION
NO	NAME		
1	DB15	DO	Data Bit 15 (MSB)
2	DB14	DO	Data Bit 14
3	DB13	DO	Data Bit 13
4	DB12	DO	Data Bit 12
5	DB11	DO	Data Bit 11
6	DB10	DO	Data Bit 10
7	DB9	DO	Data Bit 9
8	DB8	DO	Data Bit 8
9	DB7	DO	Data Bit 7
10	DB6	DO	Data Bit 6
11	DB5	DO	Data Bit 5
12	DB4	DO	Data Bit 4
13	DB3	DO	Data Bit 3
14	DB2	DO	Data Bit 2
15	DB1	DO	Data Bit 1
16	DB0	DO	Data Bit 0 (LSB)
17	BUSY	DO	High when a conversion is in progress.
18	+DV <sub>DD</sub>	P	Digital Power Supply, +5VDC.
19	DGND	P	Digital Ground
20	CLOCK	DI	An external CMOS-compatible clock can be applied to the CLOCK input to synchronize the conversion process to an external source.
21	$\overline{\text{CONVST}}$	DI	Convert Start
22	$\overline{\text{RD}}$	DI	Synchronization pulse for the parallel output.
23	BYTE	DI	Selects eight most significant bits (low) or eight least significant bits (high). Data valid on pins 9-16.
24	$\overline{\text{CS}}$	DI	Chip Select
25	-IN	AI	Inverting Input Channel
26	+IN	AI	Noninverting Input Channel
27	AGND	P	Analog Ground
28	+AV <sub>DD</sub>	P	Analog Power Supply, +5VDC.
29	NC	—	No connection
30	NC	—	No connection
31	REF <sub>IN</sub>	AI	Reference Input. When using the internal 2.5V reference, tie this pin directly to REF <sub>OUT</sub> .
32	REF <sub>OUT</sub>	AO	Reference Output. A 0.1μF capacitor should be connected to this pin when the internal reference is used.

(1) **AI** is analog input, **AO** is analog output, **DI** is digital input, **DO** is digital output, and **P** is power-supply connection.

TIMING INFORMATION



TIMING CHARACTERISTICS<sup>(1)(2)</sup>

All specifications typical at -40°C to +85°C, +DV<sub>DD</sub> = +5V.

PARAMETER	TEST CONDITIONS	ADS8323			UNIT
		MIN	TYP	MAX	
t <sub>CONV</sub>	Conversion Time			1.6	μs
t <sub>AQC</sub>	Acquisition Time	350			ns
t <sub>C1</sub>	CLOCK Period	100			ns
t <sub>W1</sub>	CLOCK High Time	40			ns
t <sub>W2</sub>	CLOCK Low Time	40			ns
t <sub>D1</sub>	CONVST Low to Clock High	10			ns
t <sub>W3</sub>	CONVST Low Time	20			ns
t <sub>D2</sub>	CONVST Low to BUSY High			25	ns
t <sub>D3</sub>	CS Low to CONVST Low	0			ns
t <sub>W4</sub>	CONVST High	20			ns
t <sub>D4</sub>	CLOCK High to BUSY Low			25	ns
t <sub>W5</sub>	CS High	0			ns
t <sub>D5</sub>	CS Low to RD Low	0			ns
t <sub>D6</sub>	RD High to CS High	0			ns
t <sub>W6</sub>	RD Low Time	50			ns
t <sub>D7</sub>	RD Low to Data Valid	40			ns
t <sub>D8</sub>	Data Hold from RD High	5			ns
t <sub>D9</sub>	BYTE Change to RD Low <sup>(3)</sup>	0			ns
t <sub>W7</sub>	RD High Time	20			ns

- (1) All input signals are specified with rise and fall times of 5ns, t<sub>R</sub> = t<sub>F</sub> = 5ns (10% to 90% of DV<sub>DD</sub>) and timed from a voltage level of (V<sub>IL</sub> + V<sub>IH</sub>) / 2.
- (2) See timing diagram.
- (3) BYTE is asynchronous; when BYTE is '0', bits 15 through 0 appear at DB15-DB0. When BYTE is '1', bits 15 through 8 appear on DB7-DB0. RD may remain low between changes in BYTE.

**TYPICAL CHARACTERISTICS**

At  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $+DV_{DD} = +AV_{DD} = +5\text{V}$ ,  $V_{REF} = +2.5\text{V}$ ,  $f_{SAMPLE} = 500\text{kSPS}$ , and  $f_{CLK} = 20 \cdot f_{SAMPLE}$ , unless otherwise specified.

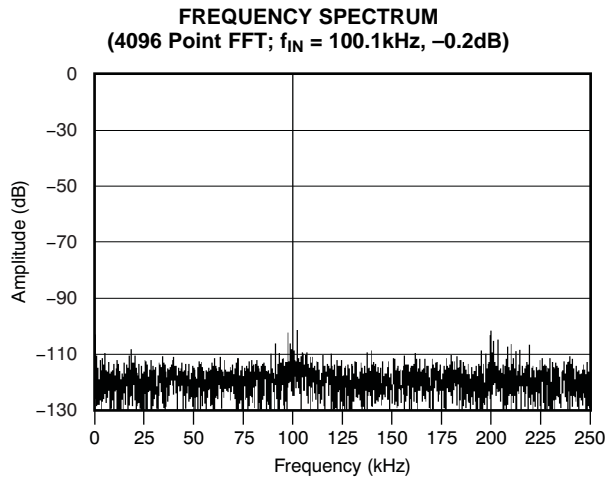


Figure 1.

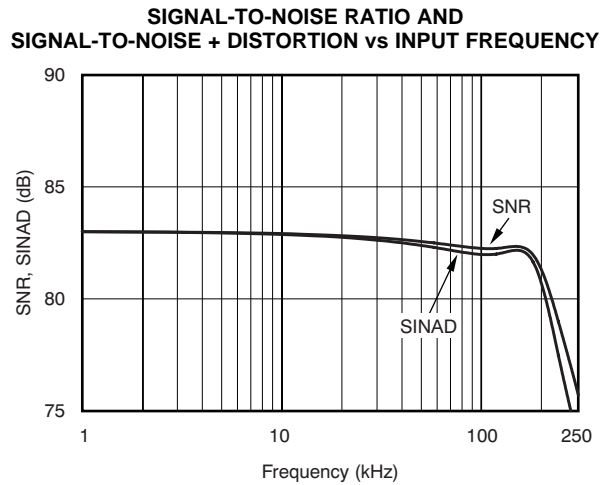


Figure 2.

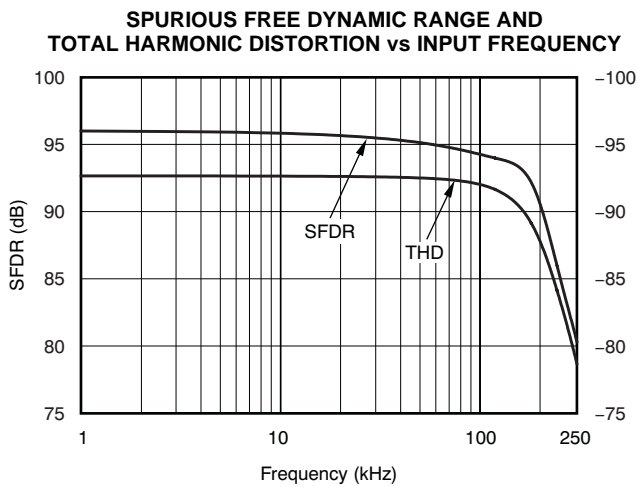


Figure 3.

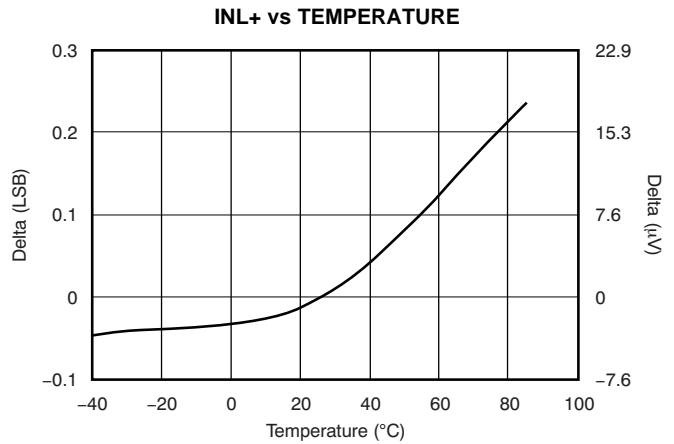


Figure 4.

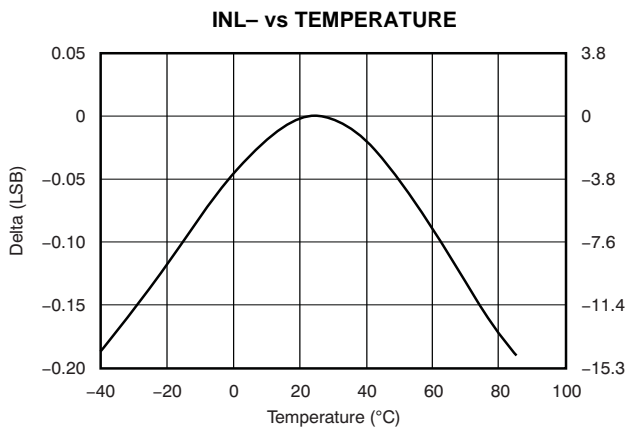


Figure 5.

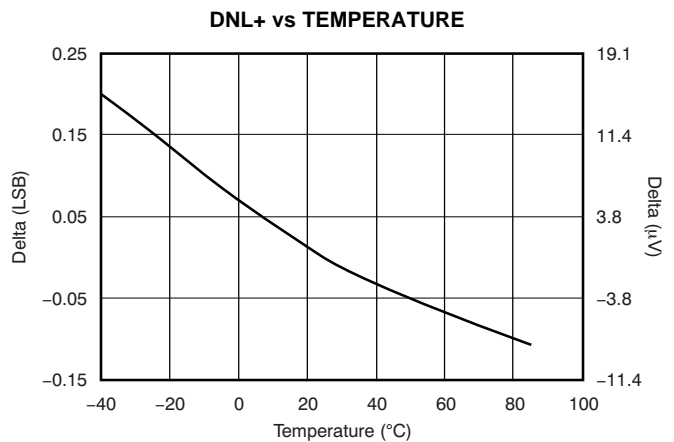


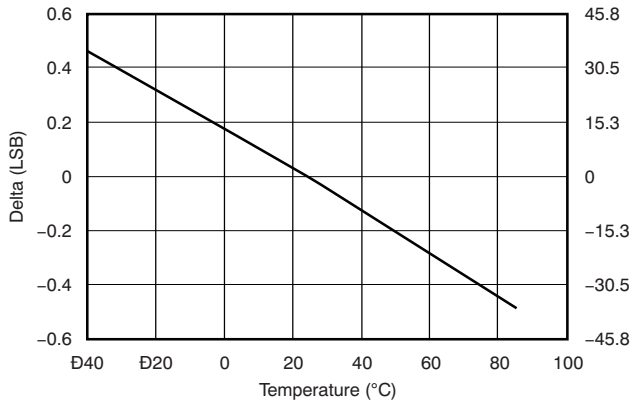
Figure 6.



**TYPICAL CHARACTERISTICS (continued)**

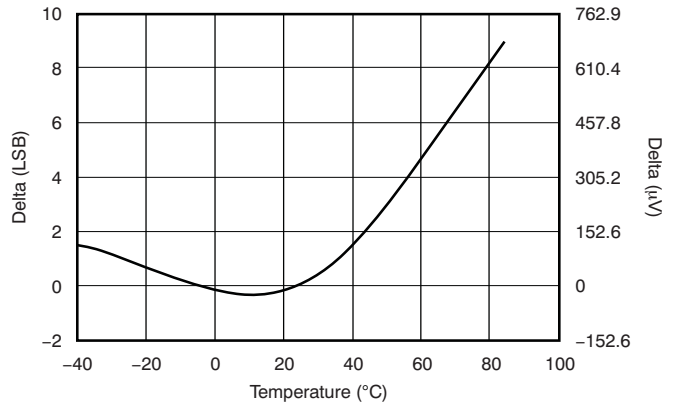
At  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $+DV_{DD} = +AV_{DD} = +5\text{V}$ ,  $V_{REF} = +2.5\text{V}$ ,  $f_{SAMPLE} = 500\text{kSPS}$ , and  $f_{CLK} = 20 \cdot f_{SAMPLE}$ , unless otherwise specified.

**DNL- vs TEMPERATURE**



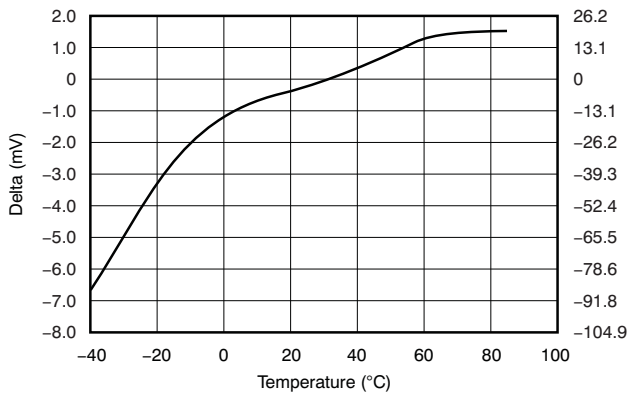
**Figure 7.**

**GAIN ERROR vs TEMPERATURE**



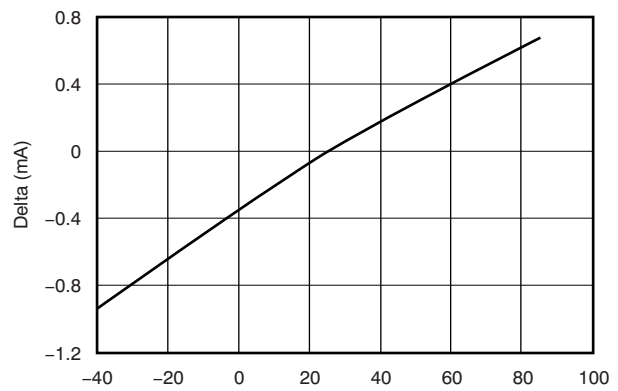
**Figure 8.**

**V<sub>REF</sub> vs TEMPERATURE**



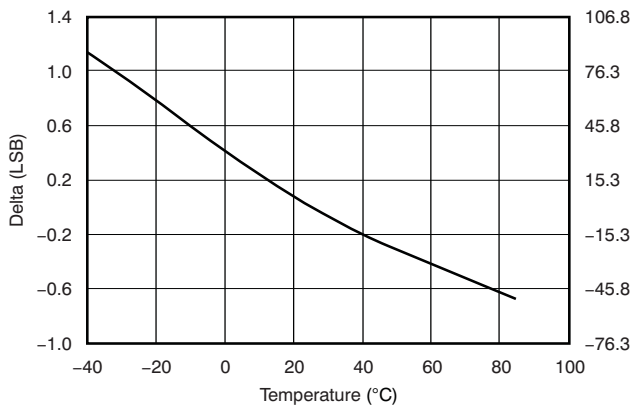
**Figure 9.**

**I<sub>Q</sub> vs TEMPERATURE**



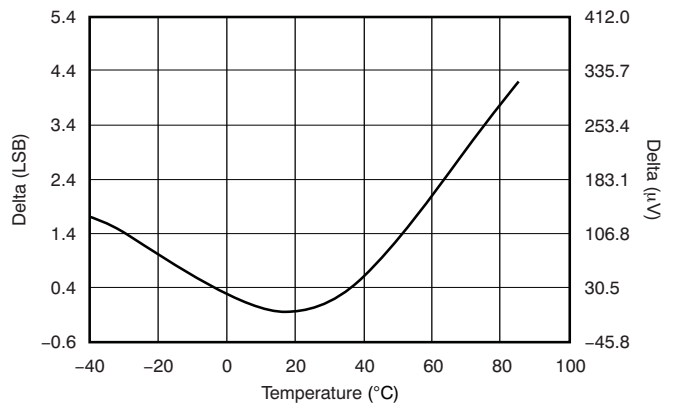
**Figure 10.**

**BIPOLAR ZERO vs TEMPERATURE**



**Figure 11.**

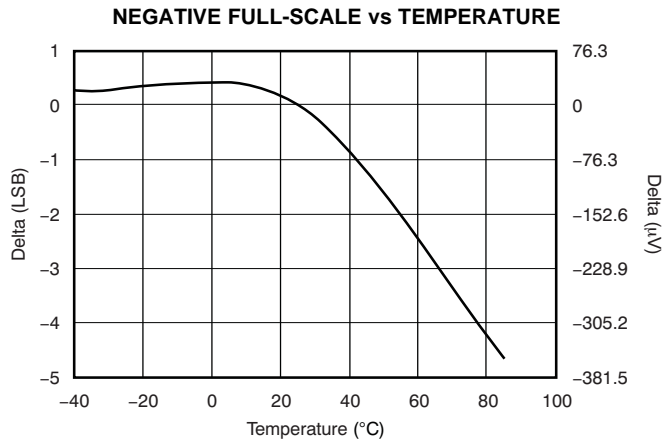
**POSITIVE FULL-SCALE vs TEMPERATURE**



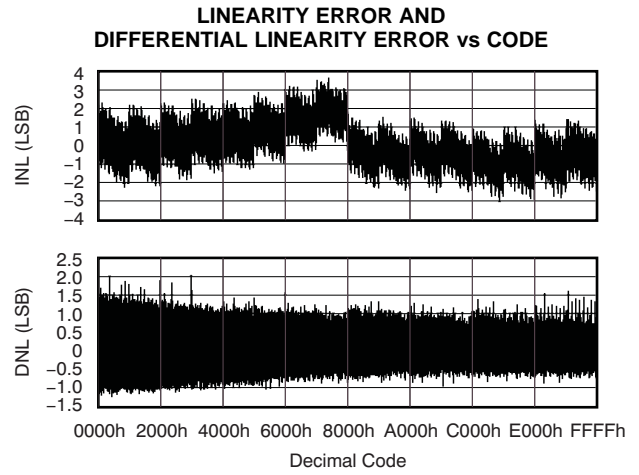
**Figure 12.**

**TYPICAL CHARACTERISTICS (continued)**

At  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $+DV_{DD} = +AV_{DD} = +5\text{V}$ ,  $V_{REF} = +2.5\text{V}$ ,  $f_{SAMPLE} = 500\text{kSPS}$ , and  $f_{CLK} = 20 \cdot f_{SAMPLE}$ , unless otherwise specified.



**Figure 13.**



**Figure 14.**

### THEORY OF OPERATION

The ADS8322 is a high-speed successive approximation register (SAR) A/D converter with an internal 2.5V bandgap reference that operates from a single +5V supply. The input is fully differential with a typical common-mode rejection of 70dB. The device accepts a differential analog input voltage in the range of  $-V_{REF}$  to  $+V_{REF}$ , centered on the common-mode voltage (see the [Analog Input](#) section). The device also accepts bipolar input ranges when a level shift circuit is used at the front end (see [Figure 21](#)). The basic operating circuit for the ADS8323 is shown in [Figure 15](#).

The ADS8323 requires an external clock to run the conversion process. This clock can vary between 25kHz (1.25kHz throughput) and 10MHz (500kSPS throughput). The duty cycle of the clock is unimportant as long as the minimum high and low times are at least 40ns and the clock period is at least 100ns. The minimum clock frequency is governed by the parasitic leakage of the Capacitive Digital-to-Analog Converter (CDAC) capacitors internal to the ADS8323.

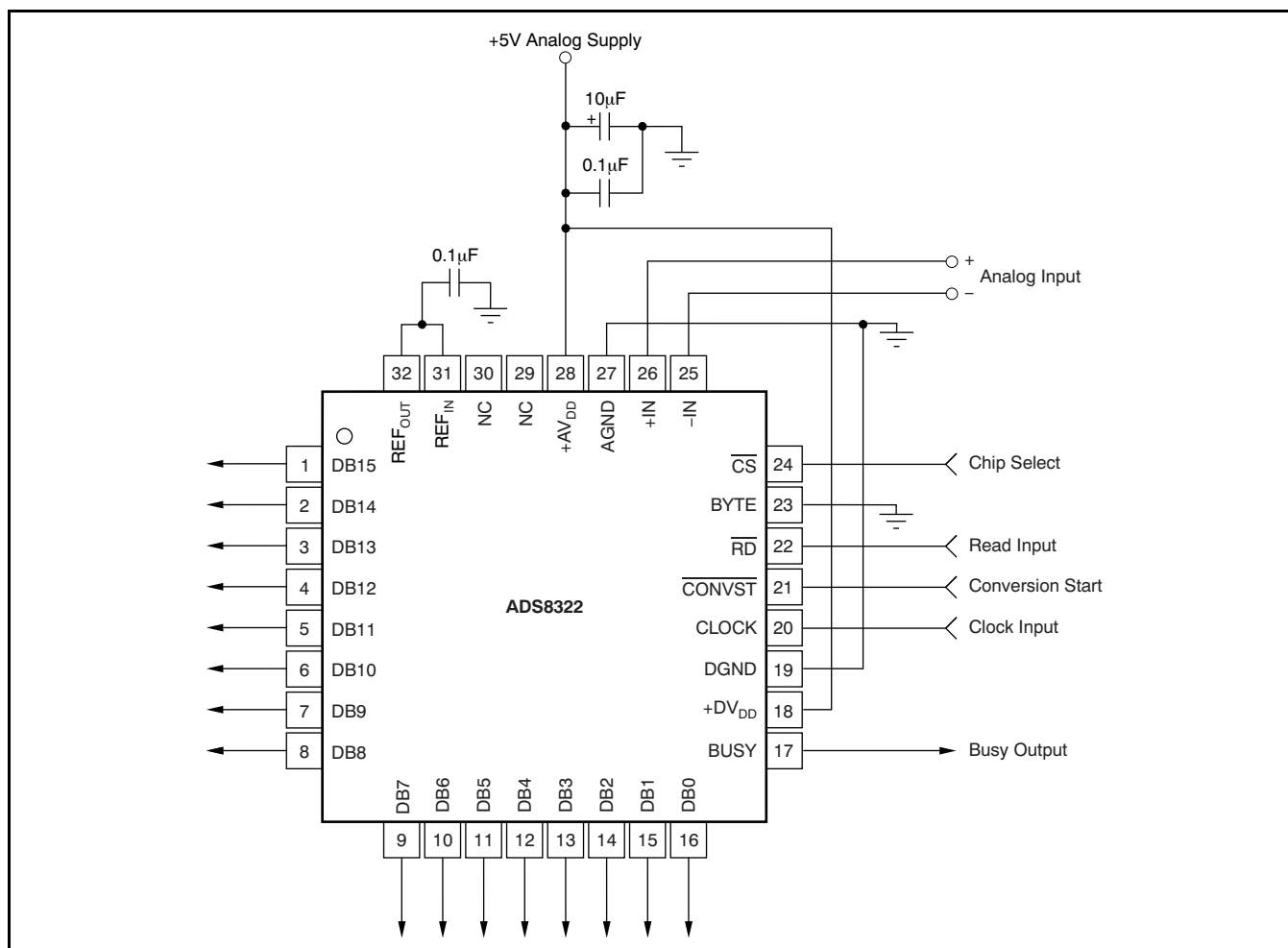


Figure 15. Typical Circuit Configuration

The analog input is provided to two input pins, +IN and –IN. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. A conversion is initiated on the ADS8323 by bringing  $\overline{\text{CONVST}}$  (pin 21) low for a minimum of 20ns.  $\overline{\text{CONVST}}$  low places the sample-and-hold amplifier in the hold state and the conversion process is started. The BUSY output (pin 17) goes high when the conversion begins and stays high during the conversion. While a conversion is in progress, both inputs are disconnected from any internal function. When the conversion result is latched into the output register, the BUSY signal goes low. The data can be read from the parallel output bus following the conversion by bringing both  $\overline{\text{RD}}$  and  $\overline{\text{CS}}$  low.

**NOTE:** This mode of operation is described in more detail in the *Timing and Control* section of this data sheet.

## SAMPLE-AND-HOLD SECTION

The sample-and-hold on the ADS8323 allows the ADC to accurately convert an input sine wave of full-scale amplitude to 16-bit resolution. The input bandwidth of the sample-and-hold is greater than the Nyquist rate (Nyquist equals one-half of the sampling rate) of the ADC even when the ADC is operated at its maximum throughput rate of 500kSPS. The typical small-signal bandwidth of the sample-and-hold amplifier is 20MHz. The typical aperture delay time, or the time it takes for the ADS8323 to switch from the sample to the hold mode following the negative edge of the  $\overline{\text{CONVST}}$  signal, is 10ns. The average

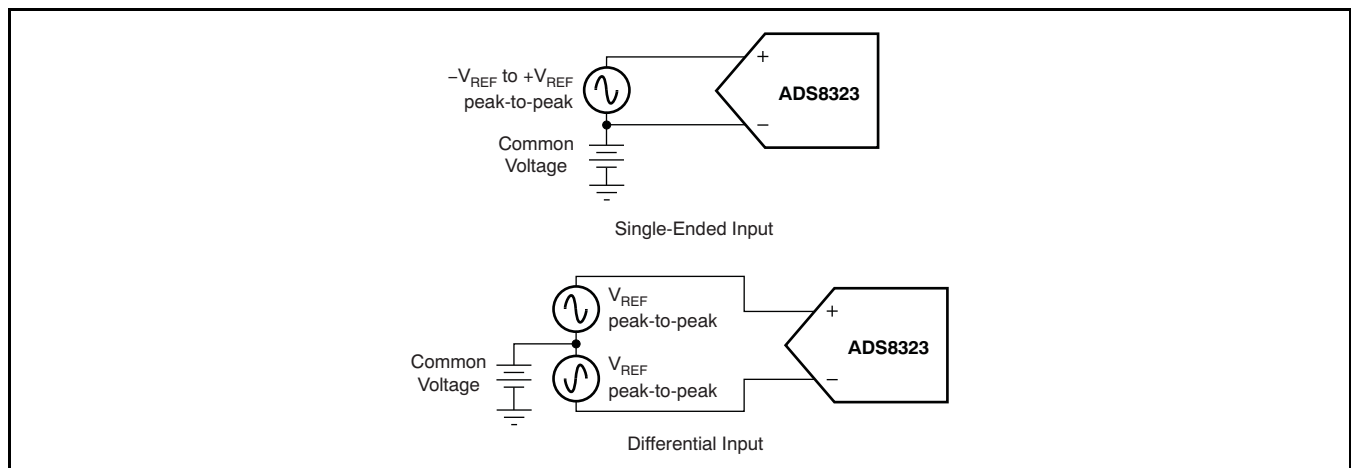
delta of repeated aperture delay values is typically 30ps (also known as aperture jitter). These specifications reflect the ability of the ADS8323 to capture ac input signals accurately at the exact same moment in time.

## REFERENCE

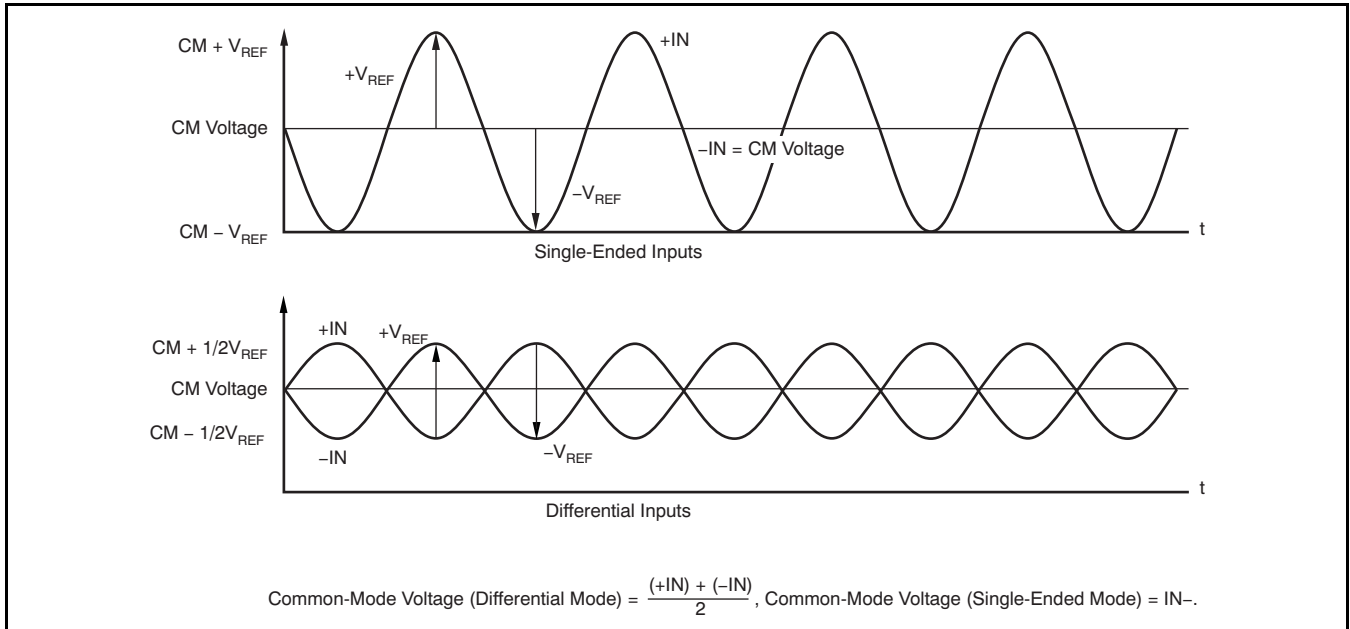
If the internal reference is used,  $\text{REF}_{\text{OUT}}$  (pin 32) should be directly connected to  $\text{REF}_{\text{IN}}$  (pin 31); see [Figure 15](#). The ADS8323 can operate, however, with an external reference in the range of 1.5V to 2.55V for a corresponding full-scale range of 3.0V to 5.1V. The internal reference of the ADS8323 is double-buffered. If the internal reference is used to drive an external load, a buffer is provided between the reference and the load applied to  $\text{REF}_{\text{OUT}}$  (pin 32) (the internal reference can typically source or sink 10 $\mu\text{A}$  of current; compensation capacitance should be at least 0.1 $\mu\text{F}$  to minimize noise). If an external reference is used, the second buffer provides isolation between the external reference and the CDAC. This buffer is also used to recharge all of the capacitors of the CDAC during conversion.

## ANALOG INPUT

The analog input is bipolar and fully differential. There are two general methods of driving the analog input of the ADS8323: single-ended or differential, as shown in [Figure 16](#) and [Figure 17](#). When the input is single-ended, the –IN input is held at the common-mode voltage. The +IN input swings around the same common voltage and the peak-to-peak amplitude is the (common-mode +  $V_{\text{REF}}$ ) and the (common-mode –  $V_{\text{REF}}$ ). The value of  $V_{\text{REF}}$  determines the range over which the common-mode voltage may vary (see [Figure 18](#)).

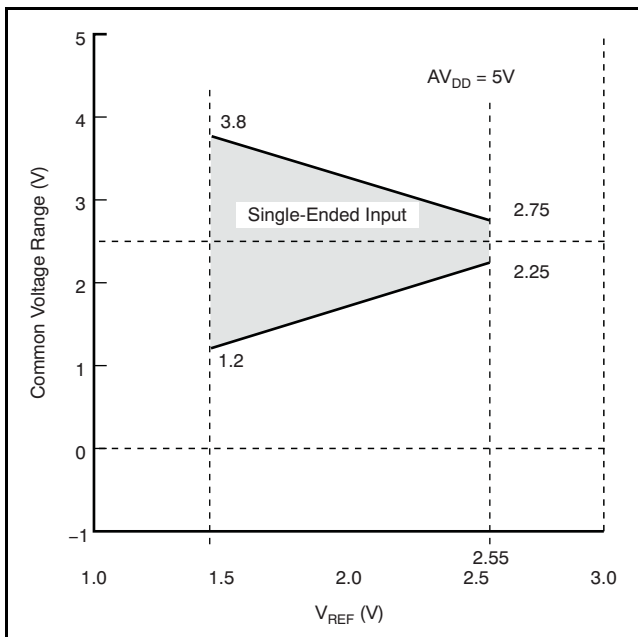


**Figure 16. Methods of Driving the ADS8323: Single-Ended or Differential**

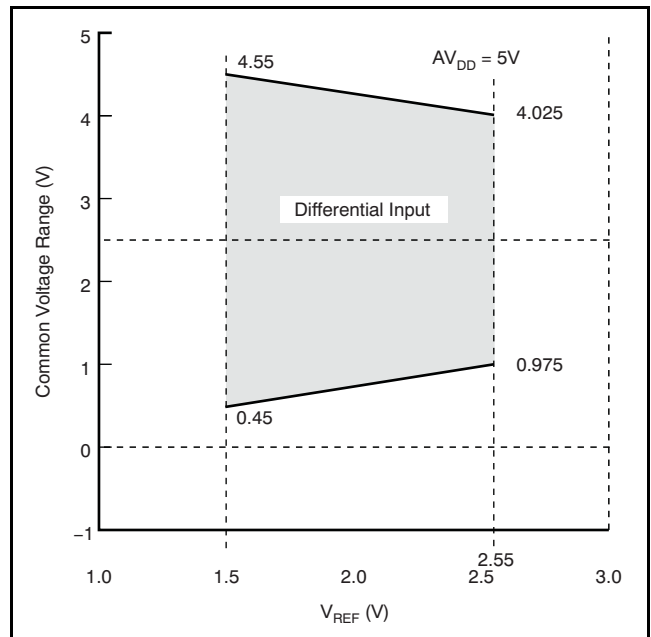


Note: The maximum differential voltage between +IN and -IN of the ADS8323 is  $V_{REF}$ . See Figure 18 and Figure 19 for a further explanation of the common voltage range for single-ended and differential inputs.

**Figure 17. Using the ADS8323 in the Single-Ended and Differential Input Modes**



**Figure 18. Single-Ended Input: Common-Mode Voltage Range vs  $V_{REF}$**



**Figure 19. Differential Input: Common-Mode Voltage Range vs  $V_{REF}$**

### NOISE

Figure 20 shows the transition noise of the ADS8323. A low-level dc input was applied to the analog-input pins and the converter was put through 8192 conversions. The digital output of the ADC varies in output code due to the internal noise of the ADS8323. This characteristic is true for all 16-bit SAR-type ADCs. The ADS8323, with five output codes for the  $\sigma$  distribution, yields a greater than  $\pm 0.8$ LSB transition noise at 5V operation. Remember that to achieve this low-noise performance, the peak-to-peak noise of the input signal and reference must be less than  $50\mu\text{V}$ .

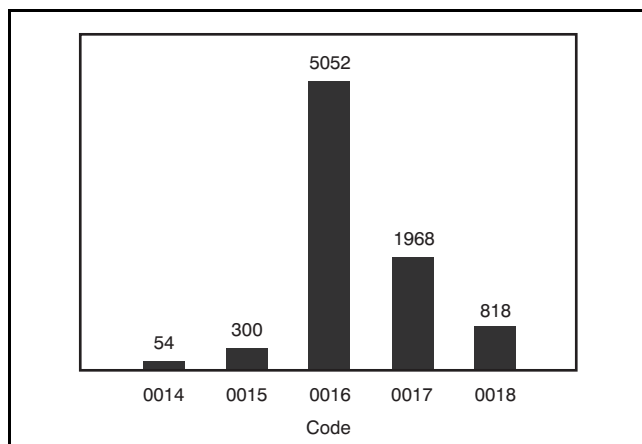


Figure 20. Histogram of 8,192 Conversions of a Low-Level DC Input

### AVERAGING

Averaging the digital codes can compensate the noise of the ADC. By averaging conversion results, transition noise is reduced by a factor of  $1/\sqrt{n}$ , where  $n$  is the number of averages. For example, averaging four conversion results reduces the transition noise by  $1/2$  to  $\pm 0.4$ LSB. Averaging should only be used for input signals with frequencies near dc. For ac signals, a digital filter can be used to low-pass filter and decimate the output codes. This process works in a similar manner to averaging—for every decimation by 2, the signal-to-noise ratio improves by 3dB.

### BIPOLAR INPUTS

The differential inputs of the ADS8323 were designed to accept bipolar inputs ( $-V_{REF}$  and  $+V_{REF}$ ) around the common-mode voltage, which corresponds to a 0V to 5V input range with a 2.5V reference. By using a simple op amp circuit featuring four high-precision external resistors, the ADS8323 can be configured to accept bipolar inputs. The conventional  $\pm 2.5\text{V}$ ,  $\pm 5\text{V}$ , and  $\pm 10\text{V}$  input ranges could be interfaced to the ADS8323 using the resistor values shown in Figure 21.

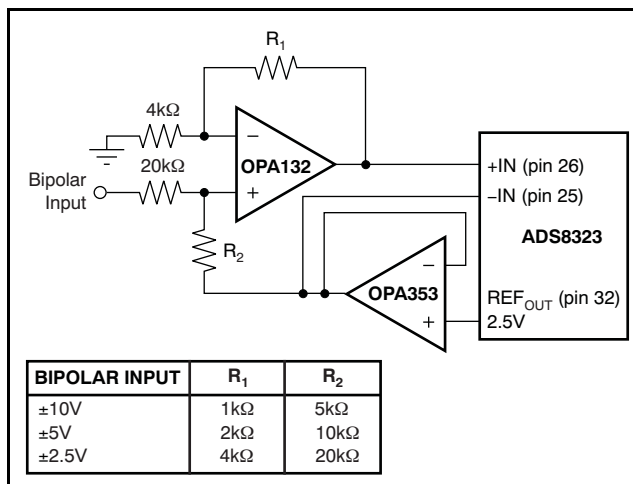


Figure 21. Level Shift Circuit for Bipolar Input Ranges

### DIGITAL INTERFACE

#### TIMING AND CONTROL

See the [timing diagram](#) and the [Timing Characteristics](#) section for detailed information on timing signals and the respective requirements for each.

The ADS8323 uses an external clock (CLOCK, pin 20) that controls the conversion rate of the CDAC. With a 10MHz external clock, the ADC sampling rate is 500kSPS that corresponds to a  $2\mu\text{s}$  maximum throughput time.

Conversions are initiated by bringing the  $\overline{\text{CONVST}}$  pin low for a minimum of 20ns (after the 20ns minimum requirement has been met, the  $\overline{\text{CONVST}}$  pin can be brought high), while  $\overline{\text{CS}}$  is low. The ADS8322 switches from Sample-to-Hold mode on the falling edge of the  $\overline{\text{CONVST}}$  command. Following the first rising edge of the external clock after a  $\overline{\text{CONVST}}$  low, the ADS8322 begins conversion (this first rising edge of the external clock represents the start of clock cycle one; the ADS8322 requires 16 rising clock edges to complete a conversion). The  $\overline{\text{BUSY}}$  output goes high immediately following  $\overline{\text{CONVST}}$  going low.  $\overline{\text{BUSY}}$  stays high through the conversion process and returns low when the conversion has ended.

Both  $\overline{\text{RD}}$  and  $\overline{\text{CS}}$  can be high during and before a conversion (although  $\overline{\text{CS}}$  must be low when  $\overline{\text{CONVST}}$  goes low to initiate a conversion). Both the  $\overline{\text{RD}}$  and  $\overline{\text{CS}}$  pins are brought low in order to enable the parallel output bus with the conversion.

## EXPLANATION OF CLOCK, BUSY AND BYTE PINS

**CLOCK:** An external clock must be provided for the ADS8323. The maximum clock frequency is 10MHz and that provides 500kSPS throughput. The minimum clock frequency is 25kHz and that provides 1.25kHz throughput. The minimum clock cycle is 100ns (see [Timing Diagram](#),  $t_{C1}$ ), and CLOCK must remain high (see [Timing Diagram](#),  $t_{W1}$ ) or low (see [Timing Diagram](#),  $t_{W2}$ ) for at least 40ns.

**BUSY:** Initially, BUSY output is low. Reading data from output register or sampling the input analog signal does not affect the state of the BUSY signal. After the  $\overline{\text{CONVST}}$  input goes low and conversion starts, a maximum of 25ns later the BUSY output goes high. That signal stays high during conversion and provides the status of the internal ADC to the DSP or  $\mu\text{C}$ . At the end of conversion, on the rising edge of the 17th clock cycle, new data from the internal ADC are latched into the output registers. The BUSY signal goes low a maximum of 25ns later (see [Timing Diagram](#),  $t_{D4}$ ).

**BYTE:** The output data appear as a full 16-bit word on DB15-DB0 (MSB-LSB or D15-D0) if BYTE is low. If there is only an 8-bit bus available on a board, the result may also be read on an 8-bit bus by using only DB7-DB0. In this case, two reads are necessary (see the [timing diagram](#)). The first, as before, leaving BYTE low and reading the eight least significant bits on DB7-DB0, then bringing BYTE high. When BYTE is high, the upper eight bits (D15-D8) appear on DB7-DB0.

## START OF A CONVERSION AND READING DATA

By bringing the  $\overline{\text{CONVST}}$  signal low, the input data are immediately placed in the hold mode (10ns), although  $\overline{\text{CS}}$  must be low when  $\overline{\text{CONVST}}$  goes low to initiate a conversion. The conversion follows with the next rising edge of CLOCK. If it is important to detect a hold command during a certain clock cycle, then the falling edge of the  $\overline{\text{CONVST}}$  signal must occur at least 10ns before the rising edge of CLOCK (see [Timing Diagram](#),  $t_{D1}$ ). The  $\overline{\text{CONVST}}$  signal can

remain low without initiating a new conversion. The  $\overline{\text{CONVST}}$  signal must be high for at least 20ns (see [Timing Diagram](#),  $t_{W4}$ ) before it is brought low again and  $\overline{\text{CONVST}}$  must stay low for at least 20ns (see [Timing Diagram](#),  $t_{W3}$ ). Once a  $\overline{\text{CONVST}}$  signal goes low, further impulses of this signal are ignored until the conversion is finished or the device is reset.

When the conversion is finished (after 16 clock cycles) the sampling switches close and sample the new value. The start of the next conversion must be delayed to allow the input capacitor of the ADS8323 to be fully charged. This delay time depends on the driving amplifier, but should be at least 400ns. To gain acquisition time, the falling edge of  $\overline{\text{CONVST}}$  must take place just before the rising edge of CLOCK (see [Timing Diagram](#),  $t_{D1}$ ). One conversion cycle requires 20 clock cycles. However, reading data during the conversion or on a falling hold edge may cause a loss in performance.

**Reading Data ( $\overline{\text{RD}}$ ,  $\overline{\text{CS}}$ ):** In general, the data outputs are in 3-state. Both  $\overline{\text{CS}}$  and  $\overline{\text{RD}}$  must be low to enable these outputs.  $\overline{\text{RD}}$  and  $\overline{\text{CS}}$  must stay low together for at least 40ns (see [Timing Diagram](#),  $t_{D7}$ ) before the output data is valid.  $\overline{\text{RD}}$  must remain high for at least 20ns (see [Timing Diagram](#),  $t_{W7}$ ) before bringing it back low for a subsequent read command. 16 clock-cycles after the start of a conversion (that is, the next rising edge of the clock after the falling edge of  $\overline{\text{CONVST}}$ ), the new data are latched into the output register and the reading process can start again. Refer to [Table 1](#) for ideal output codes.

$\overline{\text{CS}}$  being low tells the ADS8323 that the bus on the board is assigned to the ADS8323. If an ADC shares a bus with digital gates, there is a possibility that digital (high-frequency) noise could get coupled into the ADC. If the bus is just used by the ADS8323,  $\overline{\text{CS}}$  can be hard-wired to ground. The output data should not be read 125ns prior to the falling edge of  $\overline{\text{CONVST}}$  and 10ns after the falling edge.

The ADS8323 output is in binary twos complement format (see [Figure 22](#)).

**Table 1. Ideal Input Voltages and Output Codes**

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT BINARY TWOS COMPLEMENT	
		BINARY CODE	HEX CODE
Full-Scale Range	$2 \cdot V_{\text{REF}}$		
Least Significant Bit (LSB)	$2 \cdot V_{\text{REF}}/65535$		
+Full Scale	$+V_{\text{REF}} - 1 \text{ LSB}$	0111 1111 1111 1111	7FFF
Midscale	0V	0000 0000 0000 0000	0000
Midscale – 1 LSB	$0V - 1 \text{ LSB}$	1111 1111 1111 1111	FFFF
Zero	$-V_{\text{REF}}$	1000 0000 0000 0000	8000

## LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8323 circuitry. This consideration is particularly true if the CLOCK input is approaching the maximum throughput rate.

As the ADS8323 offers single-supply operation, it is often used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to achieve good performance from the converter.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections and digital inputs that occur just before latching the output of the analog comparator. Thus, during any single conversion for an n-bit SAR converter, there are n *windows* in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, or nearby digital logic or high-power devices.

The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. These errors can change if the external event changes in time with respect to the CLOCK input.

On average, the ADS8323 draws very little current from an external reference, as the reference voltage is internally buffered. If the reference voltage is external and originates from an op amp, make sure that it can drive the bypass capacitor or capacitors without oscillation. A 0.1 $\mu$ F bypass capacitor is recommended from pin 31 directly to ground.

The AGND and DGND pins should be connected to a clean ground point. In all cases, this point should be the *analog* ground. Avoid connections which are too close to the grounding point of a microcontroller or digital signal processor. If required, run a ground trace directly from the converter to the power supply entry point. The ideal layout includes an analog ground plane dedicated to the converter and associated analog circuitry.

As with the GND connections,  $V_{DD}$  should be connected to a +5V power supply plane, or trace, that is separate from the connection for digital logic until they are connected at the power entry point. Power to the ADS8323 should be clean and well-bypassed. A 0.1 $\mu$ F ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1 $\mu$ F to 10 $\mu$ F capacitor is recommended. If needed, an even larger capacitor and a 5 $\Omega$  or 10 $\Omega$  series resistor may be used to low-pass filter a noisy supply. In some situations, additional bypassing may be required, such as a 100 $\mu$ F electrolytic capacitor, or even a *Pi* filter made up of inductors and capacitors all designed to essentially low-pass filter the +5V supply, removing the high-frequency noise.



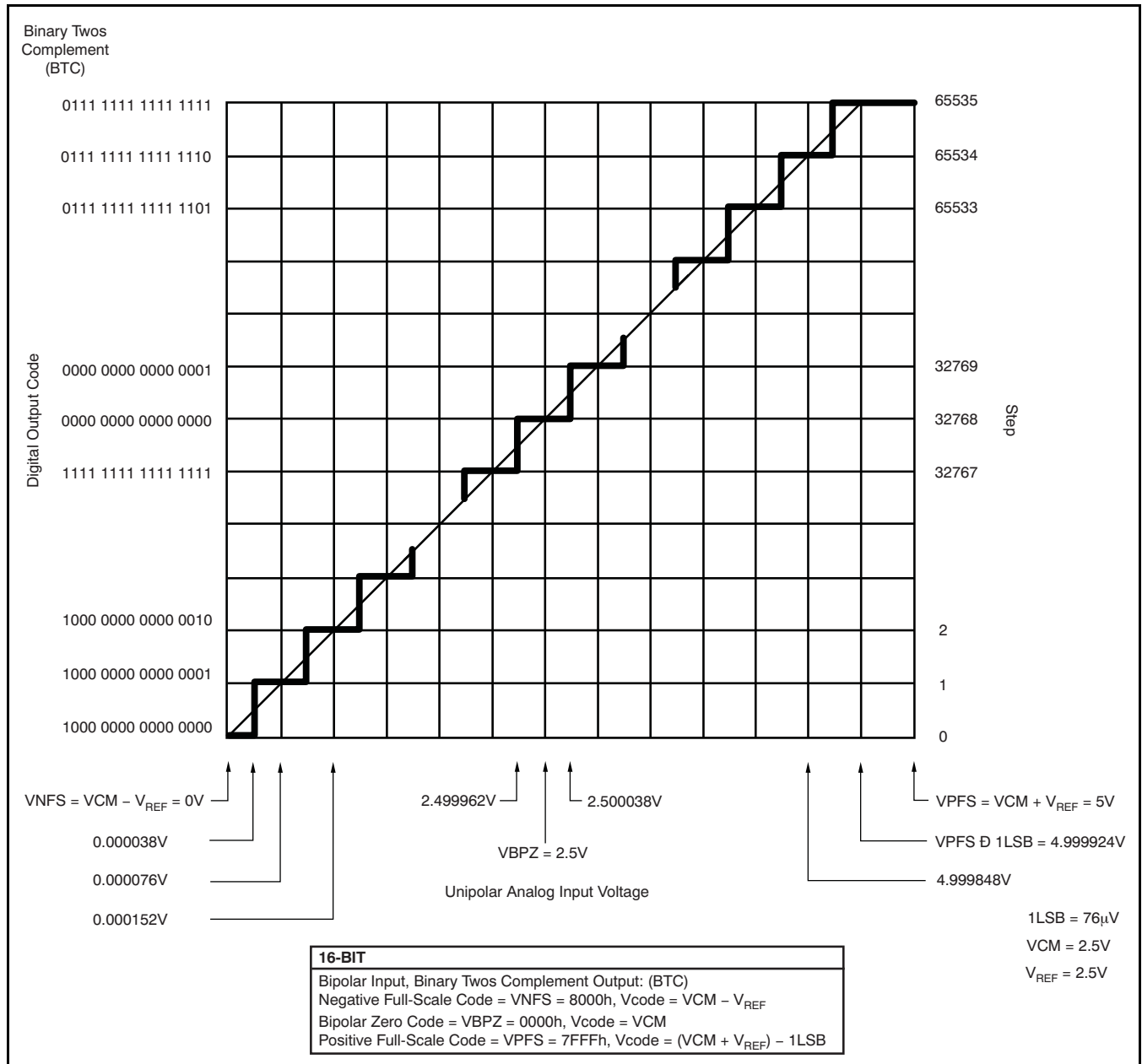


Figure 22. Ideal Conversion Characteristics (Condition: Single-Ended,  $V_{CM} = IN- = 2.5V$ ,  $V_{REF} = 2.5V$ )

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Original (May, 2002) to Revision C</b>	<b>Page</b>
• Updated document format to current standards .....	1
• Deleted <i>lead temperature</i> specifications from Absolute Maximum Ratings table .....	2
• Changed conversion time from 1.6μs (min) to 1.6μs (max) .....	3
• Changed acquisition time specification from .4μs (max) to 350ns (min) .....	3
• Changed acquisition time specification from .4μs (max) to 350ns (min) .....	7

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
ADS8323Y/250	ACTIVE	TQFP	PBS	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS8323Y/250G4	ACTIVE	TQFP	PBS	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS8323Y/2K	ACTIVE	TQFP	PBS	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS8323Y/2KG4	ACTIVE	TQFP	PBS	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS8323YB/250	ACTIVE	TQFP	PBS	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS8323YB/250G4	ACTIVE	TQFP	PBS	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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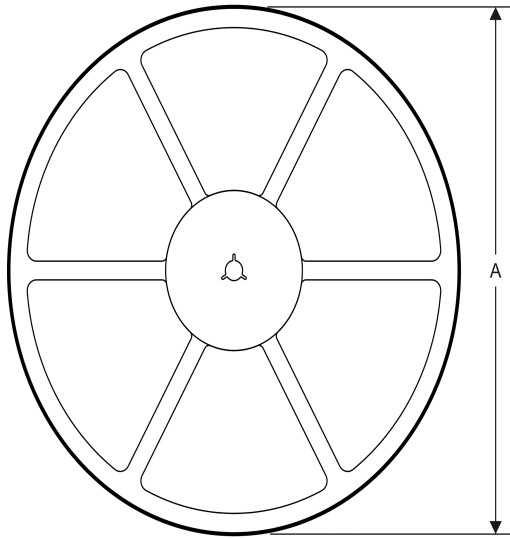
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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8323Y/250	TQFP	PBS	32	250	330.0	16.4	7.2	7.2	1.5	12.0	16.0	Q2
ADS8323Y/2K	TQFP	PBS	32	2000	330.0	16.4	7.2	7.2	1.5	12.0	16.0	Q2
ADS8323YB/250	TQFP	PBS	32	250	330.0	16.4	7.2	7.2	1.5	12.0	16.0	Q2

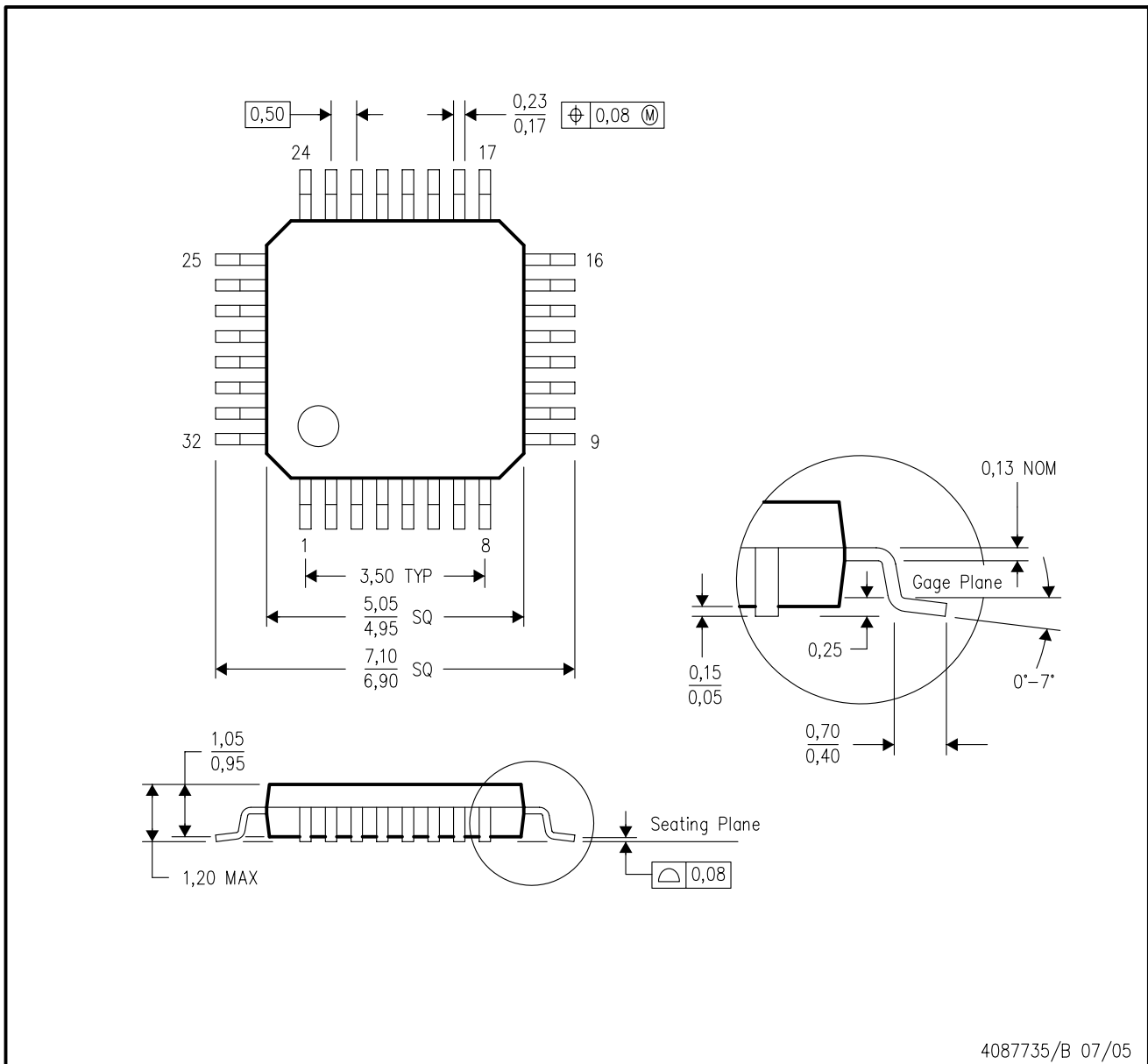
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8323Y/250	TQFP	PBS	32	250	367.0	367.0	38.0
ADS8323Y/2K	TQFP	PBS	32	2000	367.0	367.0	38.0
ADS8323YB/250	TQFP	PBS	32	250	367.0	367.0	38.0

PBS (S-PQFP-G32)

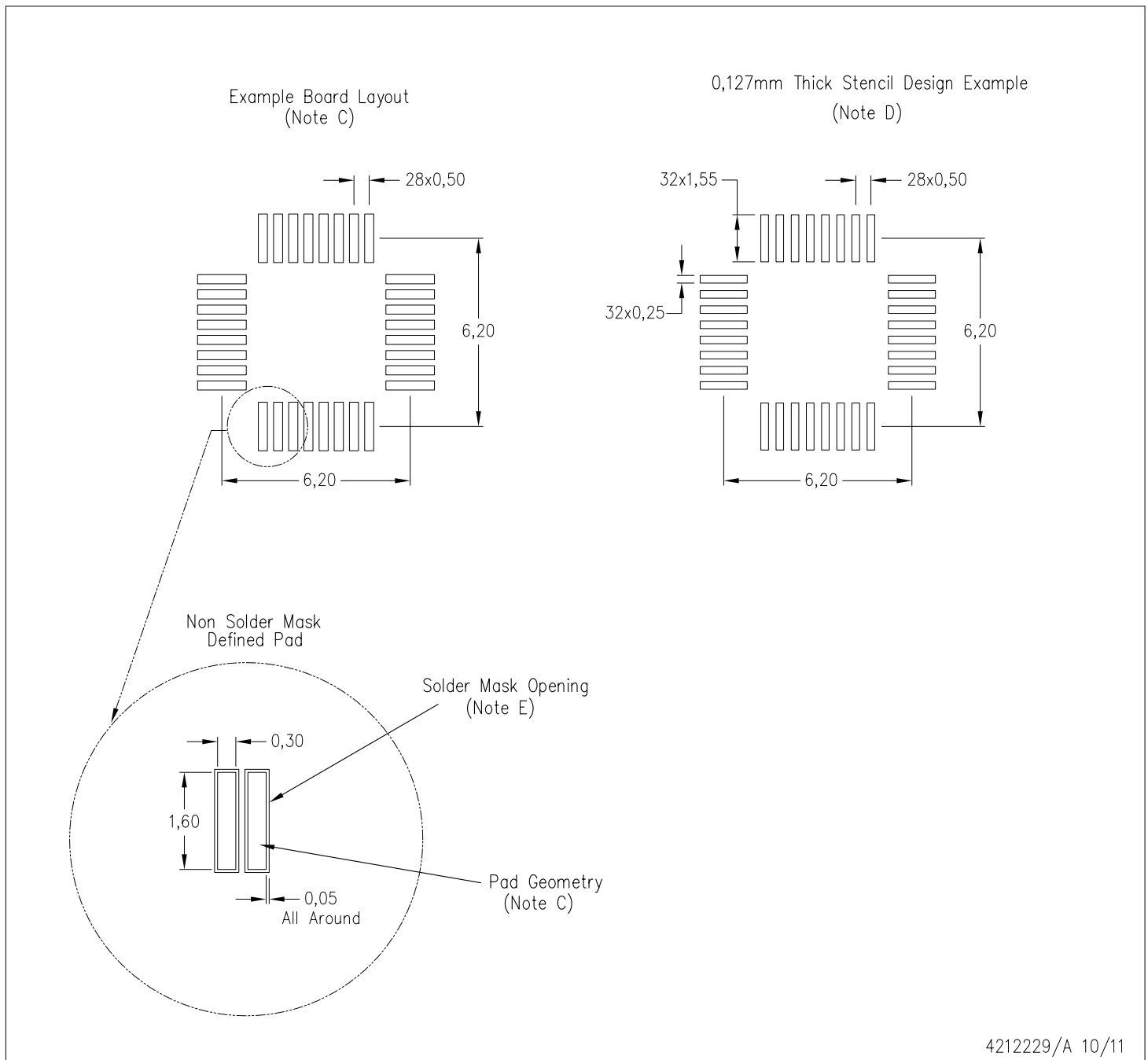
PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.

PBS (S-PQFP-G32)

PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
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