# 2.7V to 5.5V, 12-Bit, Octal DIGITAL-TO-ANALOG CONVERTER in a Wafer Chip-Scale Package—Pb-Free/Green

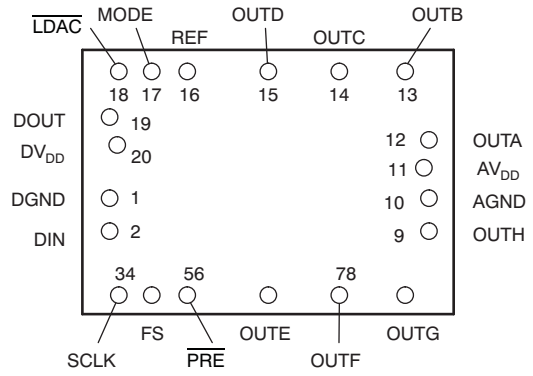
## FEATURES

- **Eight, 12-Bit, Voltage Output DACs in One Package**
- **Pin-Compatible, Pb-Free, RoHS-Compliant Upgrade to the TLV5610IYE**
- **Programmable Settling Time versus Power Consumption:**
  - **– 1μs in Fast Mode**
  - **– 3μs in Slow Mode**
- **Compatible With TMS320™ DSP Family and SPI™ Serial Ports**
- **Differential and Single-Ended Analog Input/Output**
- **Separate Software Control for ADC and DAC Power Down**
- **Monotonic Over Temperature**
- **Low Power Consumption:**
  - **– 18mW in Slow Mode at 3V**
  - **– 48mW in Fast Mode at 3V**
- **Power Down Mode**
- **Buffered, High-Impedance Reference Inputs**
- **Data Output for Daisy-Chaining**

## APPLICATIONS

- **Digital Servo-Control Loops**
- **Digital Offset and Gain Adjustment**
- **Industrial Process Control**
- **Machine and Motion Control Devices**
- **Mass Storage Devices**

**WAFER CHIP-SCALE PACKAGE**
**(BOTTOM VIEW)**




## DESCRIPTION

The TLV5610IYZ is the lead-free version of the TLV5610IYE, an eight-channel, 12-bit, voltage output digital-to-analog converter (DAC) with a flexible serial interface. The serial interface allows glueless interface to TMS320 and SPI, QSPI™, and Microwire™ serial ports. It is programmed with a 16-bit serial string containing four control and 12 data bits.

Additional features include a power-down mode, an $\overline{\text{LDAC}}$ input for simultaneous update of all eight DAC outputs, and a data output that can be used to cascade multiple devices.

The resistor string output voltage is buffered by a rail-to-rail output amplifier with a programmable settling time to allow the designer to optimize speed versus power dissipation. The buffered, high-impedance reference input can be connected to the supply voltage.

The TLV5610IYZ is implemented in a CMOS process and is available in a 20-terminal wafer chip-scale package (WCSP). The TLV5610IYZ is characterized for operation from –40°C to +85°C in a wire-bonded small outline (SO) package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION

| $T_A$ | WCSP-20 PACKAGE(1) |
|---|---|
| –40°C to +85°C | TLV5610IYZ |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)(1)

| | TLV5610IYZ | UNIT |
|---|---|---|
| Supply voltage ($AV_{DD}$, $DV_{DD}$ to GND) | 7 | V |
| Reference input voltage range | – 0.3 to $AV_{DD}$ + 0.3 | V |
| Digital input voltage range | – 0.3 to $DV_{DD}$ + 0.3 | V |
| Operating free-air temperature range, $T_A$ | –40 to +85 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

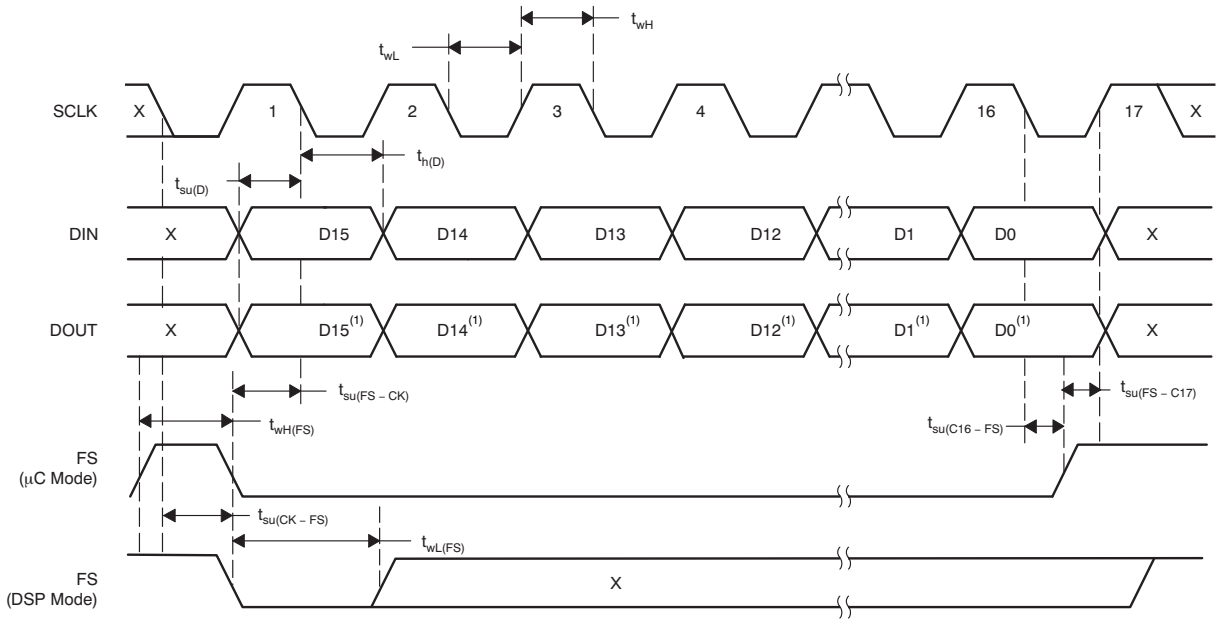
| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $AV_{DD}$, $DV_{DD}$ | 5V operation | 4.5 | 5 | 5.5 | V |
| | 3V operation | 2.7 | 3 | 3.3 | V |
| High-level digital input, $V_{IH}$ | $DV_{DD}$ = 2.7V to 5.5V | 2 | | | V |
| Low-level digital input, $V_{IL}$ | $DV_{DD}$ = 2.7V to 5.5V | | | 0..8 | V |
| Reference voltage, $V_{REF}$ | $AV_{DD}$ = 5V | GND | 4.096 | $AV_{DD}$ | V |
| | $AV_{DD}$ = 3V | GND | 2.048 | $AV_{DD}$ | V |
| Load resistance. $R_L$ | | 2 | | | kΩ |
| Load capacitance, $C_L$ | | | | 100 | pF |
| Clock frequency, $f_{CLK}$ | | | | 30 | MHz |
| Operating free-air temperature, $T_A$ | | –40 | | +85 | °C |

## ELECTRICAL CHARACTERISTICS

Over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | | |
| $I_{DD}$ | Power-supply current | Fast | No load, $V_{REF}$ = 4.096V, all inputs = $DV_{DD}$ or GND | | 16 | 21 | mA |
| | | Slow | | | 6 | 8 | mA |
| | Power-down supply current | | | | 0.1 | | µA |
| POR | Power-on threshold | | | | 2 | | V |
| PSRR | Power-supply rejection ratio | | Full-scale; see Note (1) | | –60 | | dB |
| **Static DAC Specifications** | | | | | | | |
| | Resolution | | | | 12 | | Bits |
| INL | Integral nonlinearity | | Code 40 to 4095, $V_{REF}$ = 2V, 4V | | ±2 | ±6 | LSB |
| DNL | Differential nonlinearity | | Code 40 to 4095, $V_{REF}$ = 2V, 4V | | ±0.5 | ±1 | LSB |
| $E_{ZS}$ | Zero-scale error (offset error at zero-scale) | | | | | ±30 | mV |
| $E_{ZS}$ TC | Zero-scale error temperature coefficient | | | | 30 | | µV/°C |
| $E_G$ | Gain error | | | | | ±0.6 | % Full-Scale V |
| $E_G$ TC | Gain error temperature coefficient | | | | 10 | | ppm/°C |
| **Output Specifications** | | | | | | | |
| $V_O$ | Voltage output range | | $R_L$ = 10kΩ | 0 | | $AV_{DD}$ – 4 | V |
| | Output load regulation accuracy | | $R_L$ = 2kΩ vs 10kΩ | | | ±0.3 | % Full-Scale V |
| **Reference Input** | | | | | | | |
| $V_I$ | Input voltage range | | | 0 | | $AV_{DD}$ | V |
| $R_I$ | Input resistance | | | | 100 | | kΩ |
| $C_I$ | Input capacitance | | | | 5 | | pF |
| | Reference input bandwidth | Fast | $V_{REF}$ = 0.4$V_{PP}$ + 2.048$V_{DC}$, input code = 0x800 | | 2.2 | | MHz |
| | | Slow | | | 1.9 | | MHz |
| | Reference feedthrough | | $V_{REF}$ = 2$V_{PP}$ at 1kHz + 2.048$V_{DC}$ (2) | | –84 | | dB |
| **Digital Inputs** | | | | | | | |
| $I_{IH}$ | High-level digital input current | | $V_I = DV_{DD}$ | | | 1 | µA |
| $I_{IL}$ | Low-level digital input current | | $V_I$ = 0V | –1 | | | µA |
| $C_I$ | Input capacitance | | | | 8 | | pF |
| **Digital Outputs** | | | | | | | |
| $V_{OH}$ | High-level digital output voltage | | $R_L$ = 10kΩ | 2.6 | | | V |
| $V_{OL}$ | Low-level digital output voltage | | $R_L$ = 10kΩ | | | 0.4 | V |
| | Output voltage rise time | | $R_L$ = 10kΩ, $C_L$ = 20pF, incl. propagation delay | | 7 | 20 | ns |
| **Analog Output Dynamic Performance** | | | | | | | |
| $t_S$(FS) | Output settling time (3), full-scale | Fast | $R_L$ = 10kΩ, $C_L$ = 1000pF | | 1 | 3 | µs |
| | | Slow | | | 3 | 7 | µs |
| $t_S$(CC) | Output settling time (4), code to code | Fast | $R_L$ = 10kΩ, $C_L$ = 1000pF | | 0.5 | 1 | µs |
| | | Slow | | | 1 | 2 | µs |
| SR | Slew rate (5) | Fast | $R_L$ = 10kΩ, $C_L$ = 1000pF | 4 | 10 | | V/µs |
| | | Slow | | 1 | 3 | | V/µs |
| | Glitch energy | | See Note (6) | | 4 | | nV-s |
| | Channel crosstalk | | 10kHz sine, 4$V_{PP}$ | | –90 | | dB |

(1) Power-supply rejection ratio at full-scale is measured by varying $AV_{DD}$ and is given by the following equation: PSRR = 20 log[(EG($AV_{DD}$max) – EG($AV_{DD}$min))]/$V_{DD}$max.
(2) Reference feedthrough is measured at the DAC output with an input code = 0x000.
(3) Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 0x80 to 0xFFF and 0xFFF to 0x080, respectively. Assured by design; not production tested.
(4) Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of one count. The max time applies to code changes near zero scale or full-scale. Assured by design; not production tested.
(5) Slew rate determines the time it takes for a change of the DAC output from 10% to 90% full-scale voltage.
(6) Code transition: 0x7FF to 0x800.




NOTE: (1) Previous input data.

**Figure 1. Serial Interface Timing**

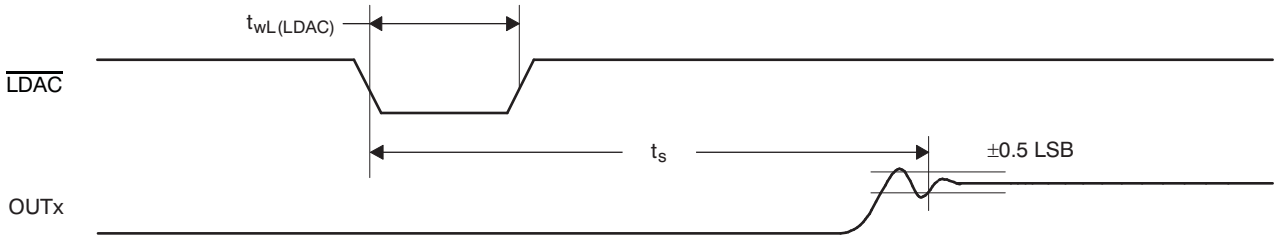
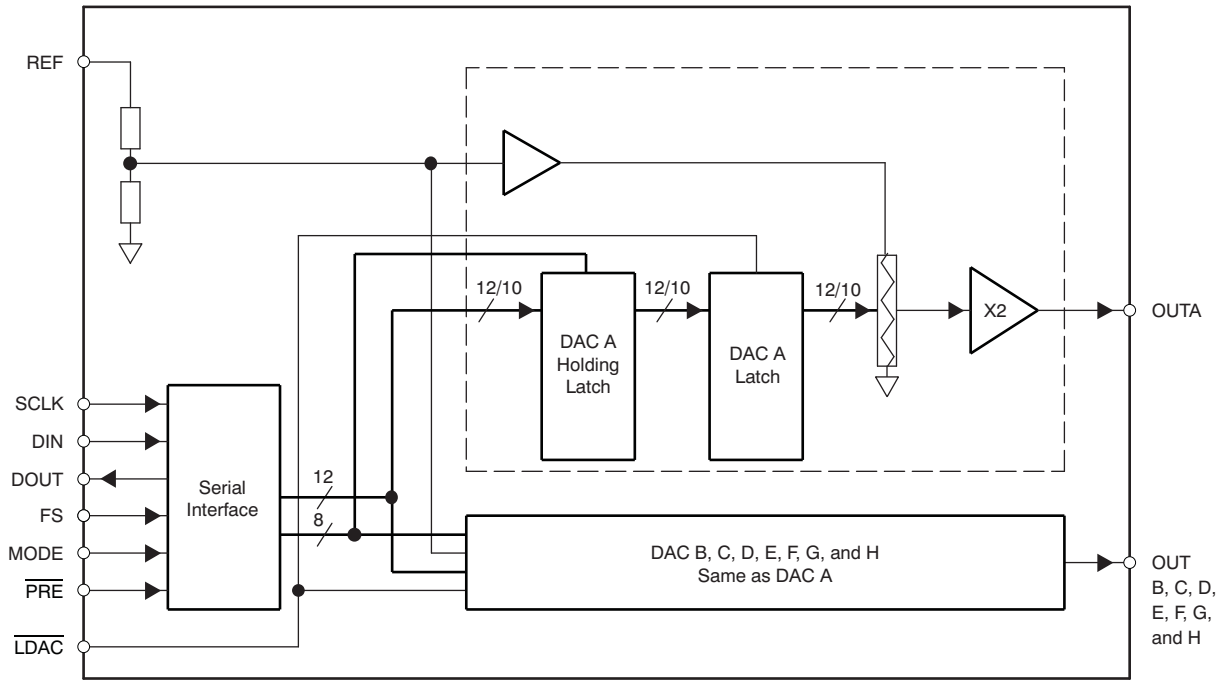



**Figure 2. Output Timing**

## DIGITAL INPUT TIMING REQUIREMENTS

| | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{su(FS-CK)}$ | Setup time, FS low before next negative SCLK edge | 8 | | | ns |
| $t_{su(C16-FS)}$ | Setup time, 16th negative edge after FS low on which bit D0 is sampled before rising edge of FS. µC mode only | 10 | | | ns |
| $t_{su(FS-C17)}$ | µC mode, setup time, FS high before 17th positive SCLK. | 10 | | | ns |
| $t_{su(CK-FS)}$ | DSP mode, setup time, SLCK low before FS low. | 5 | | | ns |
| $t_{wL(LDAC)}$ | $\overline{LDAC}$ duration low | 10 | | | ns |
| $t_{wH}$ | SCLK pulse duration high | 16 | | | ns |
| $t_{wL}$ | SCLK pulse duration low | 16 | | | ns |
| $t_{su(D)}$ | Setup time, data ready before SCLK falling edge | 8 | | | ns |
| $t_{h(D)}$ | Hold time, data held valid after SCLK falling edge | 5 | | | ns |
| $t_{wH(FS)}$ | FS duration high | 10 | | | ns |
| $t_{wL(FS)}$ | FS duration low | 10 | | | ns |
| $t_s$ | Settling time | See Analog Output Dynamic Performance | | | |

## Functional Block Diagram




## Terminal Functions

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| AGND | 10 | P | Analog ground |
| $AV_{DD}$ | 11 | P | Analog power supply |
| DGND | 1 | P | Digital ground |
| DIN | 2 | I | Digital serial data input |
| DOUT | 19 | O | Digital serial data output |
| $DV_{DD}$ | 20 | P | Digital power supply |
| FS | 4 | I | Frame sync input |
| $\overline{LDAC}$ | 18 | I | Load DAC. The DAC outputs are only updated if this signal is low. It is an asynchronous input. |
| MODE | 17 | I | DSP/µC mode pin. High = µC mode; NC = DSP mode. |
| $\overline{PRE}$ | 5 | I | Preset input |
| REF | 16 | I | Voltage reference input |
| SCLK | 3 | I | Serial clock input |
| OUTA–OUTH | 12–15, 6–9 | O | DAC outputs A, B, C, D, E, F, G and H |

## TYPICAL CHARACTERISTICS

**OUTPUT LOAD REGULATION**

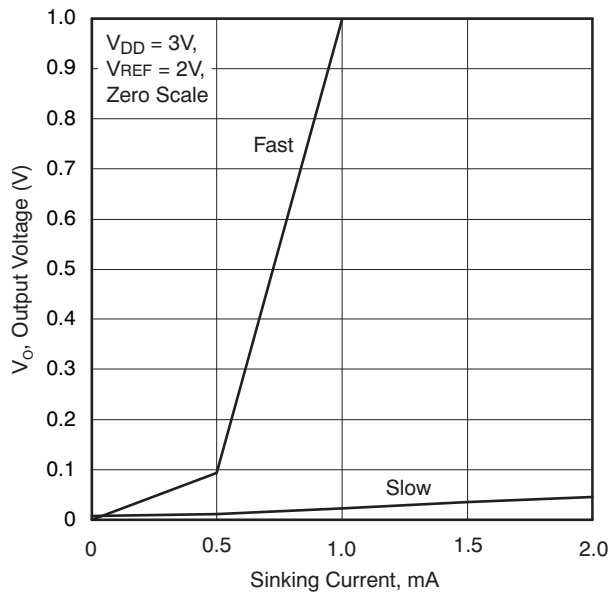



**Figure 3.**

**OUTPUT LOAD REGULATION**

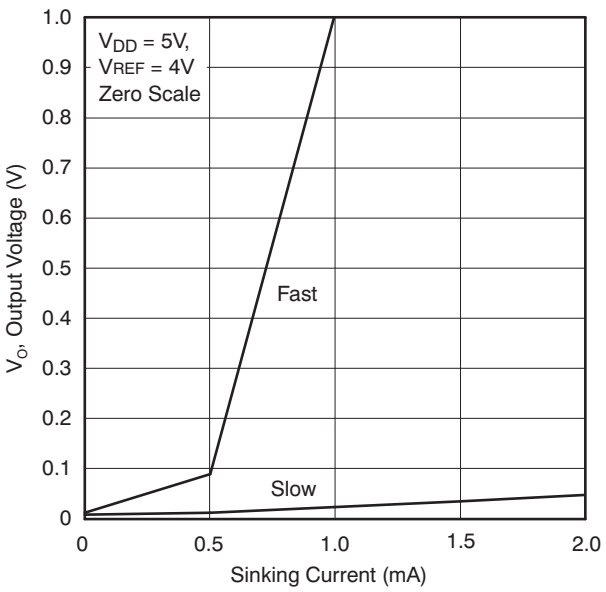



**Figure 4.**

**OUTPUT LOAD REGULATION**

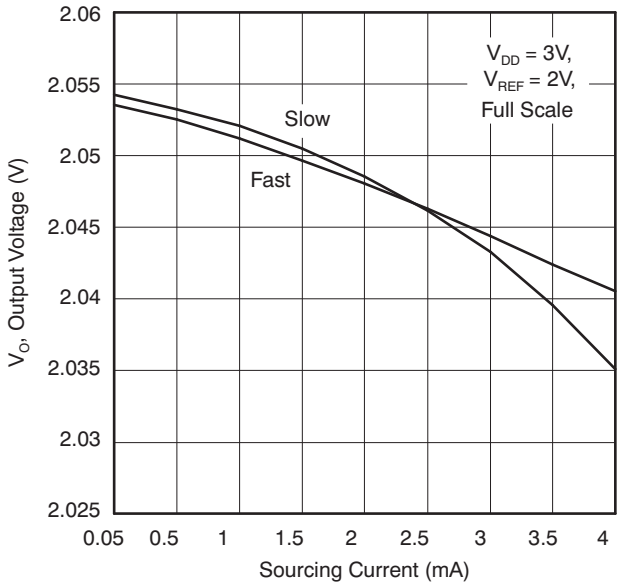



**Figure 5.**

**OUTPUT LOAD REGULATION**

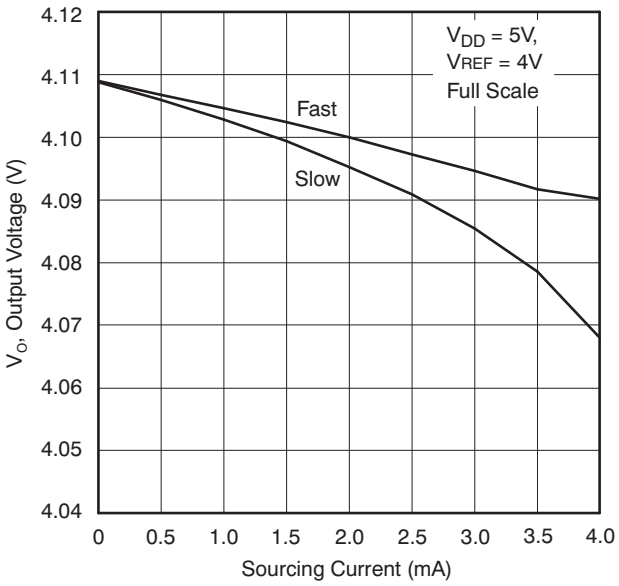



**Figure 6.**

## TYPICAL CHARACTERISTICS (continued)

**INTEGRAL NONLINEARITY vs CODE**

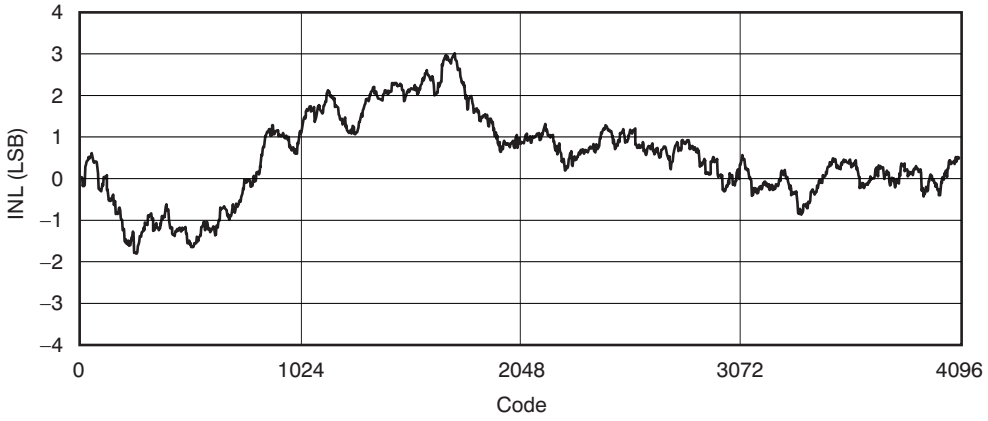



**Figure 7.**

**DIFFERENTIAL NONLINEARITY vs CODE**

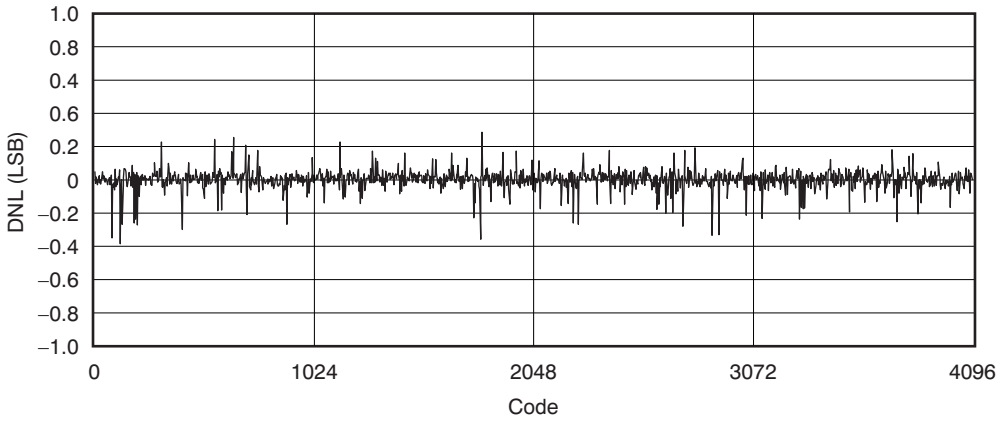



**Figure 8.**

# APPLICATION INFORMATION

## GENERAL FUNCTION

The TLV5610IYZ is an eight-channel, 12-bit, single-supply DAC, based on a resistor string architecture. The TLV5610IYZ, a green/PB-free device, is pin-compatible with the TLV5610IYE. The TLV5610IYZ consists of a serial interface, a speed and power-down control logic, a reference input buffer, a resistor string, and a rail-to-rail output buffer.

The output voltage (full-scale determined by external reference) for each channel is given by:

$$REF \frac{CODE}{0x1000}[V] \quad (1)$$

Where:

REF is the reference voltage.

CODE is the digital input value.

The input range is 0x000 to 0xFFF.

A power on reset initially puts the internal latches to a defined state (all bits zero).

## SERIAL INTERFACE

A falling edge of FS starts shifting the data on DIN, starting with the MSB to the internal register on the falling edges of SCLK. After 16 bits have been transferred, the content of the shift register is moved to one of the DAC holding registers, depending on the address bits within the data word. A logic '0' on the $\overline{LDAC}$ pin is required to transfer the content of the DAC holding register to the DAC latch and to update the DAC outputs. $\overline{LDAC}$ is an asynchronous input; it can be held low if a simultaneous update of all eight channels is not needed.

For daisy-chaining, DOUT provides the data sampled on DIN with a delay of 16 clock cycles.

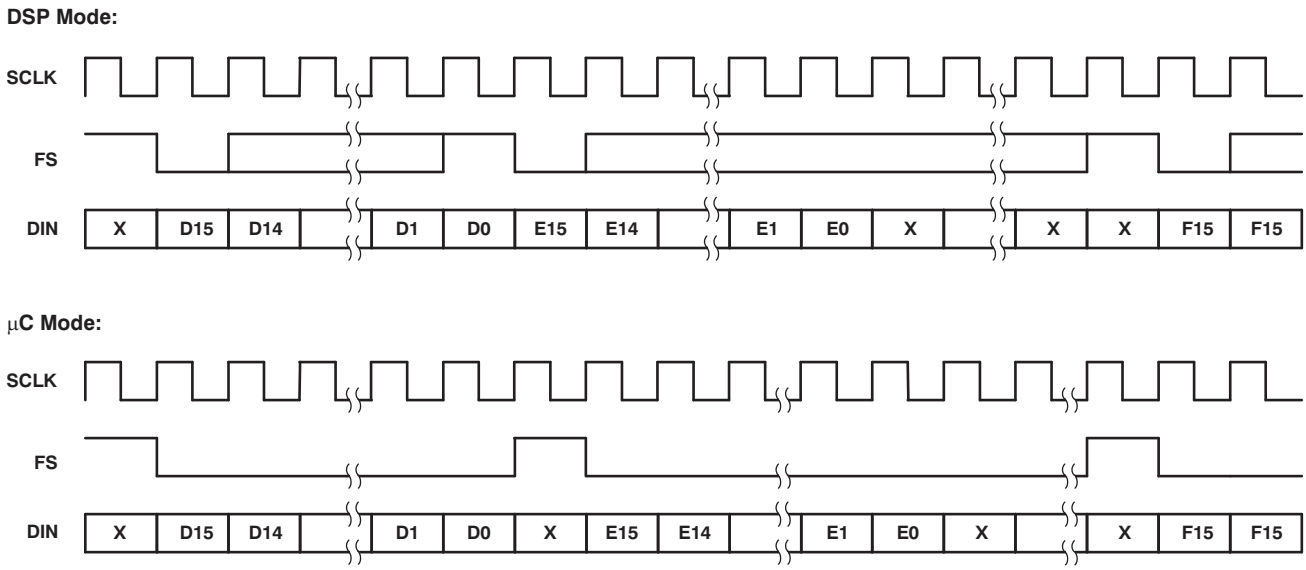



**Figure 9. Timing Diagrams**

The differences between DSP mode (MODE = NC or 0) and µC (MODE = 1) mode:

- In µC mode, FS must be held low until all 16 data bits have been transferred. If FS is driven high before the 16th falling clock edge, the data transfer is cancelled. The DAC is updated after a rising edge on FS.
- In DSP mode, FS must only stay low for 20ns and can go high before the 16th falling clock edge.

## APPLICATION INFORMATION (continued)

### SERIAL CLOCK FREQUENCY AND UPDATE RATE

The maximum serial clock frequency is given by:

$$f_{sclkmax} = \frac{1}{t_{whmin} + t_{wlmin}} = 30MHz \quad (2)$$

The maximum update rate is given by:

$$f_{updatemax} = \frac{1}{16\left(t_{whmin} + t_{wlmin}\right)} = 1.95MHz \quad (3)$$

Note that the maximum update rate is just a theoretical value for the serial interface because the settling time of the DAC must also be considered.

### DATA FORMAT

The 16 bit data word consists of two parts:

1. Address bits (D15...D12)
2. Data bits (D11...D0)

**Table 1. Data Format(1)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A3 | A2 | A1 | A0 | Data | | | | | | | | | | | |

(1) Ax: Address bits. See Table 2.

### REGISTER MAP

**Table 2. Register Map**

| A3 | A2 | A1 | A0 | FUNCTION |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | DAC A |
| 0 | 0 | 0 | 1 | DAC B |
| 0 | 0 | 1 | 0 | DAC C |
| 0 | 0 | 1 | 1 | DAC D |
| 0 | 1 | 0 | 0 | DAC E |
| 0 | 1 | 0 | 1 | DAC F |
| 0 | 1 | 1 | 0 | DAC G |
| 0 | 1 | 1 | 1 | DAC H |
| 1 | 0 | 0 | 0 | CTRL0 |
| 1 | 0 | 0 | 1 | CTRL1 |
| 1 | 0 | 1 | 0 | Preset |
| 1 | 0 | 1 | 1 | Reserved |
| 1 | 1 | 0 | 0 | DAC A and $\overline{B}$ |
| 1 | 1 | 0 | 1 | DAC C and $\overline{D}$ |
| 1 | 1 | 1 | 0 | DAC E and $\overline{F}$ |
| 1 | 1 | 1 | 1 | DAC G and $\overline{H}$ |

## DAC A-H AND TWO-CHANNEL REGISTERS

Writing to DAC A–H sets the output voltage of channel A–H. It is possible to automatically generate the complement of one channel by writing to one of the four, two-channel registers (DAC A and $\overline{B}$, etc.).

The TLV5610IYZ decodes all 12 data bits.

## PRESET

The outputs of all DAC channels can be driven to a predefined value stored in the preset register by driving the $\overline{PRE}$ input low. The $\overline{PRE}$ input is asynchronous to the clock.

## CTRL0

**Table 3. CTRL0 Bit Register**

| D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | PD | DO | X | X | IM |

**Bit Definitions:**

**PD** Full Device Power Down.
0 = Normal
1 = Power Down

**DO** Digital Output Enable.
0 = Disable
1 = Enable

**IM** Input Mode.
0 = Straight Binary
1 = Twos Complement

**X** Reserved.

If DOUT is enabled, the data input on DIN is output on DOUT with a 16-cycle delay. This feature makes it possible to daisy-chain multiple DACs on one serial bus.

## CTRL1

**Table 4. CTRL1 Bit Register**

| D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | PD | DO | X | X | IM |

**Bit Definitions:**

**$P_{XY}$** Power Down $DAC_{XY}$. In power-down mode, the amplifiers of the selected DAC pair within the device are disabled and the total power consumption of the device is significantly reduced. Power-down mode of a specific DAC pair can be selected by setting the $P_{XY}$ bit within the data word to '1'.
0 = Normal
1 = Power Down

**$S_{XY}$** $DAC_{XY}$ Speed Mode. There are two settling time modes: fast and slow. Fast mode of a DAC pair is selected by setting $S_{XY}$ to '1', and slow mode is selected by setting $S_{XY}$ to '0'.
0 = Slow
1 = Fast

**NOTE:** *XY* refers to DAC pair AB, CD, EF, or GH.

## USING THE TLV5610IYZ WAFER CHIP-SCALE PACKAGE (WCSP)

TLV5610 qualifications are done using a wire-bonded small outline (SO) package. The qualifications include: steady state life, thermal shock, ESD, latch-up, biased HAST, autoclave, and characterization. These qualified devices are orderable as TLV5610IDW.

**NOTE:** The wafer chip-scale package (WCSP) for the TLV5610IYZ uses the same ***die*** as TLV5610IDW, but is not qualified. WCSP qualification, including board level reliability (BLR), is the responsibility of the customer.

It is recommended that underfill be used for increased reliability. BLR is application-dependent, but may include tests such as: temperature cycling, drop test, key push, bend, vibration, and package shear.

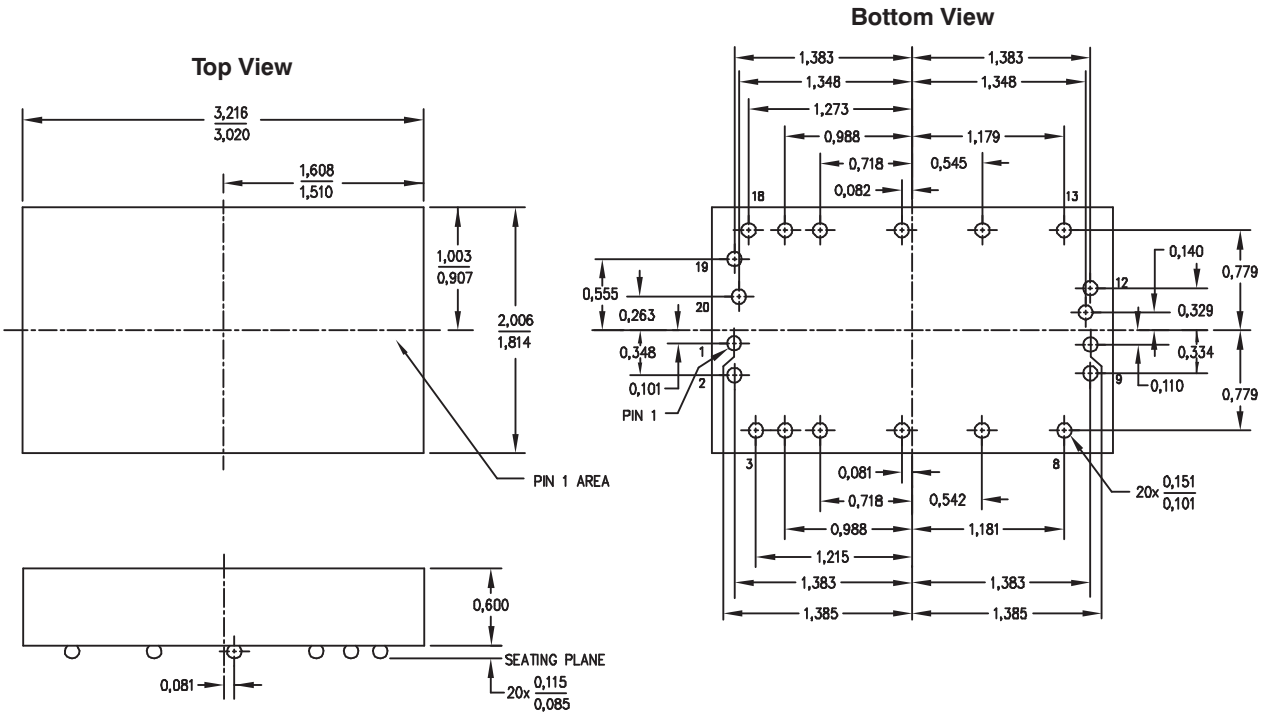
For general guidelines on board assembly of the WCSP, the following documentation provides more details:

- Application Report NanoStar™ & NanoFree™ 300µm Solder Bump WCSP Application—SBVA017
- Design Summary WCSP Little Logic—SCET007B

**NOTE:** The use of underfill is **required** and greatly reduces the risk of thermal mismatch fails.

Underfill is an epoxy/adhesive that may be added during the board assembly process to improve board level/system level reliability. The process is to dispense the epoxy under the dice after die attach reflow. The epoxy adheres to the body of the device and to the printed-circuit board. It reduces stress placed upon the solder joints because of thermal coefficient of expansion (TCE) mismatch between the board and the component. Underfill material is highly filled with silica or other fillers to increase epoxy modulus, reduce creep sensitivity, and decrease material TCE.

**NOTE:** The recommendation for peak flow temperatures of +250°C to +260°C is based on general empirical results that indicate that this temperature range is needed to facilitate good wetting of the solder bump to the substrate or circuit board pad. Lower peak temperatures may cause nonwets (cold solder joints).




A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

**Figure 10. TLV5610IYZ Wafer Chip-Scale Package**

## Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Original (July 2006) to A Revision | Page |
|---|---|
| • Deleted separate INL and DNL specifications for Code 20 to 1023; not relevant to this device | 3 |
| • Replaced timing diagram | 4 |
| • Updated Digital Input Timing Requirements Table | 4 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| TLV5610IYZR | ACTIVE | DSBGA | YZ | 20 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-NC-NC-UNLIM | |
| TLV5610IYZT | ACTIVE | DSBGA | YZ | 20 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-NC-NC-UNLIM | |

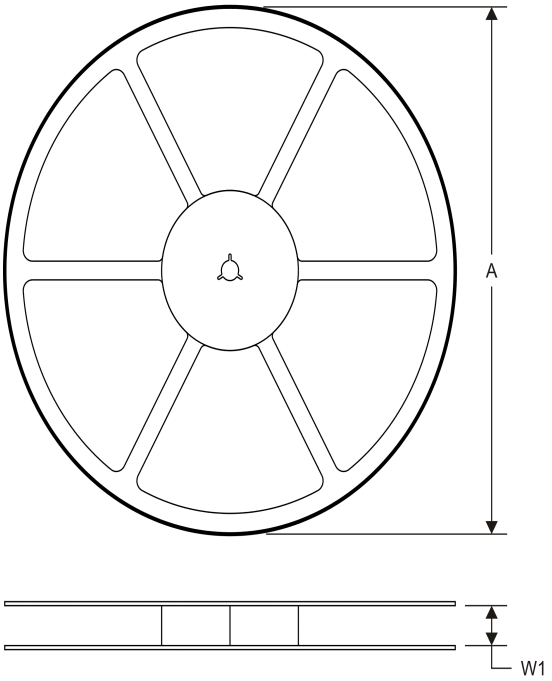
(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

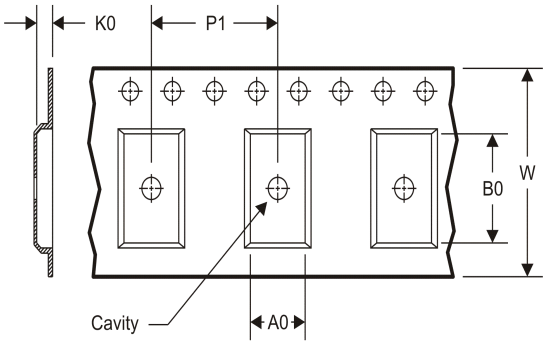
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**




**TAPE DIMENSIONS**



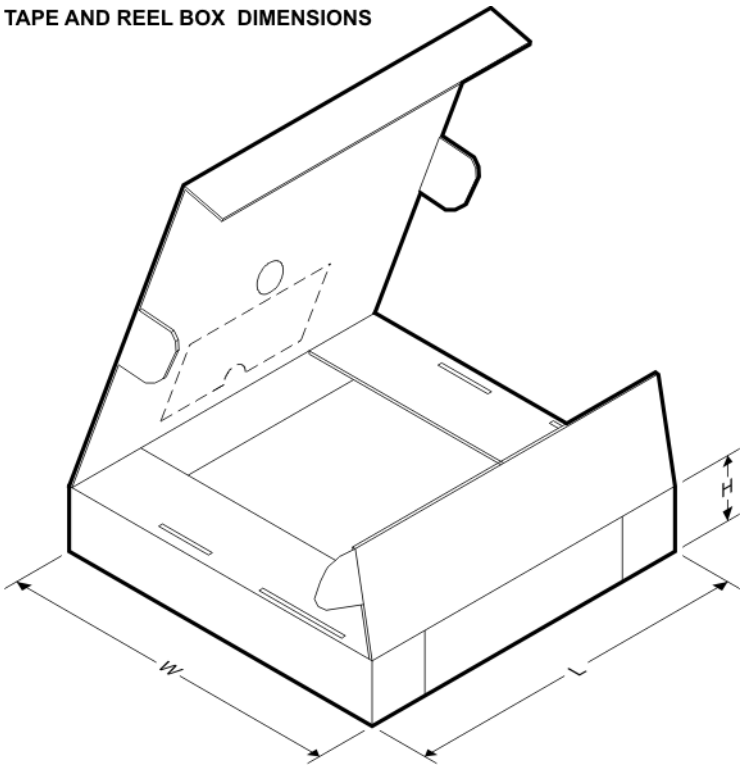

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV5610IYZR | DSBGA | YZ | 20 | 3000 | 180.0 | 8.4 | 2.18 | 3.18 | 1.0 | 4.0 | 8.0 | Q2 |
| TLV5610IYZT | DSBGA | YZ | 20 | 250 | 180.0 | 8.4 | 2.18 | 3.18 | 1.0 | 4.0 | 8.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV5610IYZR | DSBGA | YZ | 20 | 3000 | 220.0 | 220.0 | 34.0 |
| TLV5610IYZT | DSBGA | YZ | 20 | 250 | 220.0 | 220.0 | 34.0 |

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