

## Fully Differential Isolation Amplifier

Check for Samples: [AMC1200-Q1](#)

### FEATURES

- **AEC-Q100 Qualified With the Following Results:**
  - **Device Temperature Grade 2: –40°C to 105°C Ambient Operating Temperature Range**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C3B**
- **±250-mV Input Voltage Range Optimized for Shunt Resistors**
- **Very Low Nonlinearity: 0.075% Max. at 5 V**
- **Low Offset Error: 1.5 mV Max.**
- **Low Noise: 3.1 mV<sub>RMS</sub> Typ.**
- **Low High-Side Supply Current: 8 mA Max. at 5 V**
- **Input Bandwidth: 60 kHz Min.**
- **Fixed Gain: 8 (0.5% Accuracy)**
- **High Common-Mode Rejection Ratio: 108 dB**
- **3.3-V Operation on Low-Side**
- **Certified Galvanic Isolation:**
  - **UL1577 and IEC60747-5-2 Approved**
  - **Isolation Voltage: 4000 V<sub>PEAK</sub>**
  - **Working Voltage: 1200 V<sub>PEAK</sub>**
  - **Transient Immunity: 10 kV/μs Min.**
- **Typical 10-Year Lifespan at Rated Working Voltage (see Application Report [SLLA197](#))**
- **Fully Specified Over the Extended Industrial Temperature Range**

### APPLICATIONS

- **Shunt Resistor Based Current Sensing in:**
  - **Motor Control**
  - **Green Energy**
  - **Frequency Inverters**
  - **Uninterruptible Power Supplies**

### DESCRIPTION

The AMC1200-Q1 is a precision isolation amplifier with an output separated from the input circuitry by a silicon dioxide (SiO<sub>2</sub>) barrier that is highly resistant to magnetic interference. This barrier has been certified to provide galvanic isolation of up to 4000 V<sub>PEAK</sub> according to UL1577 and IEC60747-5-2. Used in conjunction with isolated power supplies, this device prevents noise currents on a high common-mode voltage line from entering the local ground and interfering with or damaging sensitive circuitry.

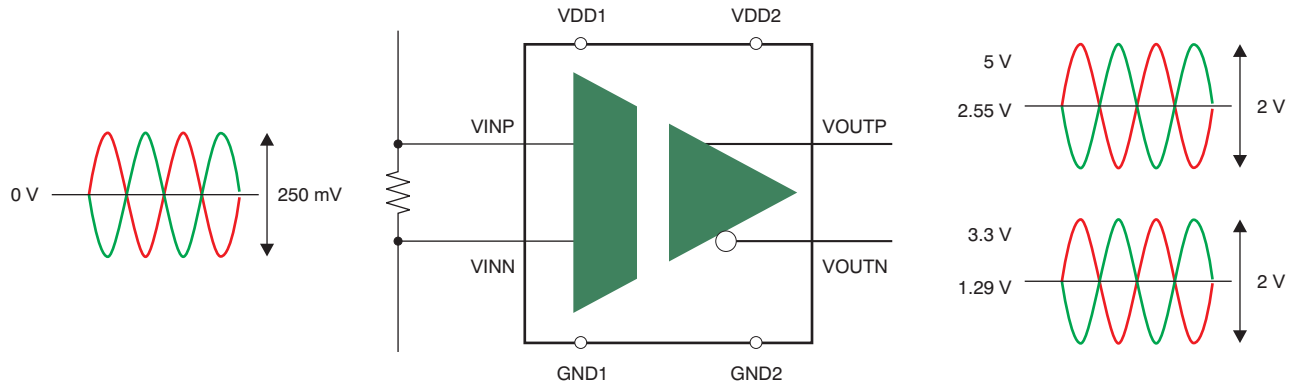
The input of the AMC1200-Q1 is optimized for direct connection to shunt resistors or other low-voltage-level signal sources. The excellent performance of the device supports accurate current control, resulting in system-level power saving and, especially in motor-control applications, lower torque ripple. The common-mode voltage of the output signal is automatically adjusted to either the 3-V or 5-V low-side supply.

The AMC1200-Q1 is fully specified over the extended industrial temperature range of –40 °C to 105 °C and is available in the SMD-type, gullwing-8 package.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on [www.ti.com](http://www.ti.com).

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over the operating ambient temperature range, unless otherwise noted.

		AMC1200-Q1	UNIT
Supply voltage, VDD1 to GND1 or VDD2 to GND2		-0.5 to 6	V
Analog input voltage at VINP, VINN		GND1 – 0.5 to VDD1 + 0.5	V
Input current to any pin except supply pins		±10	mA
Maximum junction temperature, T <sub>J</sub> Max		150	°C
Electrostatic rating	Human-body model (HBM) AEC-Q100 Classification Level H2	2.5	kV
	Charged-device model (CDM) AEC-Q100 Classification Level C3B	1000	V

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		AMC1200-Q1	UNIT
		DUB (SOP)	
		8 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance	75.1	°C/W
$\theta_{JCTop}$	Junction-to-case (top) thermal resistance	61.6	°C/W
$\theta_{JB}$	Junction-to-board thermal resistance	39.8	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	27.2	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	39.4	°C/W
$\theta_{JCbott}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## REGULATORY INFORMATION

VDE/IEC	UL
Certified according to IEC 60747-5-2	Recognized under 1577 component recognition program
File number: 40016131	File number: E181974

## IEC 60747-5-2 INSULATION CHARACTERISTICS

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	VALUE	UNIT
$V_{IORM}$	Maximum working insulation voltage		1200	$V_{PEAK}$
$V_{PR}$	Input to output test voltage	Qualification test: after Input/Output Safety Test Subgroup 2/3 $V_{PR} = V_{IORM} \times 1.2$ , $t = 10$ s, partial discharge $< 5$ pC	1140	$V_{PEAK}$
		Qualification test: method a, after environmental tests subgroup 1, $V_{PR} = V_{IORM} \times 1.6$ , $t = 10$ s, partial discharge $< 5$ pC	1920	$V_{PEAK}$
		100% production test: method b1, $V_{PR} = V_{IORM} \times 1.875$ , $t = 1$ s, partial discharge $< 5$ pC	2250	$V_{PEAK}$
$V_{IOTM}$	Transient overvoltage	Qualification test: $t = 60$ s	4000	$V_{PEAK}$
$V_{ISO}$	Insulation voltage per UL	Qualification test: $V_{TEST} = V_{ISO}$ , $t = 60$ s	4000	$V_{PEAK}$
		100% production test: $V_{TEST} = 1.2 \times V_{ISO}$ , $t = 1$ s	4800	$V_{PEAK}$
$R_S$	Insulation resistance	$V_{IO} = 500$ V at $T_S$	$> 10^9$	$\Omega$
PD	Pollution degree		2	°

## IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output (I/O) circuitry. A failure of the I/O circuitry can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

The safety-limiting constraint is the operating virtual junction temperature range specified in the [Absolute Maximum Ratings](#) table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determine the junction temperature. The assumed junction-to-air thermal resistance in the [Thermal Information](#) table is that of a device installed in the JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages* and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_S$	Safety input, output, or supply current	$\theta_{JA} = 246^\circ\text{C}/\text{W}$ , $V_{IN} = 5.5$ V, $T_J = 150^\circ\text{C}$ , $T_A = 25^\circ\text{C}$			10	mA
$T_C$	Maximum case temperature				150	$^\circ\text{C}$

## IEC 61000-4-5 RATINGS

PARAMETER		TEST CONDITIONS	VALUE	UNIT
$V_{IOSM}$	Surge immunity	1.2- $\mu\text{s}/50$ - $\mu\text{s}$ voltage surge and 8- $\mu\text{s}/20$ - $\mu\text{s}$ current surge	$\pm 6000$	V

## IEC 60664-1 RATINGS

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage $\leq 150$ $V_{RMS}$	I-IV
	Rated mains voltage $\leq 300$ $V_{RMS}$	I-IV
	Rated mains voltage $\leq 400$ $V_{RMS}$	I-III
	Rated mains voltage $< 600$ $V_{RMS}$	I-III

**PACKAGE CHARACTERISTICS<sup>(1)</sup>**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (clearance)	Shortest terminal-to-terminal distance through air	7			mm
L(I02)	Minimum external tracking (creepage)	Shortest terminal-to-terminal distance across the package surface	7			mm
CTI	Tracking resistance (comparative tracking index)	DIN IEC 60112/VDE 0303 part 1	≥ 175			V
	Minimum internal gap (internal clearance)	Distance through the insulation	0.014			mm
R <sub>IO</sub>	Isolation resistance	Input to output, V <sub>IO</sub> = 500 V, all pins on each side of the barrier tied together to create a two-terminal device, T <sub>A</sub> < 85°C		> 10 <sup>12</sup>		Ω
		Input to output, V <sub>IO</sub> = 500 V, 85°C ≤ T <sub>A</sub> < T <sub>A</sub> max		> 10 <sup>11</sup>		Ω
C <sub>IO</sub>	Barrier capacitance input to output	V <sub>I</sub> = 0.5 V <sub>PP</sub> at 1 MHz		1.2		pF
C <sub>I</sub>	Input capacitance to ground	V <sub>I</sub> = 0.5 V <sub>PP</sub> at 1 MHz		3		pF

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of a specific application. Care should be taken to maintain the creepage and clearance distance of the board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal according to the measurement techniques shown in the [Isolation Glossary](#) section. Techniques such as inserting grooves and/or ribs on the PCB are used to help increase these specifications.

**ELECTRICAL CHARACTERISTICS**

All minimum/maximum specifications at T<sub>A</sub> = –40°C to 105°C and within the specified voltage range, unless otherwise noted. Typical values are at T<sub>A</sub> = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V.

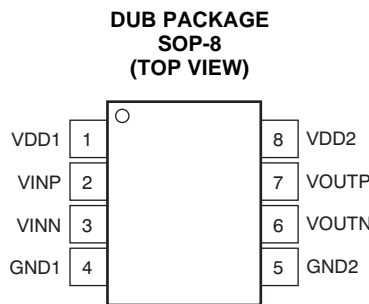
PARAMETER	TEST CONDITIONS	AMC1200-Q1			UNIT	
		MIN	TYP	MAX		
<b>INPUT</b>						
	Maximum input voltage before clipping	V <sub>INP</sub> – V <sub>INN</sub>		±320	mV	
	Differential input voltage	V <sub>INP</sub> – V <sub>INN</sub>	–250	250	mV	
V <sub>CM</sub>	Common-mode operating range		–0.16	VDD1	V	
V <sub>OS</sub>	Input offset voltage		–1.5	±0.2	1.5	mV
TCV <sub>OS</sub>	Input offset thermal drift		–10	±1.5	10	μV/K
CMRR	Common-mode rejection ratio	V <sub>IN</sub> from 0 V to 5 V at 0 Hz		108		dB
		V <sub>IN</sub> from 0 V to 5 V at 50 kHz		95		
C <sub>IN</sub>	Input capacitance to GND1	V <sub>INP</sub> or V <sub>INN</sub>		3		pF
C <sub>IND</sub>	Differential input capacitance			3.6		pF
R <sub>IN</sub>	Differential input resistance			28		kΩ
	Small-signal bandwidth		60	100		kHz
<b>OUTPUT</b>						
	Nominal gain			8		
G <sub>ERR</sub>	Gain error	Initial, at T <sub>A</sub> = 25°C	–0.5%	±0.05%	0.5%	
			–1%	±0.05%	1%	
TCG <sub>ERR</sub>	Gain error thermal drift			±56		ppm/K
	Nonlinearity	4.5 V ≤ VDD2 ≤ 5.5 V	–0.075%	±0.015%	0.075%	
		2.7 V ≤ VDD2 ≤ 3.6 V	–0.1%	±0.023%	0.1%	
	Nonlinearity thermal drift			2.4		ppm/K
	Output noise	V <sub>INP</sub> = V <sub>INN</sub> = 0 V		3.1		mV <sub>RMS</sub>
PSRR	Power-supply rejection ratio	vs VDD1, 10-kHz ripple		80		dB
		vs VDD2, 10-kHz ripple		61		
	Rise/fall time	0.5-V step, 10% to 90%		3.66	6.6	μs

### ELECTRICAL CHARACTERISTICS (continued)

All minimum/maximum specifications at  $T_A = -40^{\circ}\text{C}$  to  $105^{\circ}\text{C}$  and within the specified voltage range, unless otherwise noted. Typical values are at  $T_A = 25^{\circ}\text{C}$ ,  $V_{DD1} = 5\text{ V}$ , and  $V_{DD2} = 3.3\text{ V}$ .

PARAMETER	TEST CONDITIONS	AMC1200-Q1			UNIT
		MIN	TYP	MAX	
$V_{IN}$ to $V_{OUT}$ signal delay	0.5-V step, 50% to 10%, unfiltered output		1.6	3.3	$\mu\text{s}$
	0.5-V step, 50% to 50%, unfiltered output		3.15	5.6	
	0.5-V step, 50% to 90%, unfiltered output		5.26	9.9	
CMTI Common-mode transient immunity	$V_{CM} = 1\text{ kV}$ ( $T_A$ at $25^{\circ}\text{C}$ )	8	15		$\text{kV}/\mu\text{s}$
Output common-mode voltage	$2.7\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$	1.15	1.29	1.45	V
	$4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$	2.4	2.55	2.7	
Short-circuit current			20		mA
$R_{OUT}$ Output resistance			2.5		$\Omega$
<b>POWER SUPPLY</b>					
$V_{DD1}$ High-side supply voltage		4.5	5	5.5	V
$V_{DD2}$ Low-side supply voltage		2.7	5	5.5	V
$I_{DD1}$ High-side supply current			5.4	8	mA
$I_{DD2}$ Low-side supply current	$2.7\text{ V} < V_{DD2} < 3.6\text{ V}$		3.8	6	mA
	$4.5\text{ V} < V_{DD2} < 5.5\text{ V}$		4.4	7	
$P_{DD1}$ High-side power dissipation			27	44	mW
$P_{DD2}$ Low-side power dissipation	$2.7\text{ V} < V_{DD2} < 3.6\text{ V}$		11.4	21.6	mW
	$4.5\text{ V} < V_{DD2} < 5.5\text{ V}$		22	38.5	

### PIN CONFIGURATION



### PIN DESCRIPTIONS

PIN #	PIN NAME	FUNCTION	DESCRIPTION
1	VDD1	Power	High-side power supply
2	VINP	Analog input	Noninverting analog input
3	VINN	Analog input	Inverting analog input
4	GND1	Power	High-side analog ground
5	GND2	Power	Low-side analog ground
6	VOUTN	Analog output	Inverting analog output
7	VOUTP	Analog output	Noninverting analog output
8	VDD2	Power	Low-side power supply

**TYPICAL CHARACTERISTICS**

At VDD1 = VDD2 = 5 V, VINP = -250 mV to 250 mV, and VINN = 0 V, unless otherwise noted.

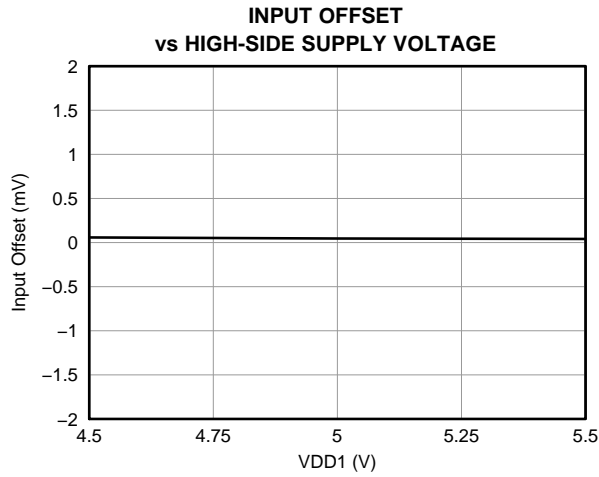


Figure 1.

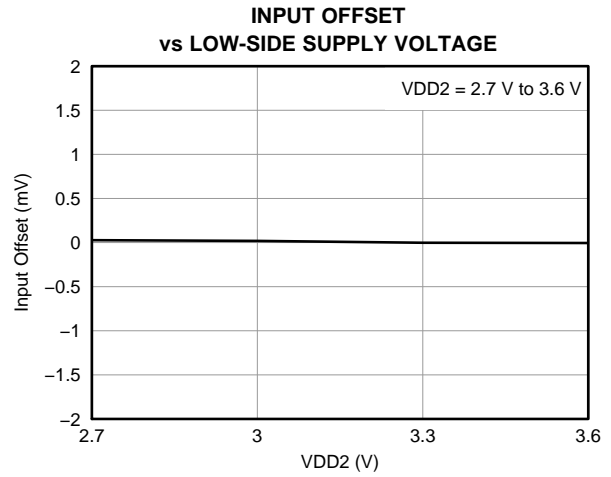


Figure 2.

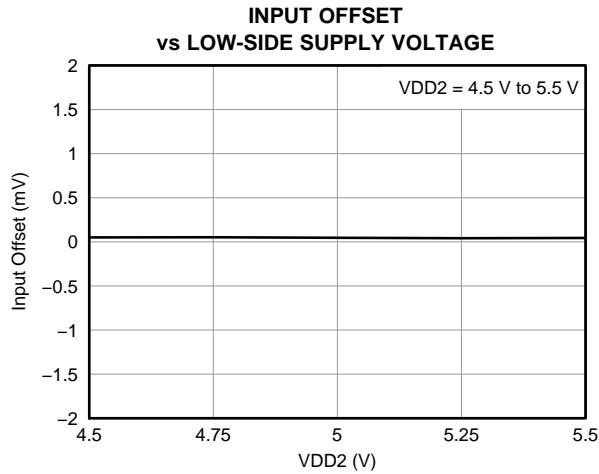


Figure 3.

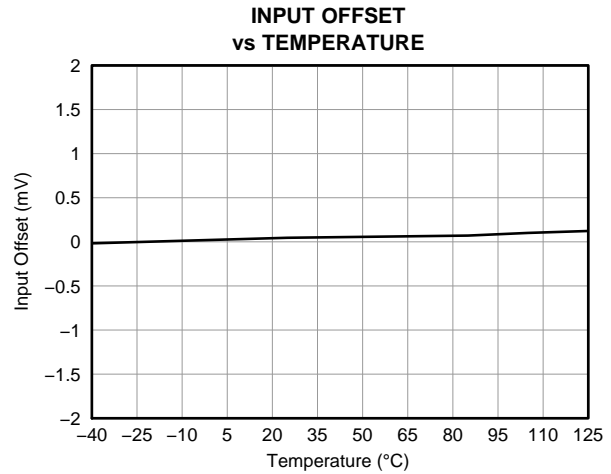


Figure 4.

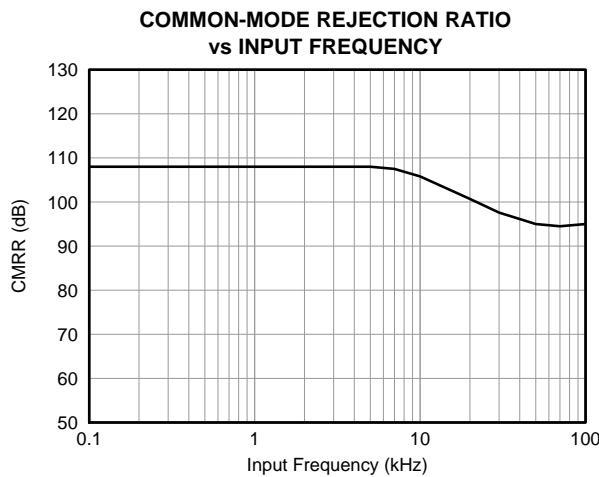


Figure 5.

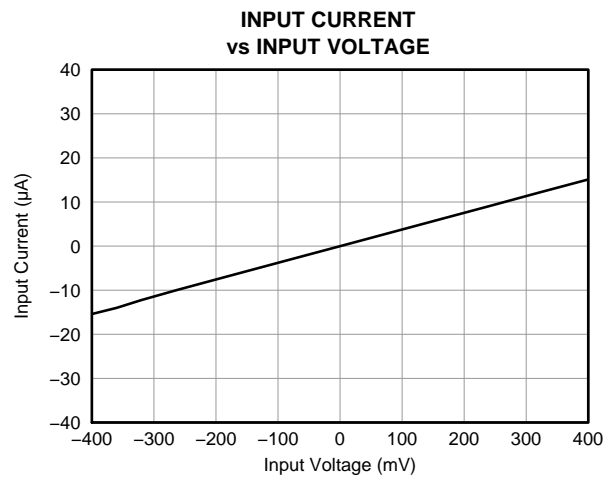


Figure 6.

**TYPICAL CHARACTERISTICS (continued)**

At VDD1 = VDD2 = 5 V, VINP = -250 mV to 250 mV, and VINN = 0 V, unless otherwise noted.

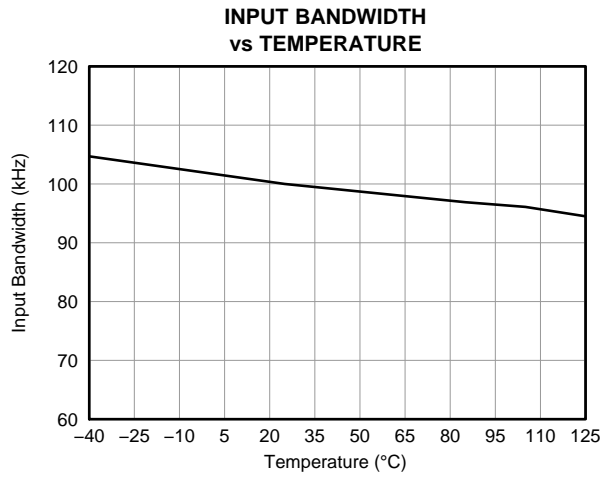


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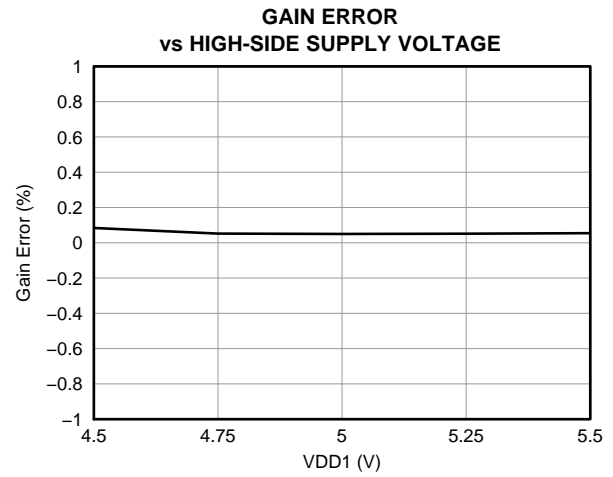


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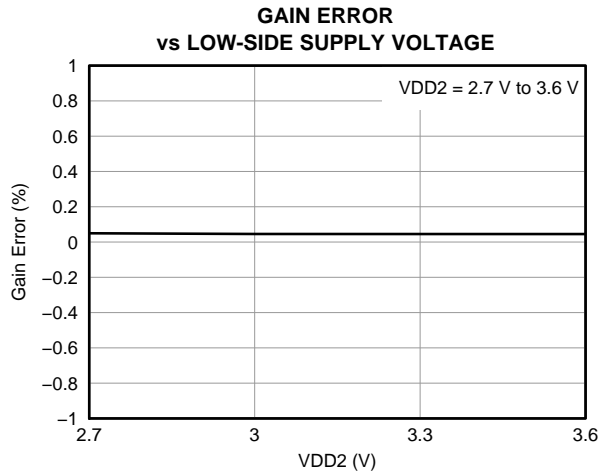


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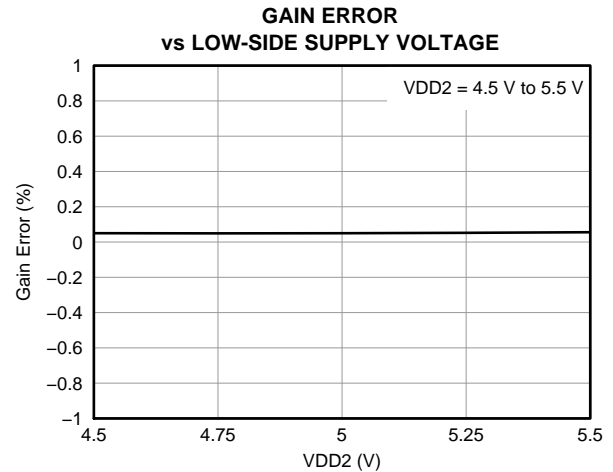


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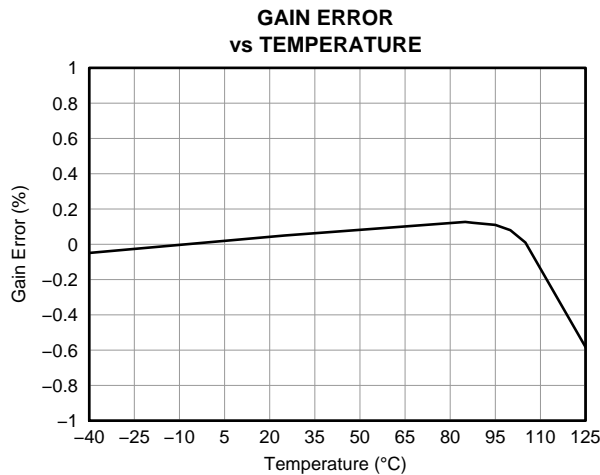


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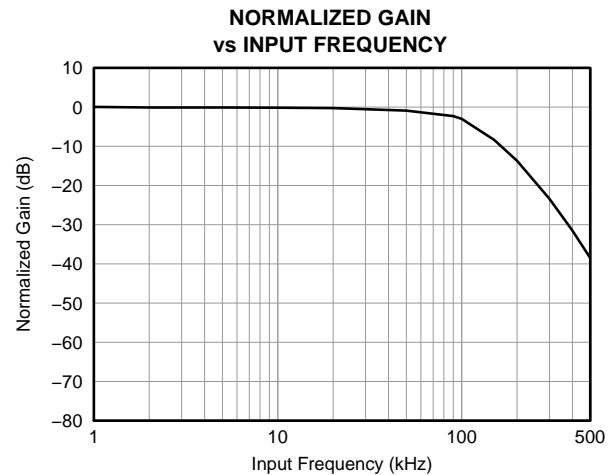


Figure 12.



**TYPICAL CHARACTERISTICS (continued)**

At VDD1 = VDD2 = 5 V, VINP = -250 mV to 250 mV, and VINN = 0 V, unless otherwise noted.

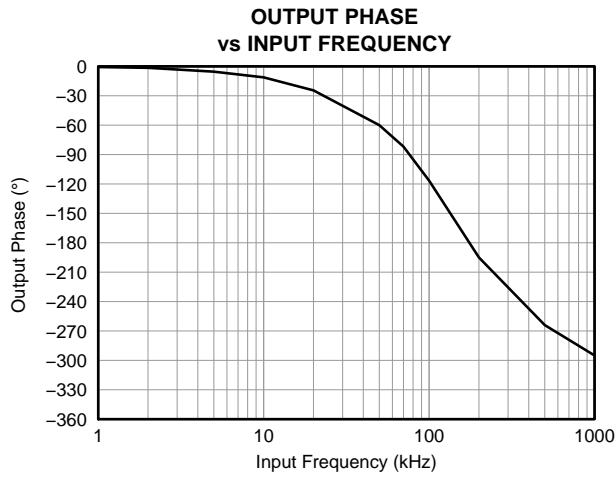


Figure 13.

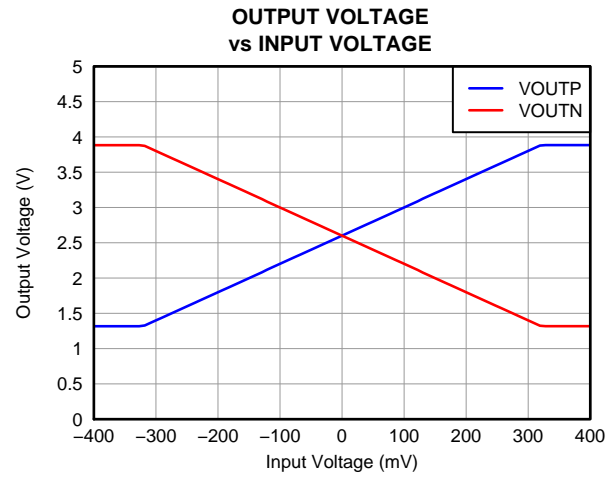


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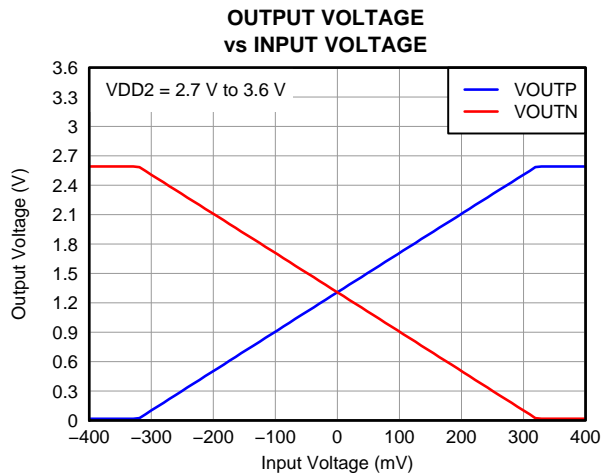


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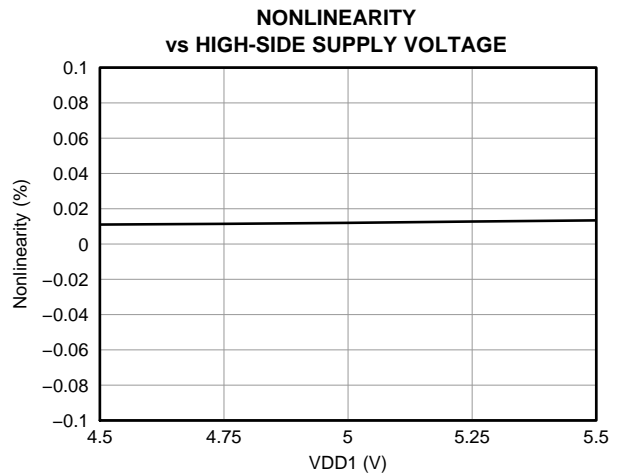


Figure 16.

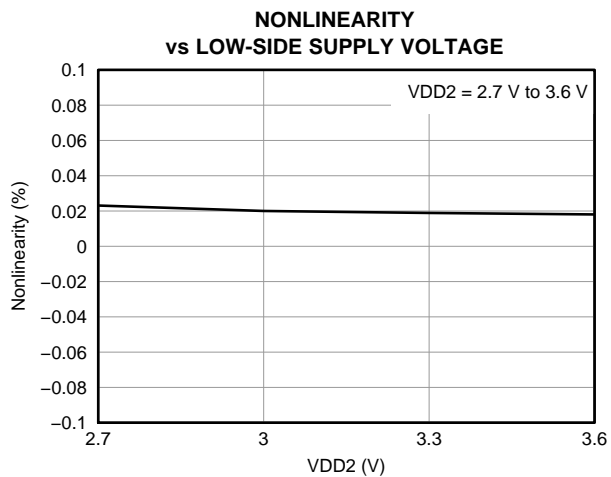


Figure 17.

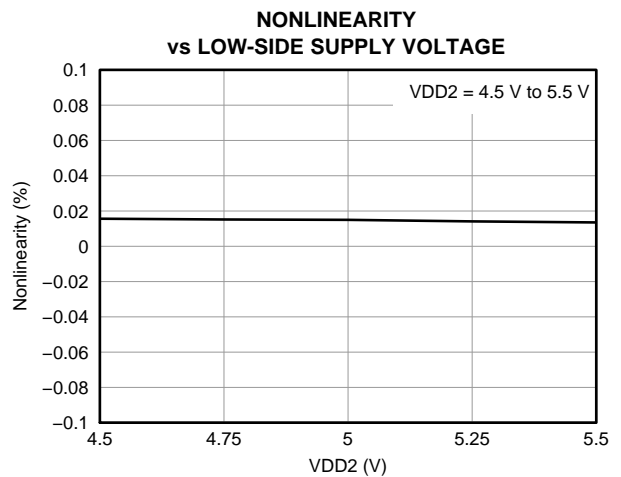


Figure 18.

**TYPICAL CHARACTERISTICS (continued)**

At VDD1 = VDD2 = 5 V, VINP = -250 mV to 250 mV, and VINN = 0 V, unless otherwise noted.

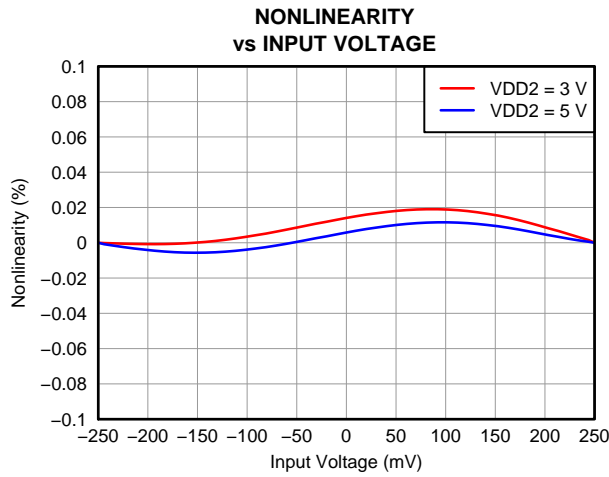


Figure 19.

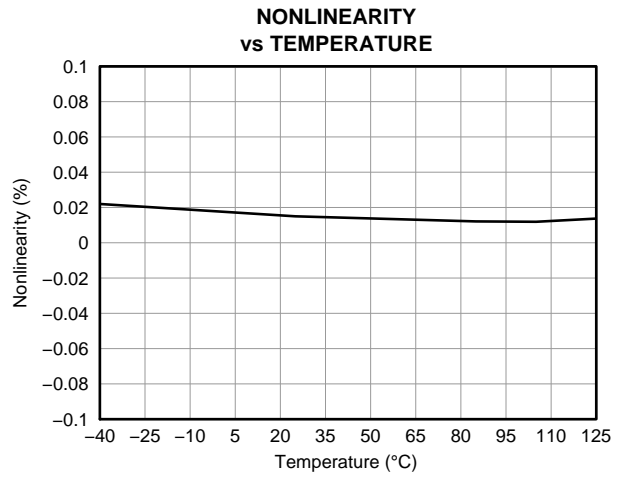


Figure 20.

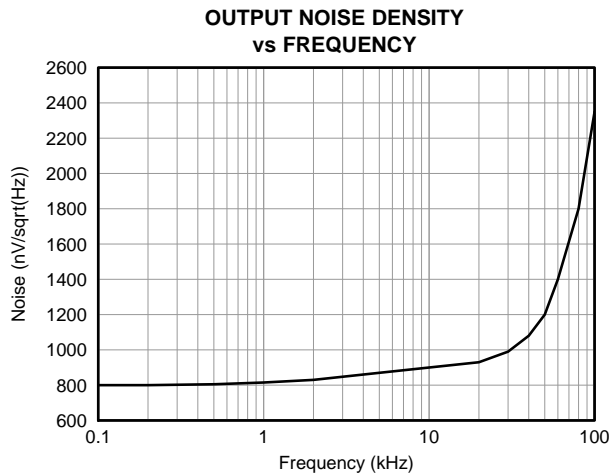


Figure 21.

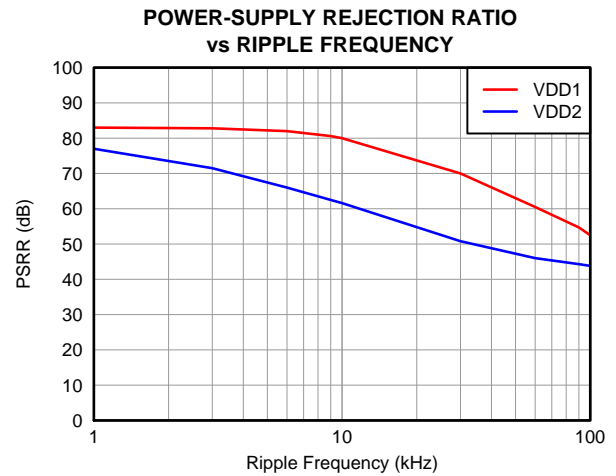


Figure 22.

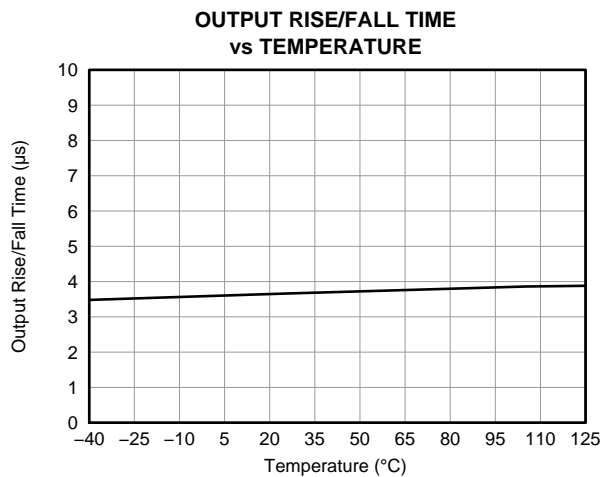


Figure 23.

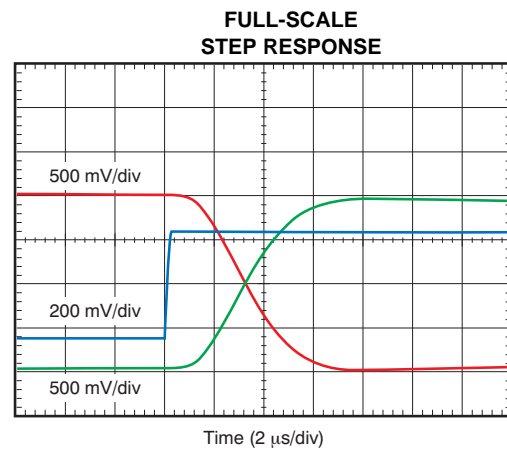


Figure 24.

**TYPICAL CHARACTERISTICS (continued)**

At VDD1 = VDD2 = 5 V, VINP = -250 mV to 250 mV, and VINN = 0 V, unless otherwise noted.

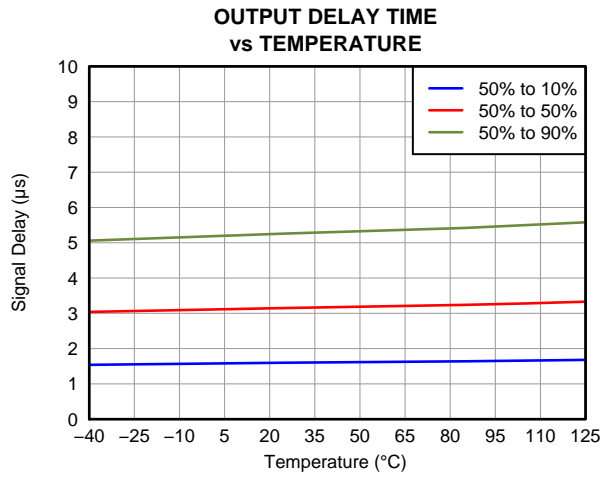


Figure 25.

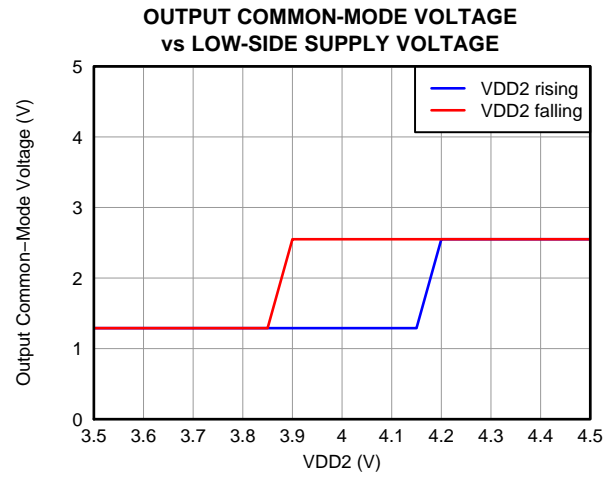


Figure 26.

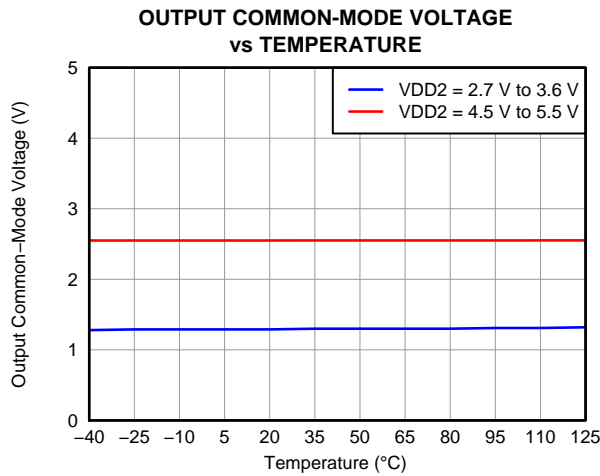


Figure 27.

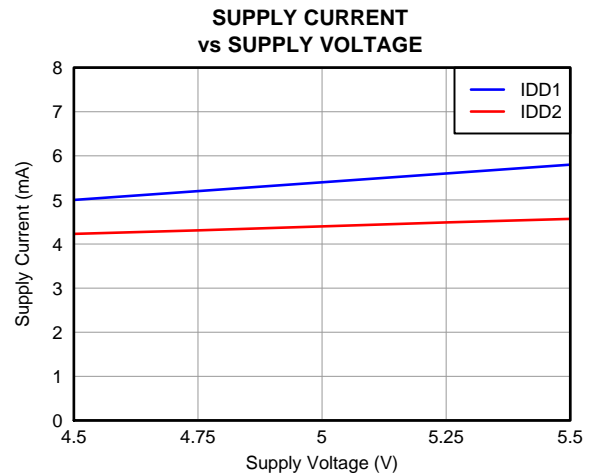


Figure 28.

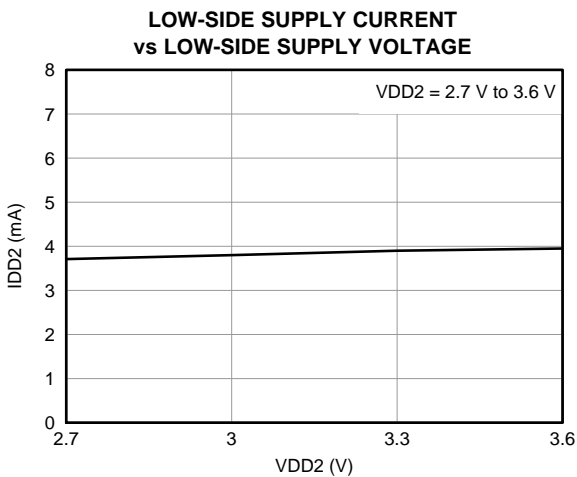


Figure 29.

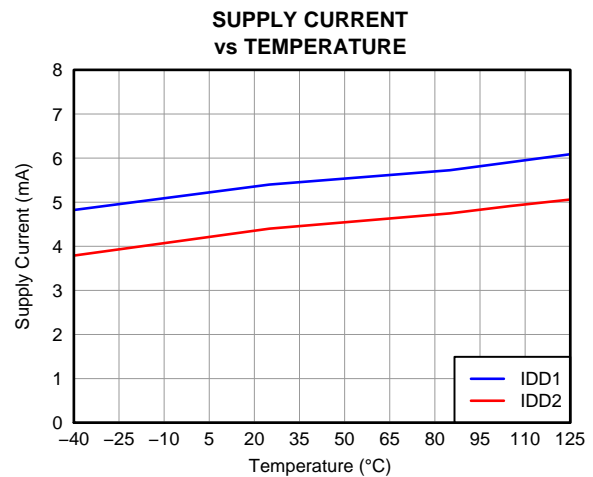


Figure 30.

## THEORY OF OPERATION

### INTRODUCTION

The differential analog input of the AMC1200-Q1 is a switched-capacitor circuit based on a second-order modulator stage that digitizes the input signal into a 1-bit output stream. The device compares the differential input signal ( $V_{IN} = V_{INP} - V_{INN}$ ) against the internal reference of 2.5 V using internal capacitors that are continuously charged and discharged with a typical frequency of 10 MHz. With the S1 switches closed,  $C_{IND}$  charges to the voltage difference across  $V_{INP}$  and  $V_{INN}$ . For the discharge phase, both S1 switches open first and then both S2 switches close.  $C_{IND}$  discharges to approximately  $AGND + 0.8 V$  during this phase. Figure 31 shows the simplified equivalent input circuitry.

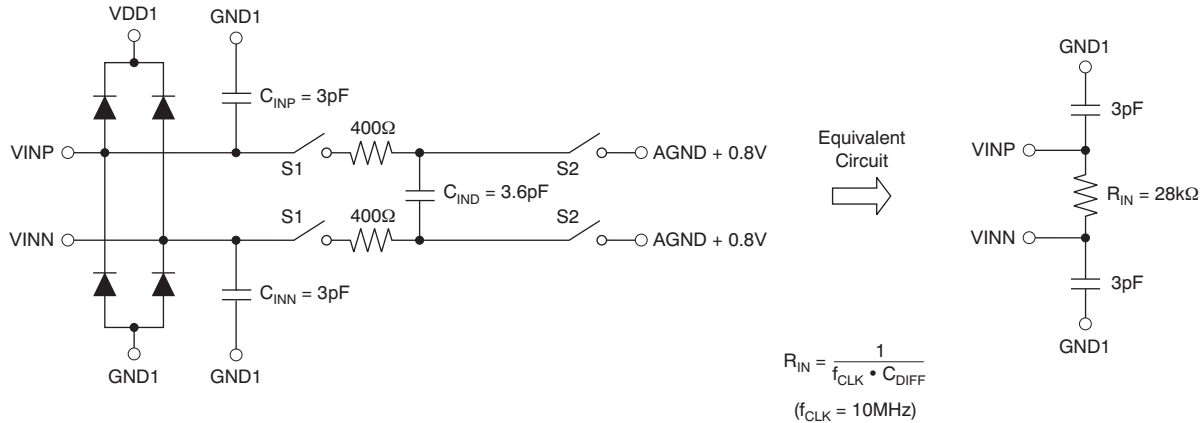


Figure 31. Equivalent Input Circuit

The analog input range is tailored to accommodate directly a voltage drop across a shunt resistor used for current sensing. However, there are two restrictions on the analog input signals,  $V_{INP}$  and  $V_{INN}$ . If the input voltage exceeds the range  $AGND - 0.5 V$  to  $AVDD + 0.5 V$ , the input current must be limited to 10 mA to protect the implemented input protection diodes from damage. In addition, the linearity and the noise performance of the device meet specifications only when the differential analog input voltage remains within  $\pm 250 mV$ .

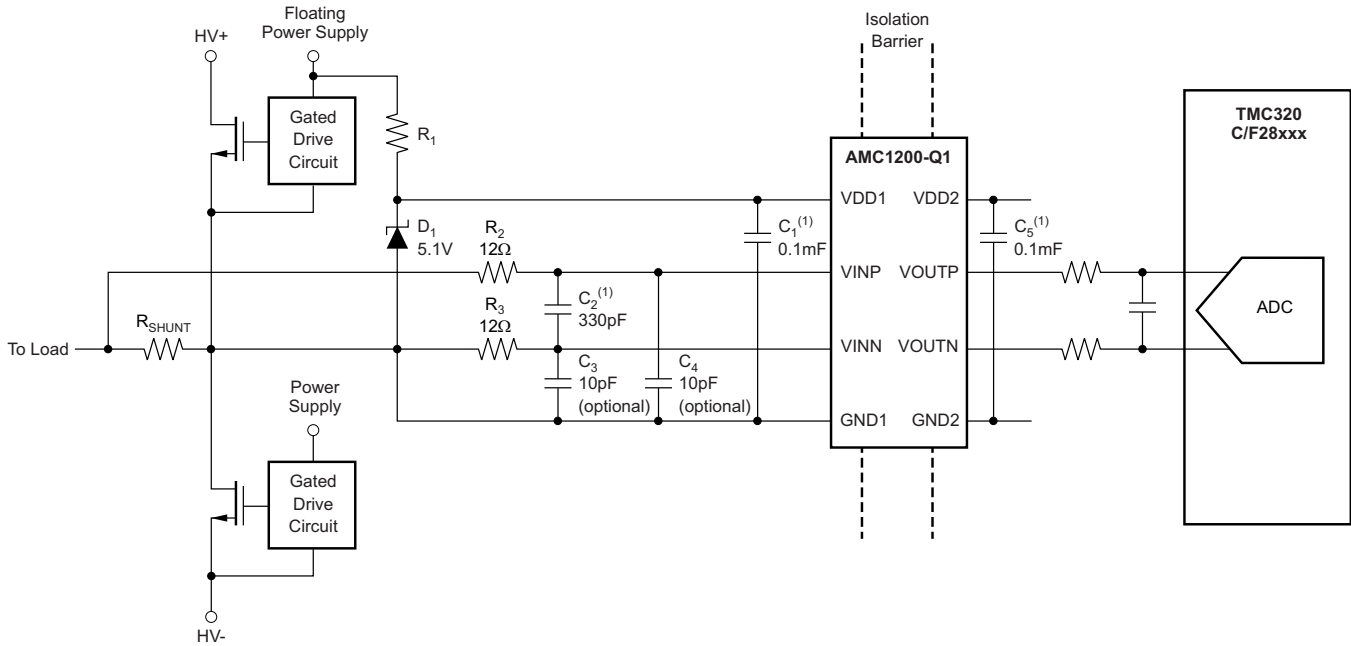
The isolated digital bit stream is processed by a third-order analog filter on the low side and presented as a differential output of the device.

The  $SiO_2$ -based capacitive isolation barrier supports a high level of magnetic field immunity, as described in application report [SLLA181](#), *ISO72x Digital Isolator Magnetic-Field Immunity* (available for download at [www.ti.com](#)).

## APPLICATION INFORMATION

### MOTOR CONTROL

A typical operation of the AMC1200-Q1 in a motor-control application is shown in [Figure 32](#). Measurement of the motor phase current is done through the shunt resistor,  $R_{SHUNT}$  (in this case, a two-terminal shunt). For better performance, the differential signal is filtered using RC filters (components  $R_2$ ,  $R_3$ , and  $C_2$ ). Optionally,  $C_3$  and  $C_4$  can be used to reduce charge dumping from the inputs. In this case, care should be taken when choosing the quality of these capacitors; mismatch in values of these capacitors leads to a common-mode error at the input of the modulator.



(1) Place these capacitors as close as possible to the AMC1200-Q1.

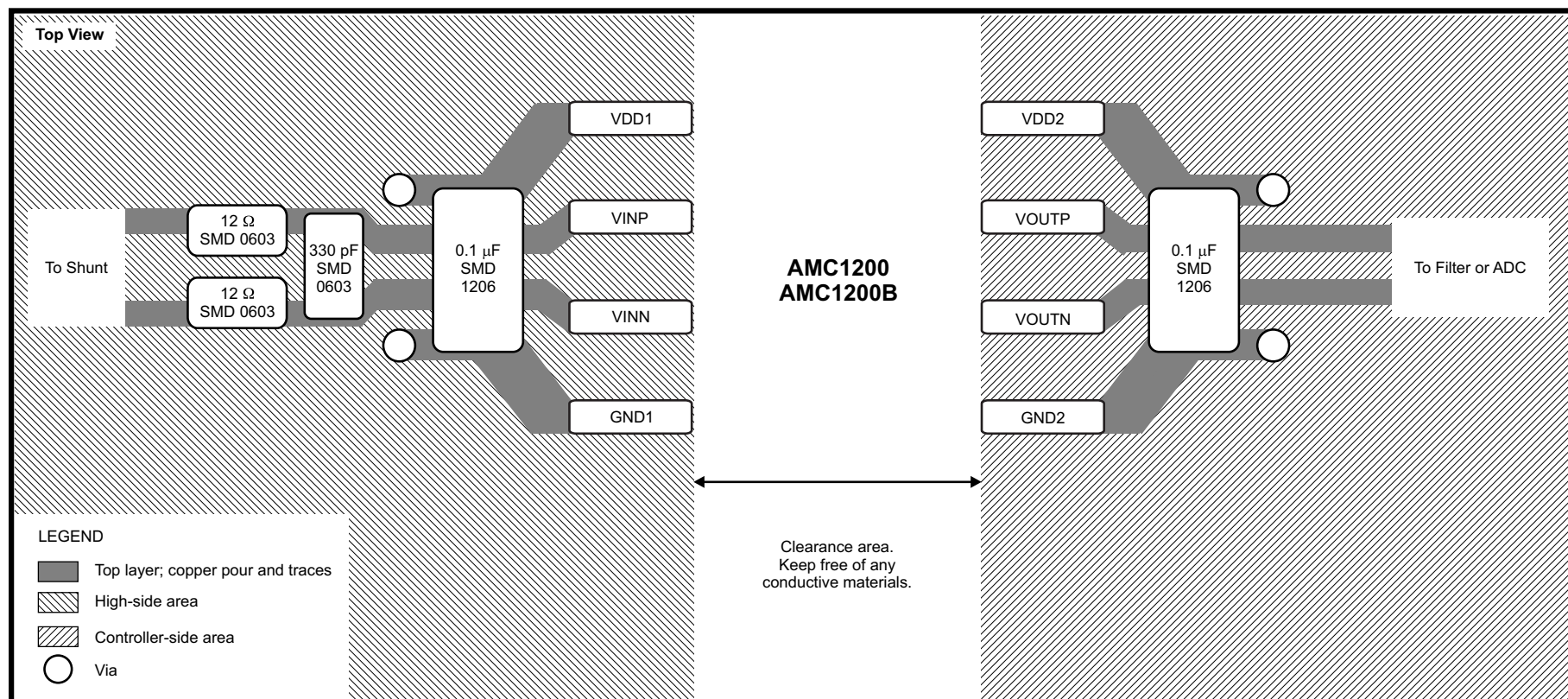
**Figure 32. Typical Application Diagram for the AMC1200-Q1**

The high-side power supply for the AMC1200-Q1 (VDD1) is derived from the power supply of the upper gate driver. For lowest cost, a Zener diode can be used to limit the voltage to  $5\text{ V} \pm 10\%$ . A decoupling capacitor of  $0.1\ \mu\text{F}$  is recommended for filtering this power-supply path. This capacitor ( $C_1$  in [Figure 32](#)) should be placed as close as possible to the VDD1 pin for best performance. If better filtering is required, an additional  $1\text{-}\mu\text{F}$  to  $10\text{-}\mu\text{F}$  capacitor can be used. The floating ground reference (GND1) is derived from the end of the shunt resistor that is connected to the negative input of the AMC1200-Q1 (VINN). If a four-terminal shunt is used, the inputs of AMC1200-Q1 are connected to the inner leads, whereas GND1 is connected to one of the outer leads of the shunt.

The high transient immunity of the AMC1200-Q1 ensures reliable and accurate operation even in high-noise environments such as the power stages of the motor drives.

The differential output of the AMC1200-Q1 can either directly drive an analog-to-digital converter (ADC) input or can be further filtered before being processed by the ADC.

As shown in [Figure 33](#), it is recommended to place the bypass and filter capacitors as close as possible to the AMC1200-Q1 to ensure best performance.



**Figure 33. AMC1200-Q1 Layout Recommendation**

To maintain the isolation barrier and the high CMTI of the device, the distance between the high-side ground (GND1) and the low-side ground (GND2) should be kept at maximum; that is, the entire area underneath the device should be kept free of any conducting materials.

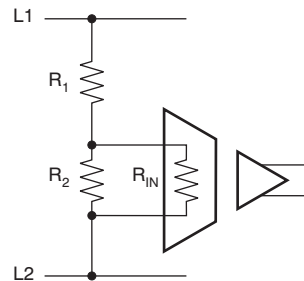
## VOLTAGE MEASUREMENT

The AMC1200-Q1 can also be used for isolated voltage measurement applications, as shown in a simplified way in [Figure 34](#). In such applications, usually a resistor divider ( $R_1$  and  $R_2$  in [Figure 34](#)) is used to match the relatively small input voltage range of the AMC1200-Q1.  $R_2$  and the input resistance  $R_{IN}$  of the AMC1200-Q1 also create a resistance divider that results in additional gain error. With the assumption that  $R_1$  and  $R_{IN}$  have a considerably higher value than  $R_2$ , the resulting total gain error can be estimated using [Equation 1](#):

$$G_{ERRTOT} = G_{ERR} + \frac{R_2}{R_{IN}}$$

Where  $G_{ERR}$  = the gain error of the AMC1200-Q1.

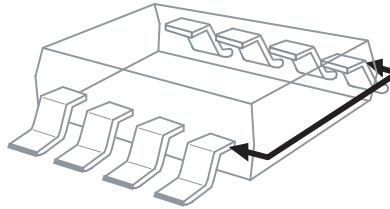
(1)



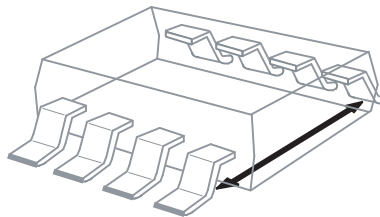
**Figure 34. Voltage Measurement Application**

## ISOLATION GLOSSARY

**Creepage Distance:** The shortest path between two conductive input to output leads measured along the surface of the insulation. The shortest distance path is found around the end of the package body.



**Clearance:** The shortest distance between two conductive input to output leads measured through air (line of sight).



**Input-to-Output Barrier Capacitance:** The total capacitance between all input terminals connected together, and all output terminals connected together.

**Input-to-Output Barrier Resistance:** The total resistance between all input terminals connected together, and all output terminals connected together.

**Primary Circuit:** An internal circuit directly connected to an external supply main or other equivalent source that supplies the primary-circuit electric power.

**Secondary Circuit:** A circuit with no direct connection to primary power that derives its power from a separate isolated source.

**Comparative Tracking Index (CTI):** CTI is an index used for electrical insulating materials. It is defined as the numerical value of the voltage that causes failure by tracking during standard testing. Tracking is the process that produces a partially conducting path of localized deterioration on or through the surface of an insulating material as a result of the action of electric discharges on or close to an insulation surface. The higher CTI value of the insulating material, the smaller the minimum creepage distance.

Generally, insulation breakdown occurs either through the material, over its surface, or both. Surface failure may arise from flashover or from the progressive degradation of the insulation surface by small localized sparks. Such sparks are the result of the breaking of a surface film of conducting contaminant on the insulation. The resulting break in the leakage current produces an overvoltage at the site of the discontinuity, and an electric spark is generated. These sparks often cause carbonization on insulation material and lead to a carbon track between points of different potential. This process is known as tracking.

### Insulation:

*Operational insulation*—Insulation needed for the correct operation of the equipment.

*Basic insulation*—Insulation to provide basic protection against electric shock.

*Supplementary insulation*—Independent insulation applied in addition to basic insulation in order to ensure protection against electric shock in the event of a failure of the basic insulation.

*Double insulation*—Insulation comprising both basic and supplementary insulation.

*Reinforced insulation*—A single insulation system that provides a degree of protection against electric shock equivalent to double insulation.



**Pollution Degree:**

*Pollution Degree 1*—No pollution, or only dry, nonconductive pollution occurs. The pollution has no influence on device performance.

*Pollution Degree 2*—Normally, only nonconductive pollution occurs. However, a temporary conductivity caused by condensation is to be expected.

*Pollution Degree 3*—Conductive pollution, or dry nonconductive pollution that becomes conductive because of condensation, occurs. Condensation is to be expected.

*Pollution Degree 4*—Continuous conductivity occurs as a result of conductive dust, rain, or other wet conditions.

**Installation Category:**

*Overvoltage Category*—This section is directed at insulation coordination by identifying the transient overvoltages that may occur, and by assigning four different levels as indicated in IEC 60664.

1. Signal Level: Special equipment or parts of equipment.
2. Local Level: Portable equipment, etc.
3. Distribution Level: Fixed installation.
4. Primary Supply Level: Overhead lines, cable systems.

Each category should be subject to smaller transients than the previous category.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
AMC1200STDUBRQ1	ACTIVE	SOP	DUB	8	350	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF AMC1200-Q1 :**

- Catalog: [AMC1200](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1200STDUBRQ1	SOP	DUB	8	350	330.0	24.4	10.9	10.01	5.85	16.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

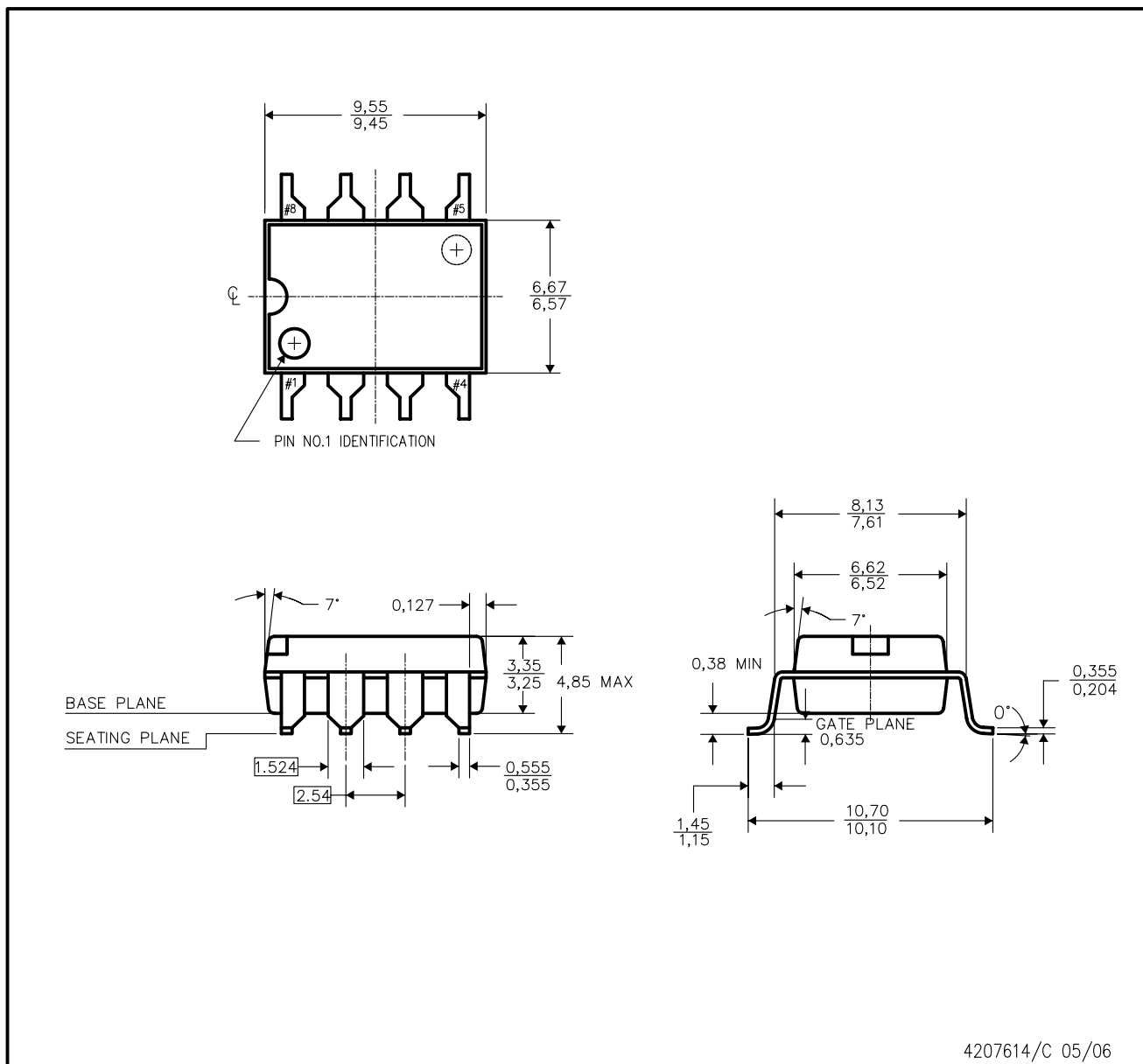


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1200STDUBRQ1	SOP	DUB	8	350	358.0	335.0	35.0

DUB (R-PDSO-G8)

PLASTIC SMALL-OUTLINE

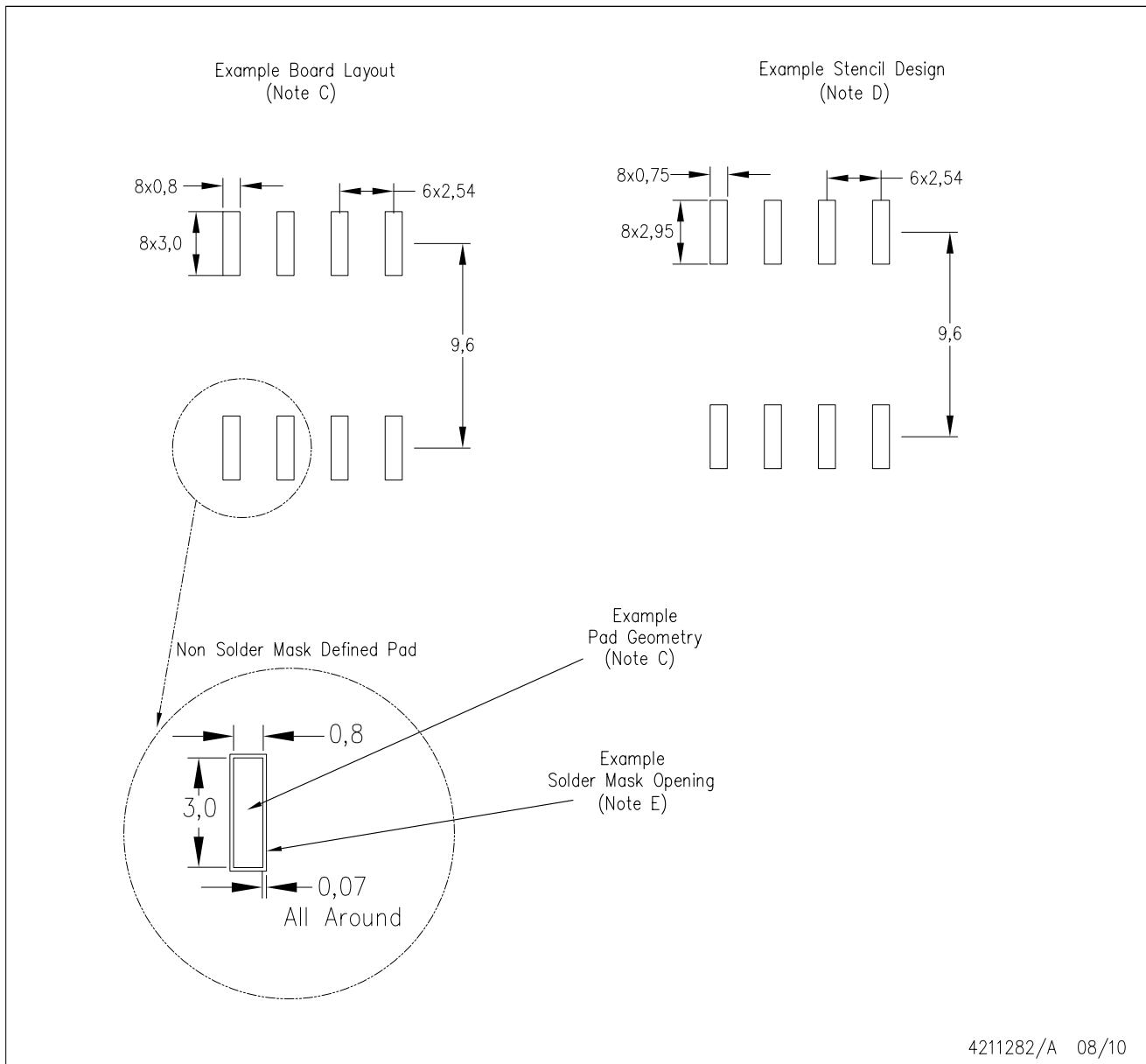


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- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ANSI Y14.5 M-1982.
  - B. This drawing is subject to change without notice.
  - C. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.254mm.

DUB (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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