# 12-Bit, 100-MSPS, 8-Channel Analog-to-Digital Converter

**Check for Samples: ADS5295**

## FEATURES

- **Maximum Sample Rate: 100 MSPS**
- **Designed for Low Power:**
  - **80 mW per channel at 100 MSPS**
- **SNR: 70.6 dBFS**
- **SFDR: 85 dBc at 10 MHz, 100 MSPS**
- **Serial LVDS ADC Data Outputs:**
  - **One- or Two-Wire Serialized LVDS Outputs per Channel**
  - **One-Wire Interface: Up to 80 MSPS Sample Rate**
  - **Two-Wire Interface: Up to 100 MSPS Sample Rate**
- **Digital Processing Block:**
  - **Programmable FIR Decimation Filter and Oversampling to Minimize Harmonic Interference**
  - **Programmable IIR High-Pass Filter to Minimize DC Offset**
  - **Programmable Digital Gain: 0 dB to 12 dB**
- **Low-Frequency Noise Suppression Mode**
- **Programmable Mapping Between ADC Input Channels and LVDS Output Pins**
- **Channel Averaging Mode**
- **Variety of LVDS Test Patterns to Verify Data Capture by FPGA or Receiver**
- **Package: 12-mm × 12-mm QFP-80**

## APPLICATIONS

- **Ultrasound Imaging**
- **Communication Applications**
- **Multichannel Data Acquisition**

## DESCRIPTION

The ADS5295 is a low-power, 12-bit, 100-MSPS, 8-channel analog-to-digital converter (ADC). Low power consumption and integration of multiple channels in a compact package make the device attractive for very high channel count data acquisition systems.

Serial low-voltage differential signaling (LVDS) outputs reduce the number of interface lines and enable high system integration. The ADC digital data can be output over one or two wires of LVDS pins per channel. At high sample rates, the two-wire interface helps keep the serial data rate low, allowing low-cost field-programmable gate array (FPGA)-based receivers to be used.

The device integrates an internal reference trimmed to accurately match across devices. Best performance is expected to be achieved through the internal reference mode. However, the device can be driven with external references as well.

Several digital functions that are commonly used in systems are included in the device. These functions include a low-frequency suppression mode, digital filtering options, and programmable mapping.

For low input frequency applications, the low-frequency noise suppression mode enables noise suppression at low frequencies and improves signal-to-noise ratio (SNR) in the 1-MHz band near dc by approximately 3 dB. Digital filtering options include low-pass, high-pass, and band-pass digital filters, as well as dc offset removal filters. The device also provides programmable mapping of the LVDS output pins and analog input channels. For applications where the 12-bit ADC SNR is not required, the ADS5295 can be configured as an 8-channel, 10-bit ADC with 10x LVDS serialization to reduce the output data rate.

The device is available in a 12-mm × 12-mm QFP-80 package. The ADS5295 is specified over the –40°C to +85°C operating temperature range.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION[1]

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER |
|---|---|---|---|---|---|
| ADS5295 | TQFP-80 | PFP | –40°C to +85°C | ADS5295 | ADS5295IPFP |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS[1]

Over operating free-air temperature range, unless otherwise noted.

| PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| Supply voltage range | AVDD | –0.3 to 2.2 | V |
| | LVDD | –0.3 to 2.2 | V |
| Voltage between | AGND and LGND | –0.3 to 0.3 | V |
| | AVDD to LVDD (when AVDD leads LVDD) | 0 to 2.2 | V |
| | LVDD to AVDD (when LVDD leads AVDD) | 0 to 2.2 | V |
| Voltage applied to | INP, INN | –0.3 to min (2.2, AVDD + 0.3) | V |
| | RESET, SCLK, SDATA, $\overline{CS}$, PD, SYNC, CLKP, CLKN[2] | –0.3 to min (2.2, AVDD + 0.3) | V |
| | Digital outputs | –0.3 to min (2.2, LVDD + 0.3) | V |
| Temperature range | Operating free-air, $T_A$ | –40 to +85 | °C |
| | Operating junction, $T_J$ | +105 | °C |
| | Storage, $T_{stg}$ | –55 to +150 | °C |
| Electrostatic discharge (ESD) rating | Human body model (HBM) | 2000 | V |

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) When AVDD is turned off, TI recommends switching off the input clock (or ensuring the voltage on CLKP and CLKN is less than |0.3 V|. This setting prevents the ESD protection diodes at the clock input pins from turning on.

## THERMAL INFORMATION

| THERMAL METRIC[1] | | ADS5295 | UNITS |
|---|---|---|---|
| | | PFP (TQFP) | |
| | | 80 PINS | |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 30.8 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 6.3 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 8.3 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.2 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 8.2 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | 0.3 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## RECOMMENDED OPERATING CONDITIONS

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLIES** | | | | | | |
| AVDD | Analog supply voltage | | 1.7 | 1.8 | 1.9 | V |
| LVDD | Digital supply voltage | | 1.7 | 1.8 | 1.9 | V |
| **ANALOG INPUTS** | | | | | | |
| $V_{ID}$ | Differential input voltage range | | | 2 | | $V_{PP}$ |
| | Input common-mode voltage | | | VCM ± 0.05 | | V |
| REFT | External reference mode | | | 1.45 | | V |
| REFB | External reference mode | | | 0.45 | | V |
| VCM | Common-mode voltage output | | | 0.95 | | V |
| **CLOCK INPUTS (ADCLK Input Sample Rate)** | | | | | | |
| | ADCLK input sample rate (1 / $t_C$) | One-wire LVDS interface | 10 | | 80 | MSPS |
| | | Two-wire LVDS interface | 10 | | 100 | MSPS |
| | Input clock amplitude differential (VCLKP – VCLKN) | Sine-wave, ac-coupled | | 1.5 | | $V_{PP}$ |
| | | LVPECL, ac-coupled | | 1.6 | | $V_{PP}$ |
| | | LVDS, ac-coupled | | 0.7 | | $V_{PP}$ |
| | Input clock CMOS single-ended (VCLKP) | $V_{IL}$ | | < 0.3 | | V |
| | | $V_{IH}$ | | > 1.5 | | V |
| | Input clock duty cycle | | 35 | 50 | 65 | % |
| **DIGITAL OUTPUTS** | | | | | | |
| | ADCLKP and ADCLKN outputs (LVDS), one-wire | | | 1x (sample rate in MSPS) | | MHz |
| | ADCLKP and ADCLKN outputs (LVDS), two-wire | | | 0.5x (sample rate in MSPS) | | MHz |
| | LCLKP and LCLKN outputs (LVDS), one-wire | 12x serialization | | 6x (sample rate in MSPS) | | MHz |
| | | 10x serialization | | 5x (sample rate in MSPS) | | MHz |
| | LCLKP and LCLKN outputs (LVDS), two-wire | 12x serialization | | 3x (sample rate in MSPS) | | MHz |
| | | 10x serialization | | 2.5x (sample rate in MSPS) | | MHz |

## ELECTRICAL CHARACTERISTICS: General

Typical values are at $T_A$ = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, 100 MSPS, two-wire LVDS interface, and –1-dBFS differential analog input, unless otherwise noted.
Minimum and maximum values are across the full temperature range of $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, AVDD = 1.8 V, and LVDD = 1.8 V.

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **RESOLUTION** | | | | | | | |
| | Resolution | | | | | 12 | Bits |
| **ANALOG INPUTS** | | | | | | | |
| | Differential input voltage range | | | | 2.0 | | $V_{PP}$ |
| | Differential input resistance | | At dc | | 2 | | kΩ |
| | Differential input capacitance | | At dc | | 3.7 | | pF |
| | Analog input bandwidth | | | | 500 | | MHz |
| | Analog input common-mode current (per input pin) | | | | 1 | | µA/MSPS |
| VCM | Common-mode output voltage | | | | 0.95 | | V |
| | VCM output current capability | | | | 5 | | mA |
| **DYNAMIC ACCURACY** | | | | | | | |
| $E_O$ | Offset error | | | –20 | | 20 | mV |
| $E_{GREF}$ | Gain error | Resulting from internal reference inaccuracy alone | | –1.5 | | 1.5 | %FS |
| $E_{GCHAN}$ | | Of channel itself | | | 0.5 | | %FS |
| | $E_{GCHAN}$ temperature coefficient | | | | < 0.01 | | Δ%FS/°C |
| **POWER SUPPLY** | | | | | | | |
| IAVDD | Analog supply current | | 100 MSPS | | 206 | 225 | mA |
| ILVDD | Output buffer supply current | | 100 MSPS, two-wire LVDS interface, 350-mV swing with 100-Ω external termination | | 150 | 163 | mA |
| AVDD | Analog power | | 100 MSPS | | 370.8 | | mW |
| LVDD | Digital power | | 100 MSPS, two-wire LVDS interface, 350-mV swing with 100-Ω external termination | | 270 | | mW |
| | Total power | | 100 MSPS, two-wire LVDS interface, 350-mV swing with 100-Ω external termination | | 640.8 | | mW |
| | Global power-down | | | | | 45 | mW |
| | Standby power | | | | 192 | | mW |

## ELECTRICAL CHARACTERISTICS: Dynamic Performance

Typical values are at $T_A$ = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, maximum rated sampling frequency, 50% clock duty cycle, 100 MSPS, two-wire LVDS interface, and –1-dBFS differential analog input, unless otherwise noted.
Minimum and maximum values are across the full temperature range of $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, AVDD = 1.8 V, and LVDD = 1.8 V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| SNR | Signal-to-noise ratio | $f_{IN}$ = 5 MHz | 67.5 | 70.6 | | dBFS |
| | | $f_{IN}$ = 30 MHz | | 70.4 | | dBFS |
| | | $f_{IN}$ = 70 MHz | | 69.7 | | dBFS |
| SINAD | Signal-to-noise and distortion ratio | $f_{IN}$ = 5 MHz | 66 | 70.4 | | dBFS |
| | | $f_{IN}$ = 30 MHz | | 70 | | dBFS |
| | | $f_{IN}$ = 70 MHz | | 68.9 | | dBFS |
| SFDR | Spurious-free dynamic range | $f_{IN}$ = 5 MHz | 72.5 | 86 | | dBc |
| | | $f_{IN}$ = 30 MHz | | 79 | | dBc |
| | | $f_{IN}$ = 70 MHz | | 76.3 | | dBc |
| THD | Total harmonic distortion | $f_{IN}$ = 5 MHz | 71 | 85 | | dBc |
| | | $f_{IN}$ = 30 MHz | | 78.4 | | dBc |
| | | $f_{IN}$ = 70 MHz | | 75.8 | | dBc |
| HD2 | Second-harmonic distortion | $f_{IN}$ = 5 MHz | 72.5 | 89.5 | | dBc |
| | | $f_{IN}$ = 30 MHz | | 89.5 | | dBc |
| | | $f_{IN}$ = 70 MHz | | 89.5 | | dBc |
| HD3 | Third-harmonic distortion | $f_{IN}$ = 5 MHz | 72.5 | 86 | | dBc |
| | | $f_{IN}$ = 30 MHz | | 79 | | dBc |
| | | $f_{IN}$ = 70 MHz | | 76.4 | | dBc |
| | Worst spur (other than second and third harmonics) | $f_{IN}$ = 5 MHz | 75 | 95 | | dBc |
| | | $f_{IN}$ = 30 MHz | | 93 | | dBc |
| | | $f_{IN}$ = 70 MHz | | 82.3 | | dBc |
| IMD | Two-tone intermodulation distortion | $f_1$ = 8 MHz, $f_2$ = 10 MHz, each tone at –7 dBFS | | 86 | | dBc |
| | Crosstalk | 10-MHz full-scale signal on aggressor channel; 5-MHz input signal applied on victim channel | | 86 | | dB |
| | Input overload recovery | Recovery to within 1% (of full-scale) for 6-dB overload with sine-wave input | | 1 | | Clock cycle |
| PSRR | AC power-supply rejection ratio | For 50-$mV_{PP}$ signal on AVDD supply, up to 10 MHz, no signal applied to analog inputs | | 60 | | dB |
| ENOB | Effective number of bits | $f_{IN}$ = 5 MHz | | 11.4 | | LSBs |
| DNL | Differential nonlinearity | $f_{IN}$ = 5 MHz | –0.82 | ±0.05 | 0.82 | LSBs |
| INL | Integrated nonlinearity | $f_{IN}$ = 5 MHz | | 0.4 | 1.1 | LSBs |

## DIGITAL CHARACTERISTICS

The dc specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level '0' or '1'. AVDD = 1.8 V and DRVDD = 1.8 V.

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **DIGITAL INPUTS (RESET, SCLK, SDATA, $\overline{CS}$, SYNC, PDN)** | | | | | | | |
| $V_{IH}$ | High-level input voltage | | All pins support 1.8-V and 3.3-V CMOS logic levels | 1.3 | | | V |
| $V_{IL}$ | Low-level input voltage | | All pins support 1.8-V and 3.3-V CMOS logic levels | | | 0.4 | V |
| $I_{IH}$ | High-level input current | $\overline{CS}$, SDATA, SCLK(1) | $V_{HIGH}$ = 1.8 V | | 6 | | µA |
| $I_{IL}$ | Low-level input current | $\overline{CS}$, SDATA, SCLK(1) | $V_{LOW}$ = 0 V | | 0.1 | | µA |
| **DIGITAL OUTPUTS (CMOS INTERFACE: SDOUT)** | | | | | | | |
| $V_{OH}$ | High-level output voltage | | | AVDD – 0.1 | | | V |
| $V_{OL}$ | Low-level output voltage | | | | | 0.1 | V |
| **DIGITAL OUTPUTS (LVDS INTERFACE: OUT1A_P, OUT1A_N to OUT8A_P, OUT8A_N and OUT1B_P, OUT1B_N to OUT8B_P, OUT8B_N)** | | | | | | | |
| $V_{ODH}$ | High-level output differential voltage(2) | | | 300 | | 485 | mV |
| $V_{ODL}$ | Low-level output differential voltage(2) | | | -485 | | -300 | mV |
| $V_{OCM}$ | Output common-mode voltage | | | 0.95 | | 1.35 | V |

(1) $\overline{CS}$, SDATA, and SCLK have an internal 220-kΩ pull-down resistor.
(2) With an external 100-Ω termination.

## TIMING REQUIREMENTS(1)

Typical values are at +25°C, AVDD = 1.8 V, LVDD = 1.8 V, sampling frequency = 100 MSPS, sine-wave input clock, $C_{LOAD}$ = 5 pF, and $R_{LOAD}$ = 100 Ω, unless otherwise noted.
Minimum and maximum values are across the full temperature range of $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, AVDD = 1.8 V, and LVDD = 1.7 V to 1.9 V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_A$ | Aperture delay | | | 4 | | ns |
| | Aperture delay matching | Between any two channels of the same device | | ±200 | | ps |
| | Variation of aperture delay | Between two devices at the same temperature and LVDD supply | | ±1 | | ns |
| $t_J$ | Aperture jitter | Sample uncertainty | | 320 | | fs rms |
| | Wake-up time | Time to valid data after coming out of standby | | 5 | | µs |
| | | Time to valid data after coming out of global power-down mode | | 100 | | µs |
| | ADC latency(2) | One-wire LVDS Output interface | | 12 | | Clock cycles |
| | | Two-wire LVDS Output interface | | 16 | | Clock cycles |
| **TWO-WIRE, 12x SERIALIZATION** | | | | | | |
| $t_{SU}$ | Data setup time | Data valid to zero-crossing of LCLKP | 0.52 | | | ns |
| $t_H$ | Data hold time | Zero-crossing of LCLKP to data becoming invalid | 0.62 | | | ns |
| $t_{PDI}$ | Clock propagation delay | Input clock rising edge crossover to output clock rising edge crossover | | $t_{PDI}$ = (11/12) × $t_S$ + $t_{DELAY}$ | | ns |
| $t_{DELAY}$ | Delay time | | 8.5 | 11 | 13.5 | ns |
| | LVDS bit clock duty cycle | Duty cycle of differential clock (LCLKP – LCLKN) | | 50 | | % |
| **ACROSS ALL SERIALIZATION MODES** | | | | | | |
| $t_{FALL}$ | Data fall time | Rise time measured from –100 mV to +100 mV, 10 MSPS ≤ sampling frequency ≤ 100 MSPS | | 0.11 | | ns |
| $t_{RISE}$ | Data rise time | Rise time measured from –100 mV to +100 mV, 10 MSPS ≤ sampling frequency ≤ 100 MSPS | | 0.11 | | ns |
| $t_{CLKRISE}$ | Output clock rise time | Rise time measured from –100 mV to +100 mV, 10 MSPS ≤ sampling frequency ≤ 100 MSPS | | 0.11 | | ns |
| $t_{CLKFALL}$ | Output clock fall time | Rise time measured from –100 mV to +100 mV, 10 MSPS ≤ sampling frequency ≤ 100 MSPS | | 0.11 | | ns |

(1) Timing parameters are ensured by design and characterization, but are not tested in production.
(2) At higher frequencies, $t_{PDI}$ is greater than one clock period and the overall latency = ADC latency + 1.

### Table 1. Two-Wire, 12x Serialization(1)(2)

| SAMPLING FREQUENCY (MSPS) | SETUP TIME (ns) | | | HOLD TIME (ns) | | | $t_{PDI}$ = (11/12) × $t_S$ + $t_{DELAY}$ Where $t_{DELAY}$ is specified as below, ns | | |
|---|---|---|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX |
| 10 | 7.80 | | | 8.00 | | | 8.5 | 11 | 13.5 |
| 30 | 2.40 | | | 2.50 | | | 8.5 | 11 | 13.5 |
| 50 | 1.10 | | | 1.60 | | | 8.5 | 11 | 13.5 |
| 65 | 0.83 | | | 1.25 | | | 8.5 | 11 | 13.5 |
| 80 | 0.60 | | | 1.00 | | | 8.5 | 11 | 13.5 |
| 100 | 0.52 | | | 0.62 | | | 8.5 | 11 | 13.5 |

(1) All the timing specifications are taken with default output clock and data delay settings (0 ps).
(2) Refer to the *Programmable LVDS Output Clock and Data Edges* section in the Application Information for output clock and data delay options.

### Table 2. One-Wire, 12x Serialization(1)(2)

| SAMPLING FREQUENCY (MSPS) | SETUP TIME (ns) | | | HOLD TIME (ns) | | | $t_{PDI}$ = (9/12) × $t_S$ + $t_{DELAY}$ Where $t_{DELAY}$ is specified as below, ns | | |
|---|---|---|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX |
| 10 | 3.90 | | | 4.00 | | | 8 | 10 | 12 |
| 30 | 1.00 | | | 1.30 | | | 8 | 10 | 12 |
| 50 | 0.60 | | | 0.57 | | | 8 | 10 | 12 |
| 65 | 0.40 | | | 0.34 | | | 8 | 10 | 12 |
| 80 | 0.22 | | | 0.24 | | | 8 | 10 | 12 |

(1) All the timing specifications are taken with default output clock and data delay settings (0 ps).
(2) Refer to the *Programmable LVDS Output Clock and Data Edges* section in the Application Information for output clock and data delay options.

### Table 3. Two-Wire, 10x Serialization(1)(2)

| SAMPLING FREQUENCY (MSPS) | SETUP TIME (ns) | | | HOLD TIME (ns) | | |
|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | MIN | TYP | MAX |
| 65 | 1.00 | | | 1.50 | | |
| 80 | 0.74 | | | 1.20 | | |
| 100 | 0.44 | | | 1.00 | | |

(1) All the timing specifications are taken with default output clock and data delay settings (0 ps).
(2) Refer to the *Programmable LVDS Output Clock and Data Edges* section in the Application Information for output clock and data delay options.

### Table 4. One-Wire, 10x Serialization(1)(2)

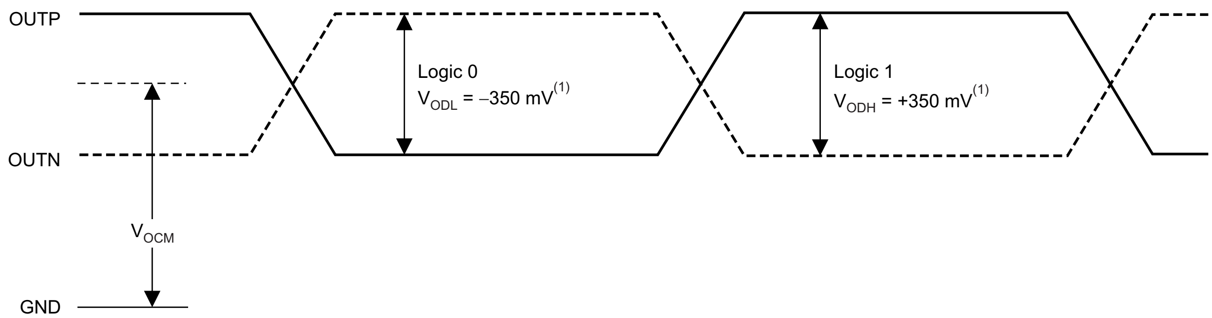
| SAMPLING FREQUENCY (MSPS) | SETUP TIME (ns) | | | HOLD TIME (ns) | | |
|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | MIN | TYP | MAX |
| 65 | 0.51 | | | 0.60 | | |
| 80 | 0.33 | | | 0.36 | | |
| 100 | 0.17 | | | 0.31 | | |

(1) All the timing specifications are taken with default output clock and data delay settings (0 ps).
(2) Refer to the *Programmable LVDS Output Clock and Data Edges* section in the Application Information for output clock and data delay options.

# PARAMETRIC MEASUREMENT INFORMATION

## LATENCY TIMING

Figure 1 shows a timing diagram of the LVDS output voltage levels.




(1) With an external 100-Ω termination.

**Figure 1. LVDS Output Voltage Levels**

Figure 2 shows a latency timing diagram.

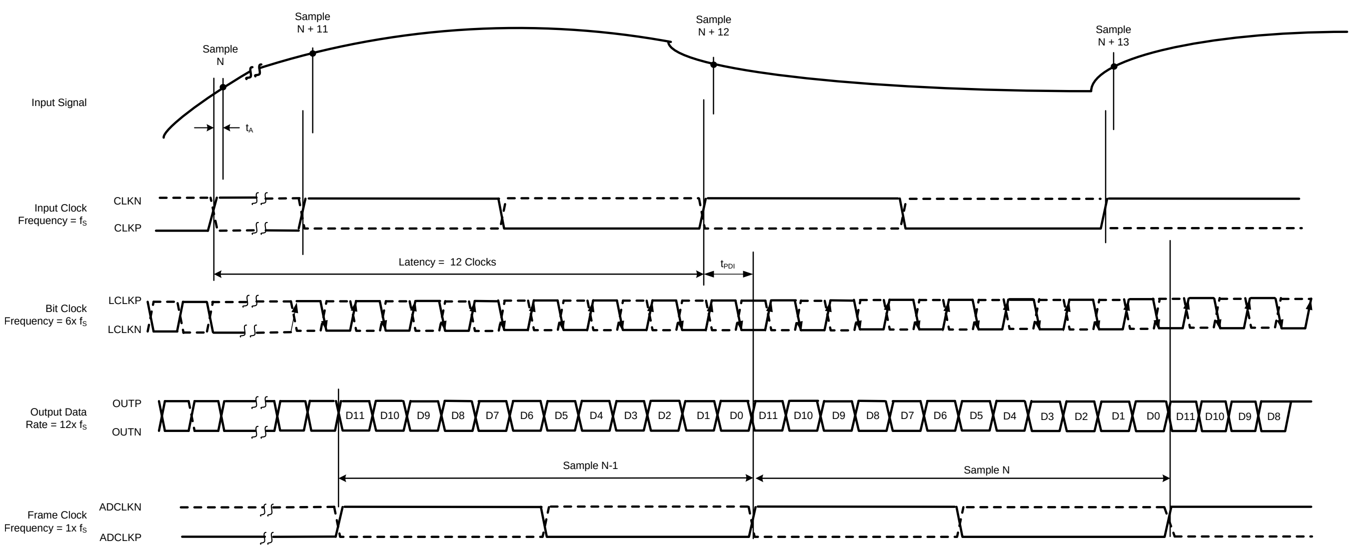
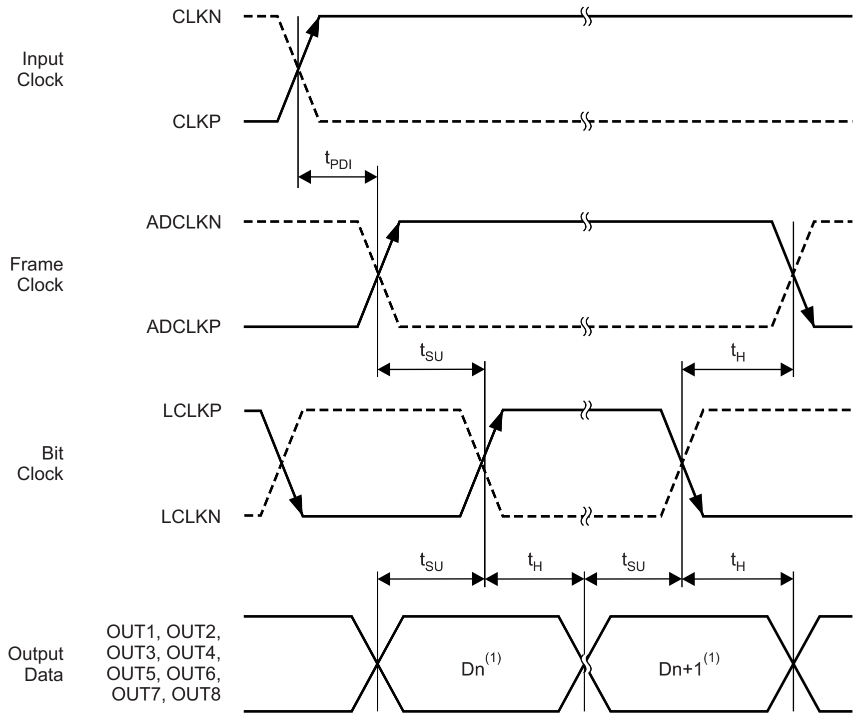



**Figure 2. Latency Timing Diagram**

## LVDS OUTPUT TIMING

Figure 3 shows the output timing described in the Timing Requirements table.

## PARAMETRIC MEASUREMENT INFORMATION (continued)

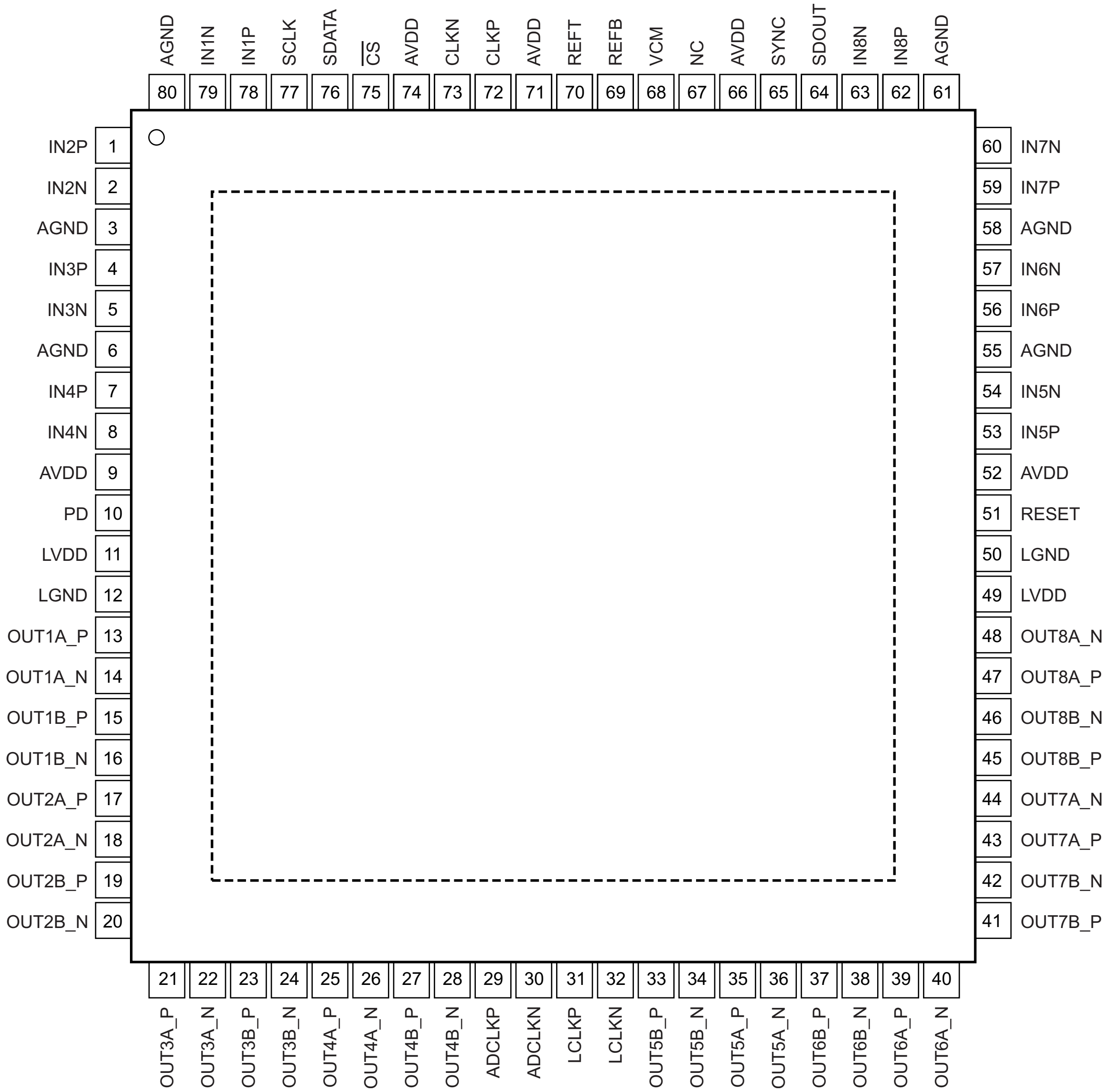



(1) n = 0 to 11.

**Figure 3. LVDS Output Timing**

# PIN DESCRIPTION

**PFP PACKAGE**
**TQFP-80**
**(Top View)**



## PIN DESCRIPTIONS

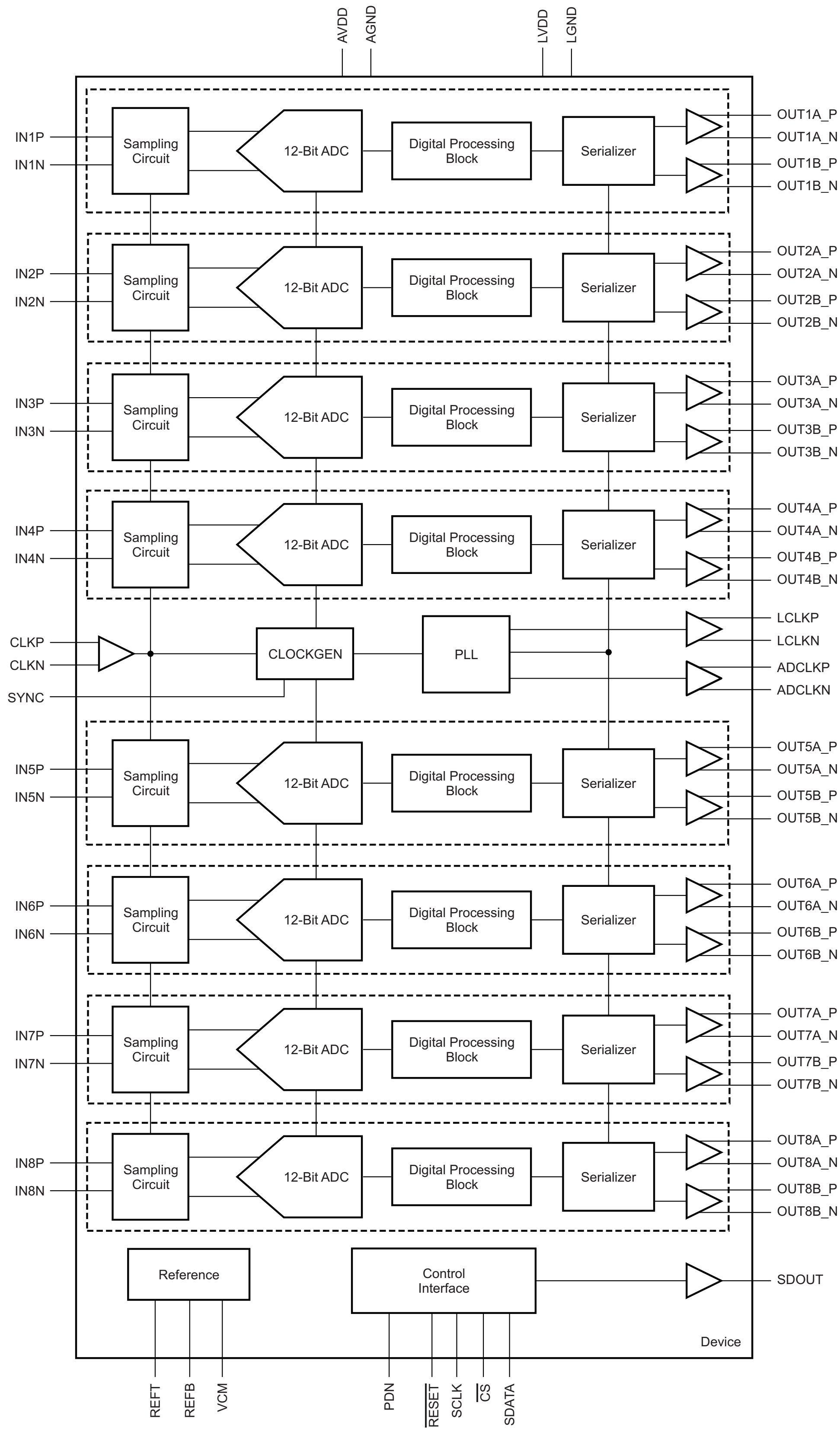
| NAME | NO. | FUNCTION(1) | DESCRIPTION |
|---|---|---|---|
| ADCLKN | 30 | DO | Differential LVDS frame clock (1x), negative |
| ADCLKP | 29 | DO | Differential LVDS frame clock (1x), positive |
| AGND | 3, 6, 55, 58, 61, 80 | G | Analog ground pin |
| AVDD | 9, 52, 66, 71, 74 | S | Analog supply pin, 1.8 V |
| CLKN | 73 | AI | Differential clock input, negative<br>For a single-ended clock, tie CLKN to 0 V |
| CLKP | 72 | AI | Differential clock input, positive |
| $\overline{CS}$ | 75 | DI | Serial enable chip select; active low digital input |
| IN1N | 79 | AI | Differential analog input for channel 1, negative |
| IN1P | 78 | AI | Differential analog input for channel 1, positive |
| IN2N | 2 | AI | Differential analog input for channel 2, negative |
| IN2P | 1 | AI | Differential analog input for channel 2, positive |
| IN3N | 5 | AI | Differential analog input for channel 3, negative |
| IN3P | 4 | AI | Differential analog input for channel 3, positive |
| IN4N | 8 | AI | Differential analog input for channel 4, negative |
| IN4P | 7 | AI | Differential analog input for channel 4, positive |
| IN5N | 54 | AI | Differential analog input for channel 5, negative |
| IN5P | 53 | AI | Differential analog input for channel 5, positive |
| IN6N | 57 | AI | Differential analog input for channel 6, negative |
| IN6P | 56 | AI | Differential analog input for channel 6, positive |
| IN7N | 60 | AI | Differential analog input for channel 7, negative |
| IN7P | 59 | AI | Differential analog input for channel 7, positive |
| IN8N | 63 | AI | Differential analog input for channel 8, negative |
| IN8P | 62 | AI | Differential analog input for channel 8, positive |
| LCLKN | 32 | DO | LVDS differential bit clock output pins (6x), negative |
| LCLKP | 31 | DO | LVDS differential bit clock output pins (6x), positive |
| LGND | 12, 50 | G | Digital ground pin |
| LVDD | 11, 49 | S | Digital and I/O power supply, 1.8 V |
| NC | 67 | — | Do not connect |
| OUT1A_N | 14 | DO | Channel 1 differential LVDS negative data output, one-wire |
| OUT1A_P | 13 | DO | Channel 1 differential LVDS positive data output, one-wire |
| OUT1B_N | 16 | DO | Channel 1 differential LVDS negative data output, two-wire |
| OUT1B_P | 15 | DO | Channel 1 differential LVDS positive data output, two-wire |
| OUT2A_N | 18 | DO | Channel 2 differential LVDS negative data output, one-wire |
| OUT2A_P | 17 | DO | Channel 2 differential LVDS positive data output, one-wire |
| OUT2B_N | 20 | DO | Channel 2 differential LVDS negative data output, two-wire |
| OUT2B_P | 19 | DO | Channel 2 differential LVDS positive data output, two-wire |
| OUT3A_N | 22 | DO | Channel 3 differential LVDS negative data output, one-wire |
| OUT3A_P | 21 | DO | Channel 3 differential LVDS positive data output, one-wire |
| OUT3B_N | 24 | DO | Channel 3 differential LVDS negative data output, two-wire |
| OUT3B_P | 23 | DO | Channel 3 differential LVDS positive data output, two-wire |
| OUT4A_N | 26 | DO | Channel 4 differential LVDS negative data output, one-wire |
| OUT4A_P | 25 | DO | Channel 4 differential LVDS positive data output, one-wire |
| OUT4B_N | 28 | DO | Channel 4 differential LVDS negative data output, two-wire |
| OUT4B_P | 27 | DO | Channel 4 differential LVDS positive data output, two-wire |

(1) Pin functionality: AI = analog input; DI = digital input; DO = digital output; G = ground; and S = supply.

## PIN DESCRIPTIONS (continued)

| NAME | NO. | FUNCTION[1] | DESCRIPTION |
|---|---|---|---|
| OUT5B_N | 34 | DO | Channel 5 differential LVDS negative data output, two-wire |
| OUT5B_P | 33 | DO | Channel 5 differential LVDS positive data output, two-wire |
| OUT5A_N | 36 | DO | Channel 5 differential LVDS negative data output, one-wire |
| OUT5A_P | 35 | DO | Channel 5 differential LVDS positive data output, one-wire |
| OUT6B_N | 38 | DO | Channel 6 differential LVDS negative data output, two-wire |
| OUT6B_P | 37 | DO | Channel 6 differential LVDS positive data output, two-wire |
| OUT6A_N | 40 | DO | Channel 6 differential LVDS negative data output, one-wire |
| OUT6A_P | 39 | DO | Channel 6 differential LVDS positive data output, one-wire |
| OUT7B_N | 42 | DO | Channel 7 differential LVDS negative data output, two-wire |
| OUT7B_P | 41 | DO | Channel 7 differential LVDS positive data output, two-wire |
| OUT7A_N | 44 | DO | Channel 7 differential LVDS negative data output, one-wire |
| OUT7A_P | 43 | DO | Channel 7 differential LVDS positive data output, one-wire |
| OUT8B_N | 46 | DO | Channel 8 differential LVDS negative data output, two-wire |
| OUT8B_P | 45 | DO | Channel 8 differential LVDS positive data output, two-wire |
| OUT8A_N | 48 | DO | Channel 8 differential LVDS negative data output, one-wire |
| OUT8A_P | 47 | DO | Channel 8 differential LVDS positive data output, one-wire |
| PD | 10 | DI | Power-down control input pin |
| REFB | 69 | AI | Negative reference input/output |
| REFT | 70 | AI | Positive reference input/output |
| RESET | 51 | DI | Active high RESET input |
| SCLK | 77 | DI | Serial clock input |
| SDATA | 76 | DI | Serial data input |
| SDOUT | 64 | DO | Serial data output |
| SYNC | 65 | DI | Synchronization input for reduced output data rate |
| VCM | 68 | AI | Common-mode output pin, 0.95-V output |

## FUNCTIONAL BLOCK DIAGRAM



## TYPICAL CHARACTERISTICS: General

Typical values are at $T_A$ = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, 100 MSPS, two-wire LVDS interface, and –1-dBFS differential analog input, unless otherwise noted.

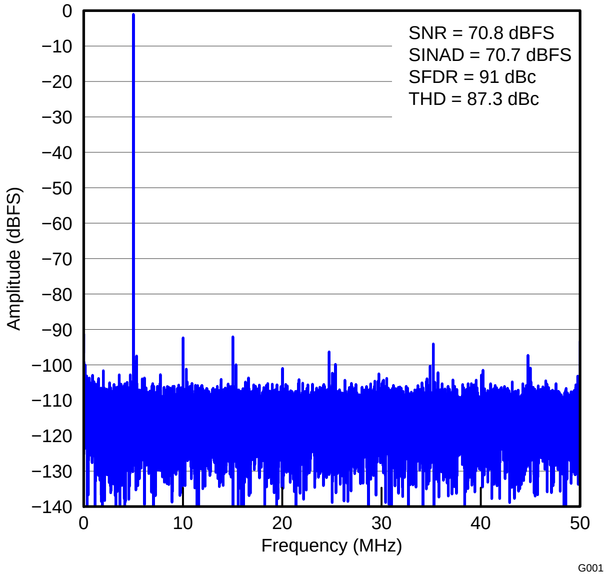



**Figure 4. FFT FOR 5-MHz INPUT SIGNAL (Sample Rate = 100 MSPS)**

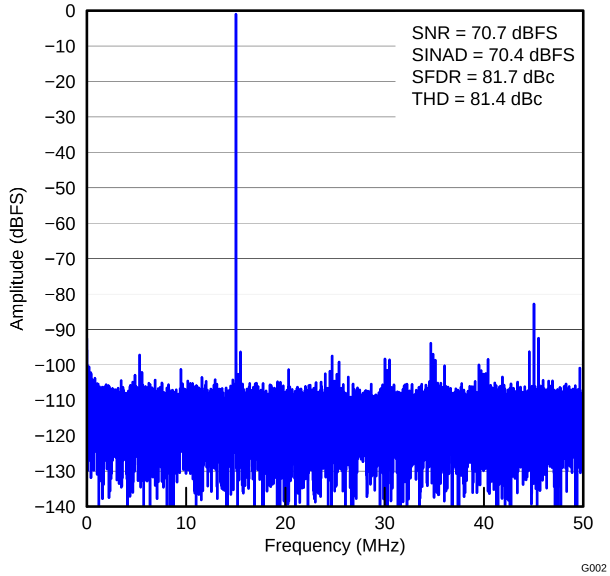



**Figure 5. FFT FOR 15-MHz INPUT SIGNAL (Sample Rate = 100 MSPS)**

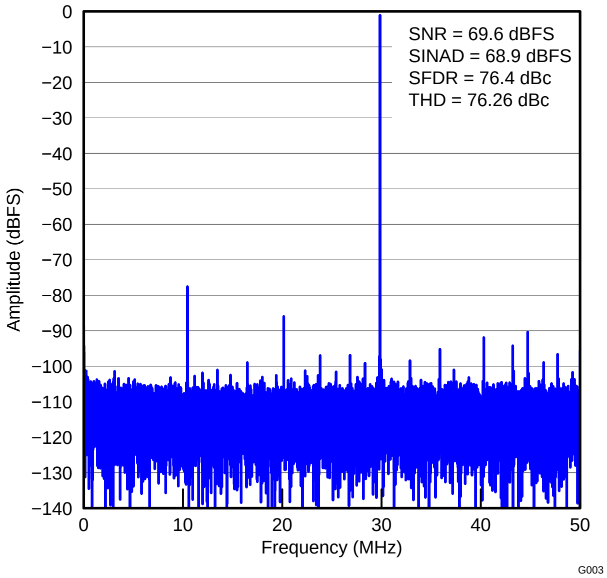



**Figure 6. FFT FOR 70-MHz INPUT SIGNAL (Sample Rate = 100 MSPS)**

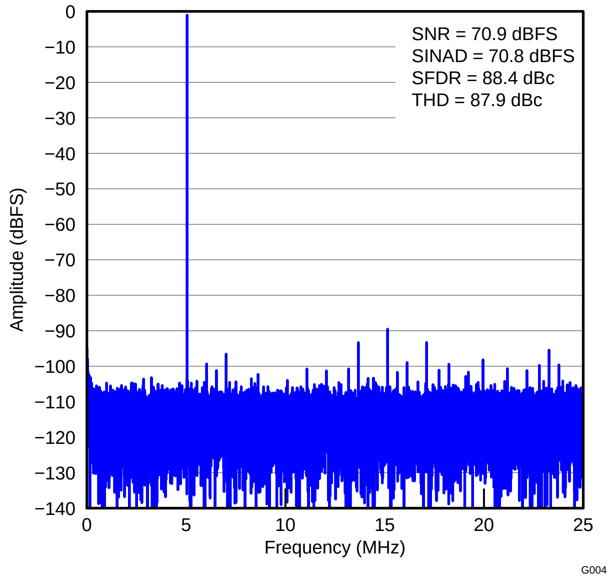



**Figure 7. FFT FOR 5-MHz INPUT SIGNAL (Sample Rate = 50 MSPS)**

## TYPICAL CHARACTERISTICS: General (continued)

Typical values are at $T_A$ = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, 100 MSPS, two-wire LVDS interface, and –1-dBFS differential analog input, unless otherwise noted.

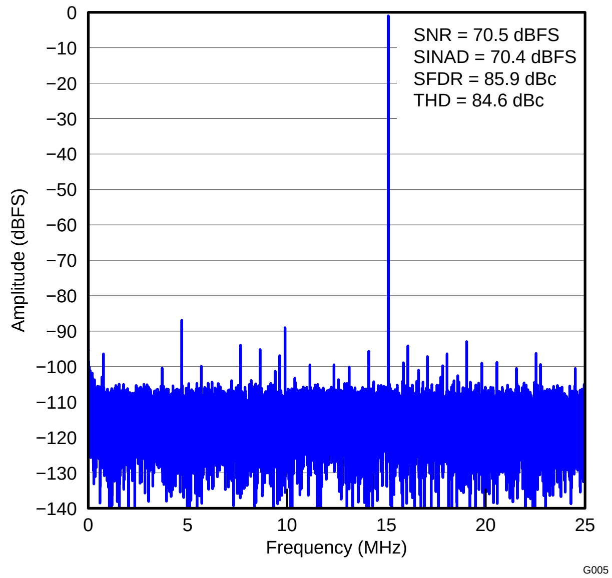



**Figure 8. FFT FOR 15-MHz INPUT SIGNAL (Sample Rate = 50 MSPS)**

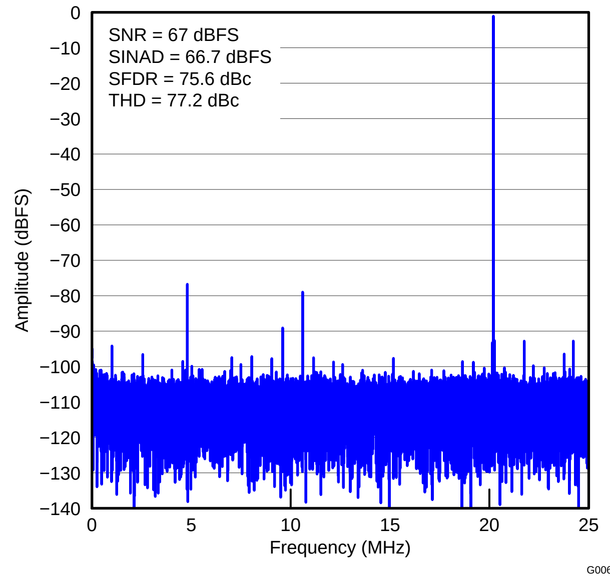



**Figure 9. FFT FOR 70-MHz INPUT SIGNAL (Sample Rate = 50 MSPS)**

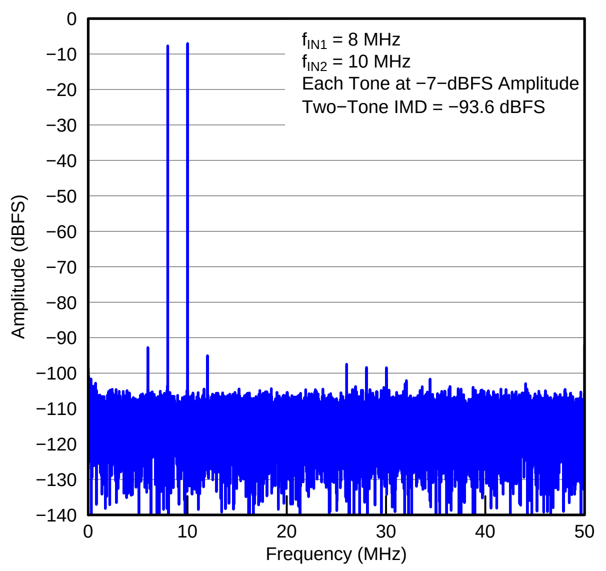



**Figure 10. FFT WITH TWO-TONE SIGNAL**

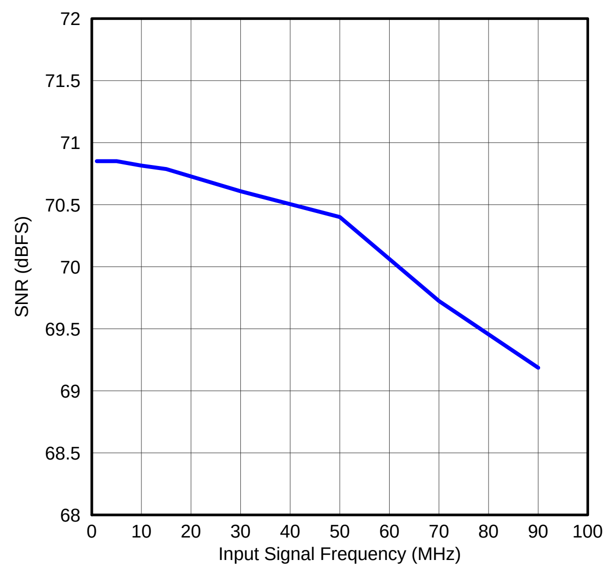



**Figure 11. SIGNAL-TO-NOISE RATIO vs INPUT SIGNAL FREQUENCY**

## TYPICAL CHARACTERISTICS: General (continued)

Typical values are at $T_A$ = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, 100 MSPS, two-wire LVDS interface, and –1-dBFS differential analog input, unless otherwise noted.

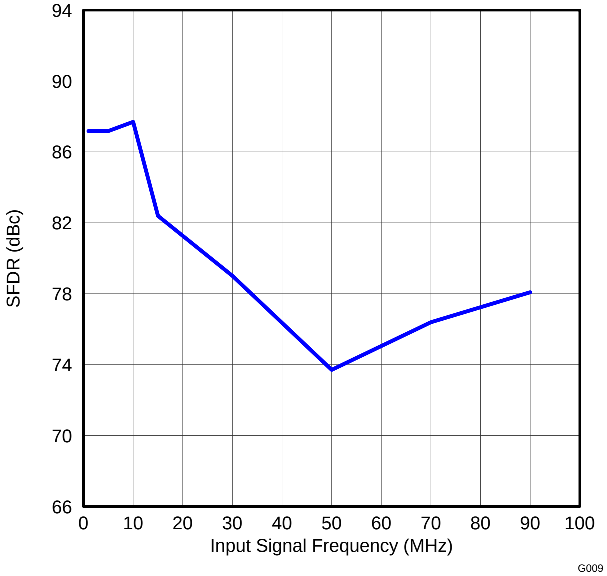



**Figure 12. SPURIOUS-FREE DYNAMIC RANGE vs INPUT SIGNAL FREQUENCY**

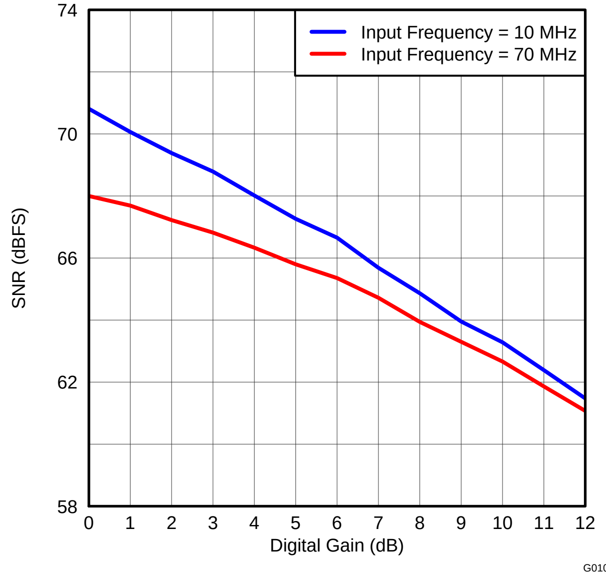



**Figure 13. SIGNAL-TO-NOISE RATIO vs DIGITAL GAIN**

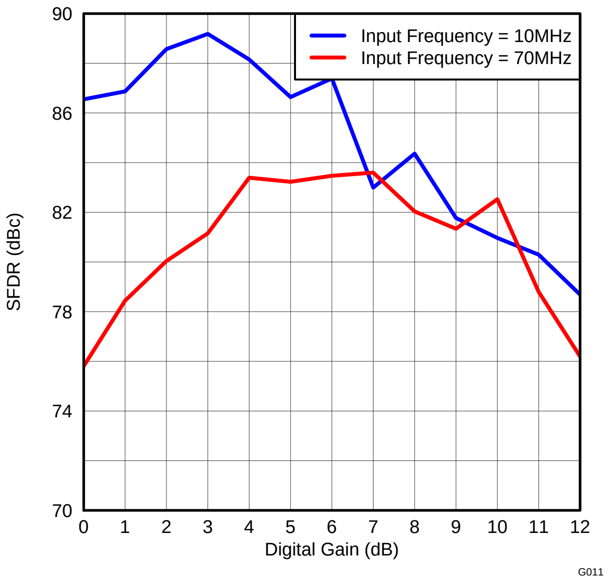



**Figure 14. SPURIOUS-FREE DYNAMIC RANGE vs DIGITAL GAIN**

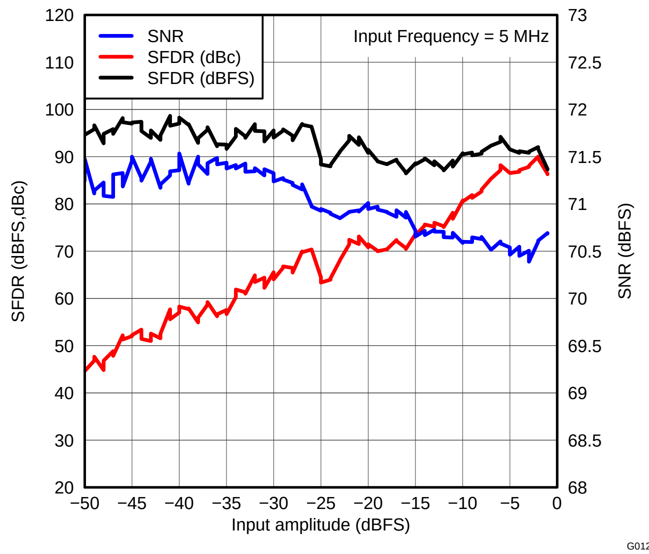



**Figure 15. PERFORMANCE vs INPUT AMPLITUDE**

## TYPICAL CHARACTERISTICS: General (continued)

Typical values are at $T_A$ = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, 100 MSPS, two-wire LVDS interface, and –1-dBFS differential analog input, unless otherwise noted.

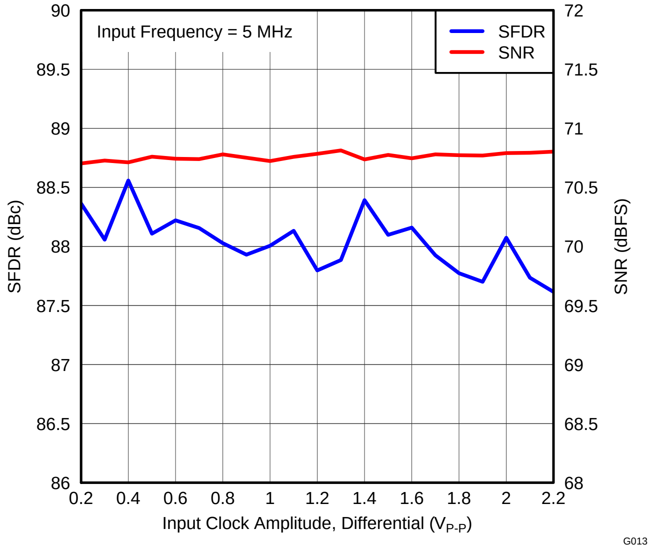



**Figure 16. PERFORMANCE vs INPUT CLOCK AMPLITUDE**

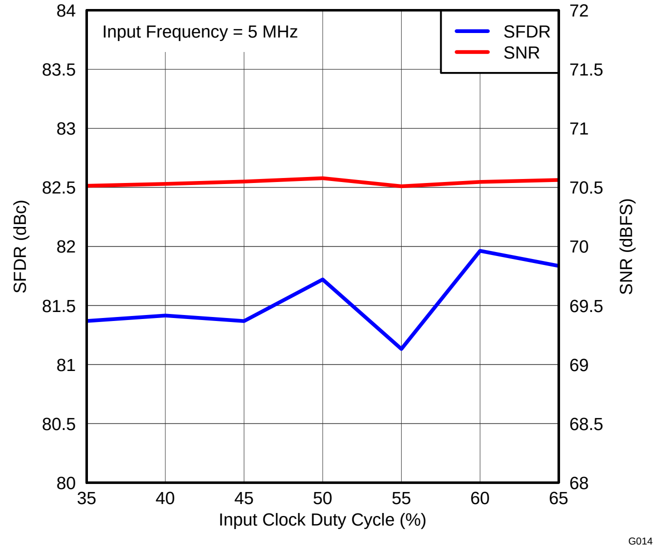



**Figure 17. PERFORMANCE vs INPUT CLOCK DUTY CYCLE**

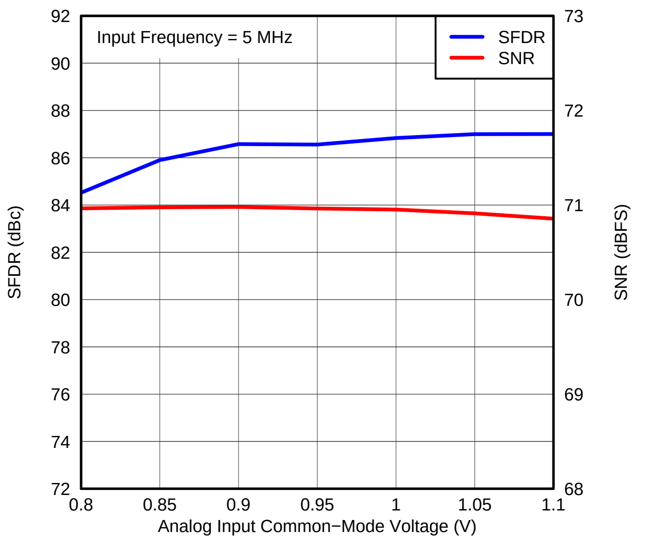



**Figure 18. PERFORMANCE vs INPUT COMMON-MODE VOLTAGE**

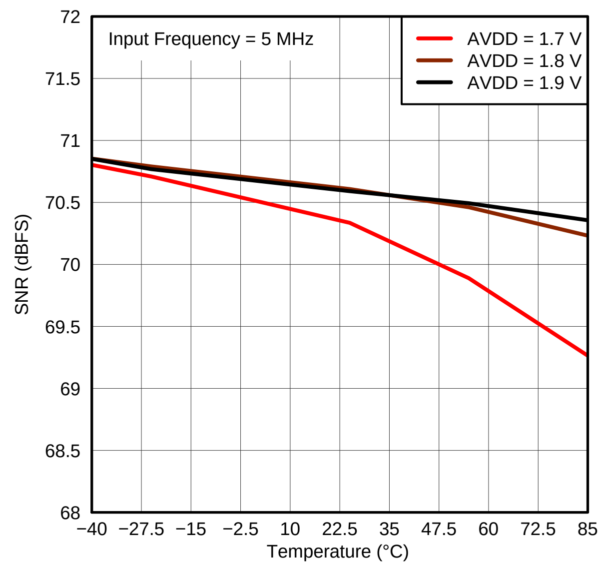



**Figure 19. SIGNAL-TO-NOISE RATIO vs AVDD AND TEMPERATURE**

## TYPICAL CHARACTERISTICS: General (continued)

Typical values are at $T_A$ = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, 100 MSPS, two-wire LVDS interface, and –1-dBFS differential analog input, unless otherwise noted.

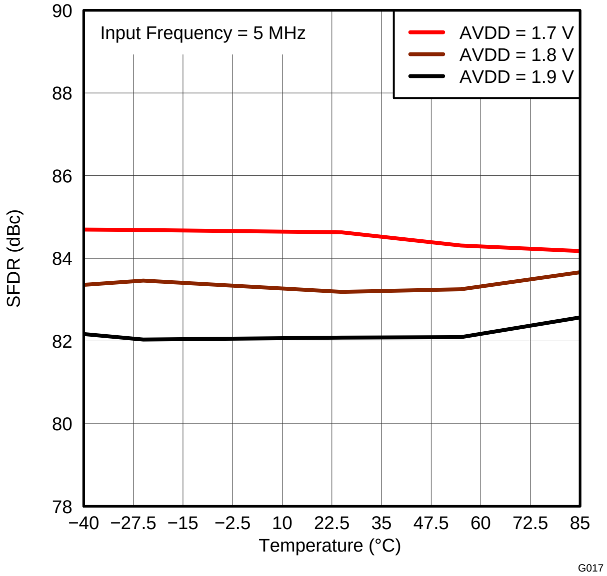



**Figure 20. SPURIOUS-FREE DYNAMIC RANGE vs AVDD AND TEMPERATURE**

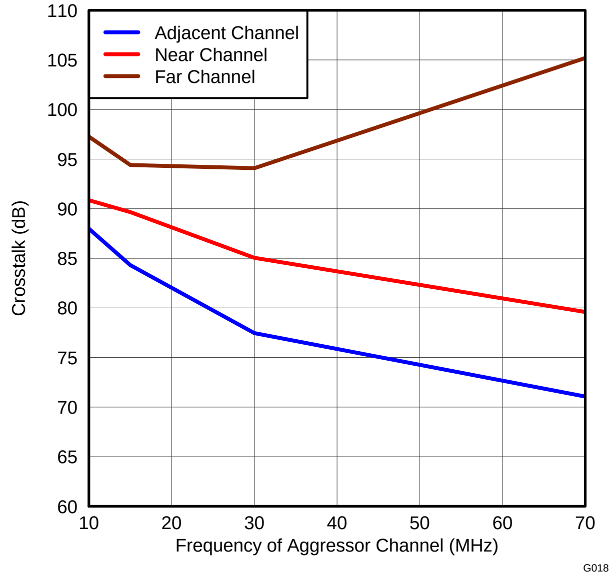



**Figure 21. CROSSTALK vs FREQUENCY** (1)

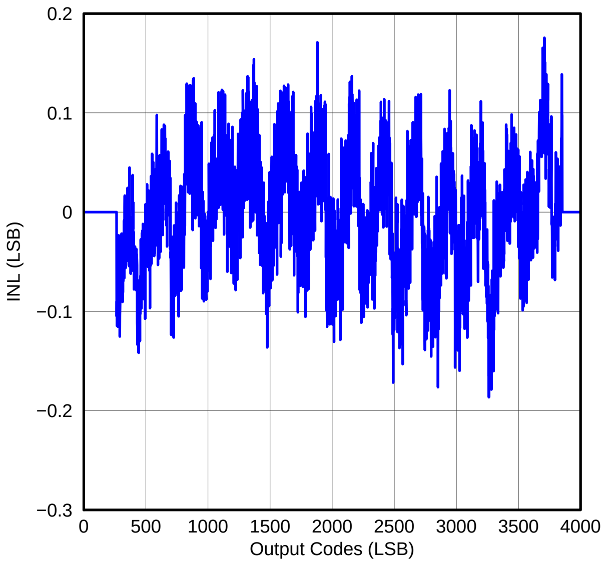



**Figure 22. INTEGRAL NONLINEARITY**

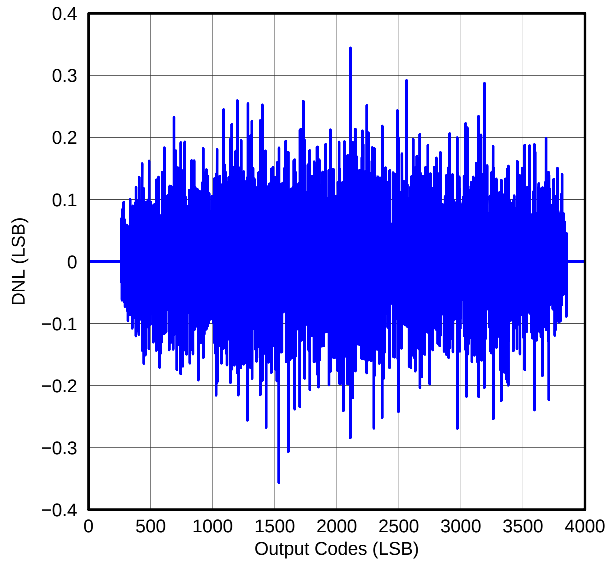



**Figure 23. DIFFERENTIAL NONLINEARITY**

(1) Adjacent channel: Neighboring channels on the immediate left and right of the channel of interest.
Near channel: Channels on the same side of the package, except the immediate neighbors.
Far channel: Channels on the opposite side of the package.

## TYPICAL CHARACTERISTICS: Digital Processing

Typical values are at $T_A$ = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, 100 MSPS, two-wire LVDS interface, and –1-dBFS differential analog input, unless otherwise noted.

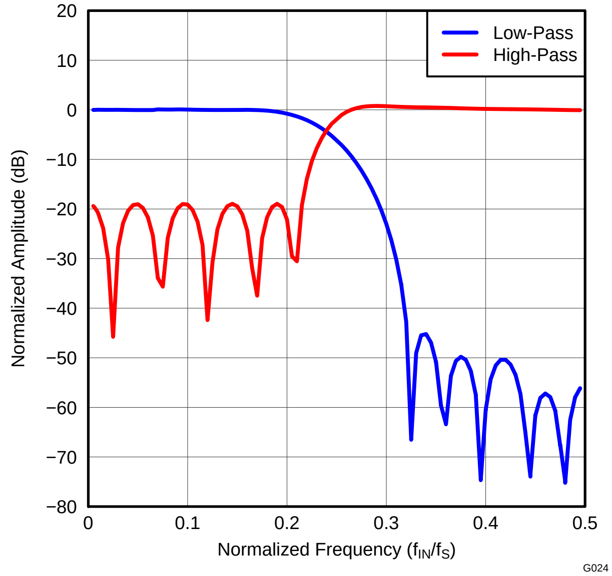



**Figure 24. DIGITAL FILTER RESPONSE (Decimate-by-2)**

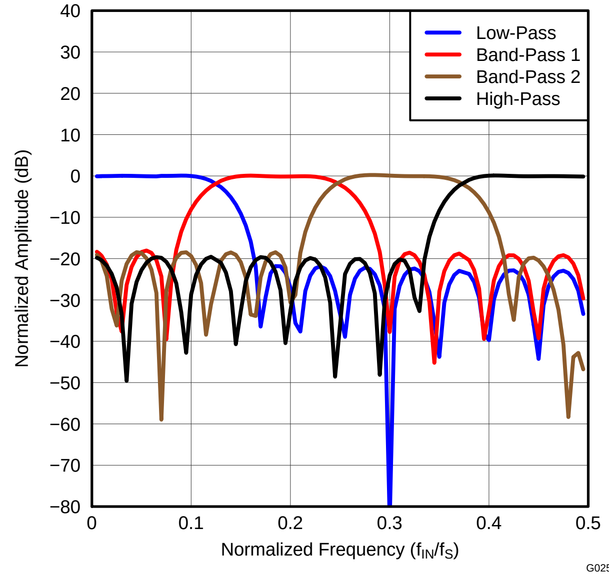



**Figure 25. DIGITAL FILTER RESPONSE (Decimate-by-4)**

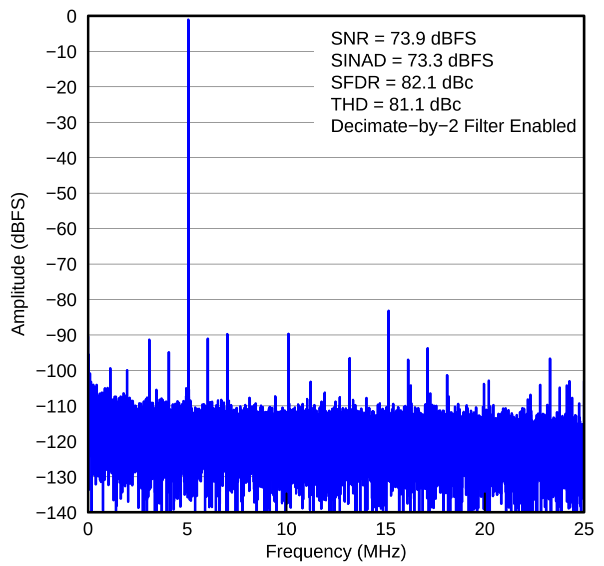



**Figure 26. FFT FOR 5-MHz INPUT SIGNAL (Sample Rate = 100 MSPS, Decimation Filter = 2)**

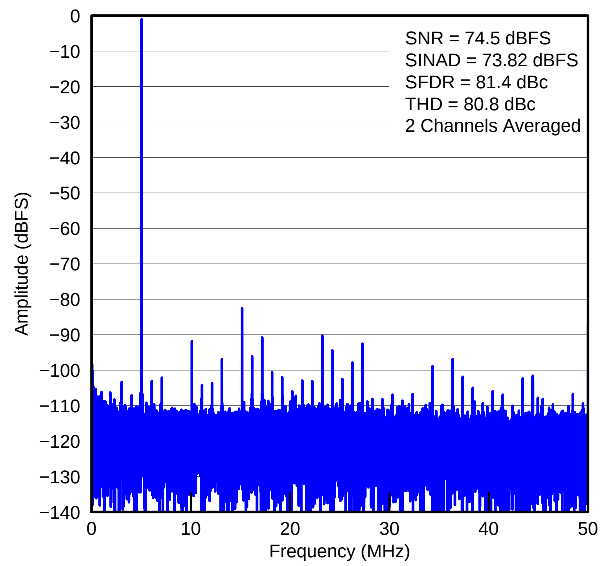



**Figure 27. FFT FOR 5-MHz INPUT SIGNAL (Sample Rate = 100 MSPS by Averaging Two Channels)**

## TYPICAL CHARACTERISTICS: Digital Processing (continued)

Typical values are at $T_A$ = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, 100 MSPS, two-wire LVDS interface, and –1-dBFS differential analog input, unless otherwise noted.

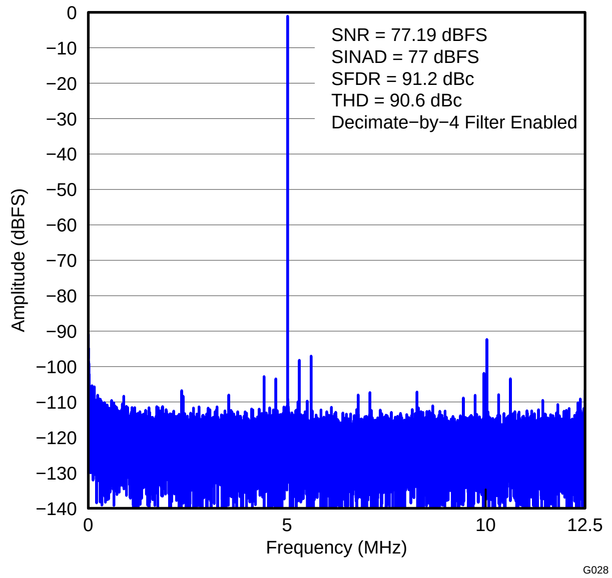



**Figure 28. FFT FOR 5-MHz INPUT SIGNAL (Sample Rate = 100 MSPS, Decimation Filter = 4)**

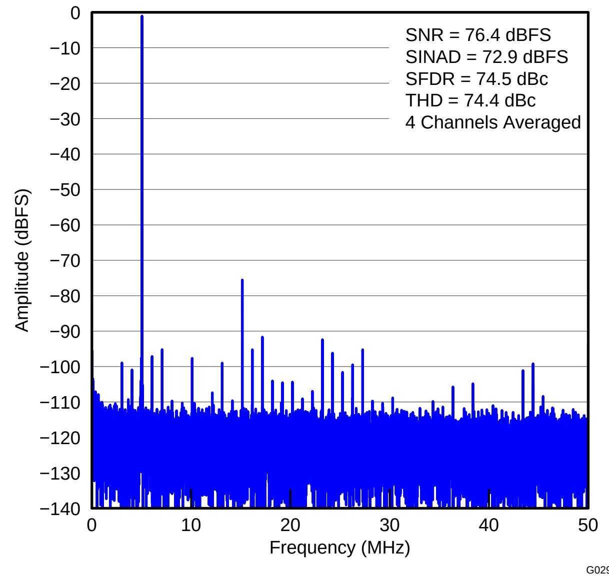



**Figure 29. FFT FOR 5-MHz INPUT SIGNAL (Sample Rate = 100 MSPS by Averaging Four Channels)**

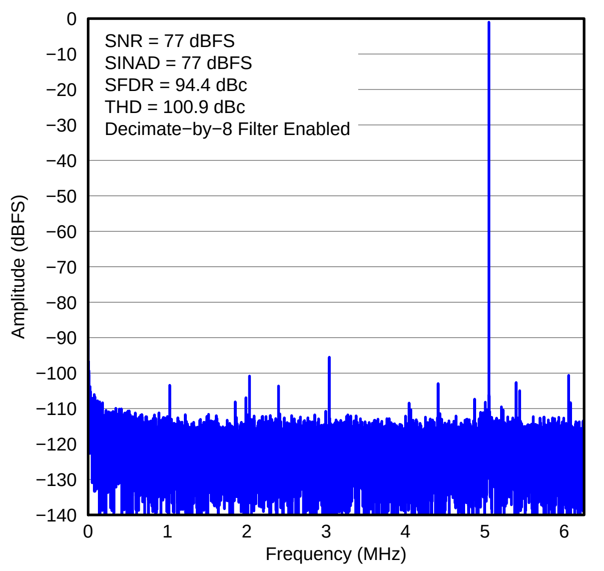



**Figure 30. FFT FOR 5-MHz INPUT SIGNAL USING CUSTOM DECIMATION-BY-8 FILTER**

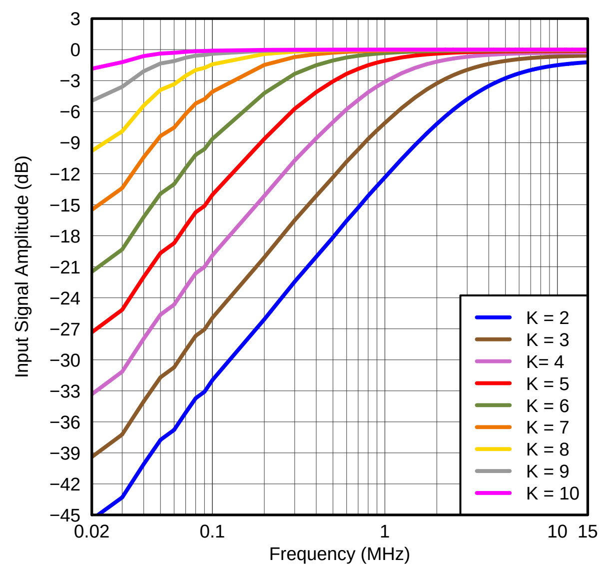



**Figure 31. DIGITAL HIGH-PASS FILTER RESPONSE**

## TYPICAL CHARACTERISTICS: Digital Processing (continued)

Typical values are at $T_A$ = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, 100 MSPS, two-wire LVDS interface, and –1-dBFS differential analog input, unless otherwise noted.

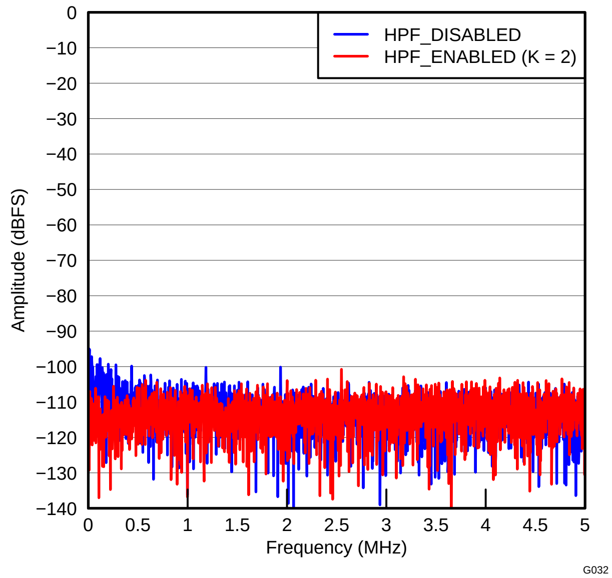



**Figure 32. FFT WITH HPF ENABLED AND DISABLED (No Signal)**

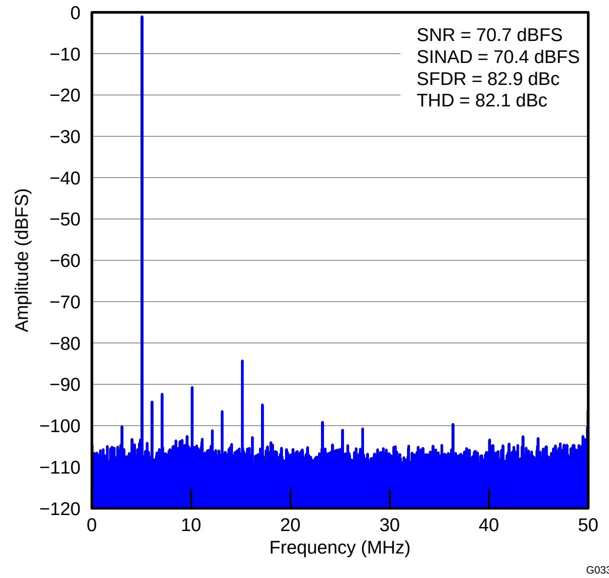



**Figure 33. FULL-BAND FFT, 5-MHz INPUT (100-MHz FS with LFNS Enabled)**

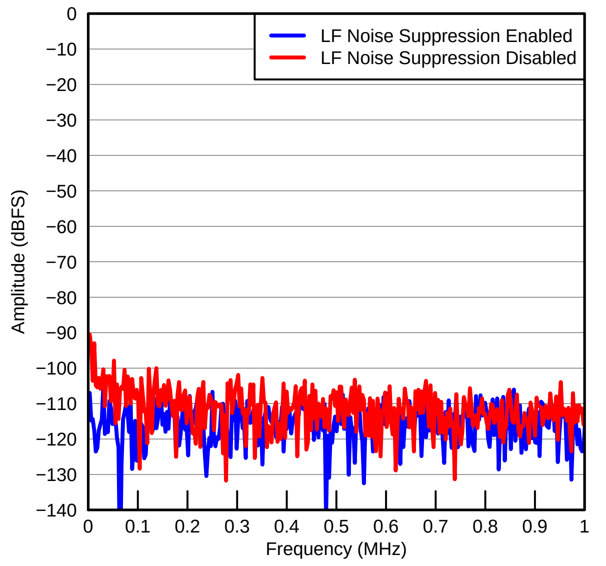



**Figure 34. 0-MHz to 1 MHz FFT, 5-MHz INPUT (100-MHz FS with LFNS Enabled)**

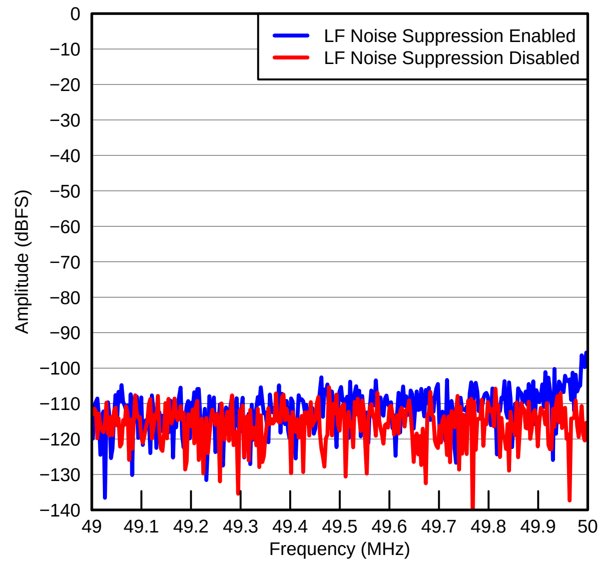



**Figure 35. 49-MHz to 50-MHz FFT, 5-MHz INPUT (100-MHz FS with LFNS Enabled)**

## TYPICAL CHARACTERISTICS: Power Consumption

Typical values are at $T_A$ = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, 100 MSPS, two-wire LVDS interface, and –1-dBFS differential analog input, unless otherwise noted.

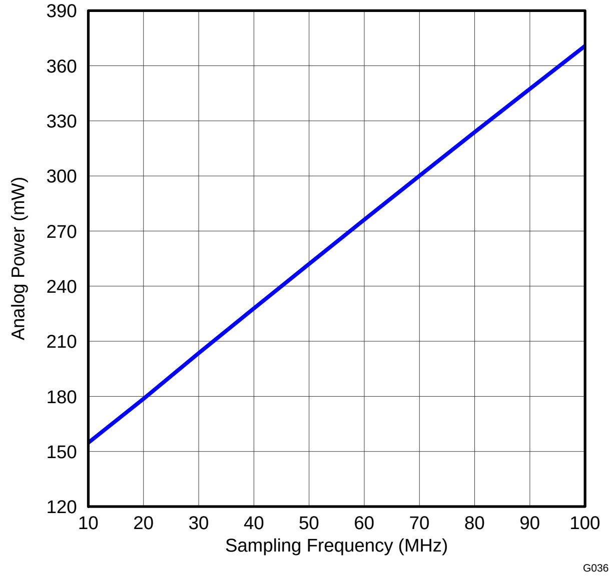



**Figure 36. ANALOG SUPPLY POWER**

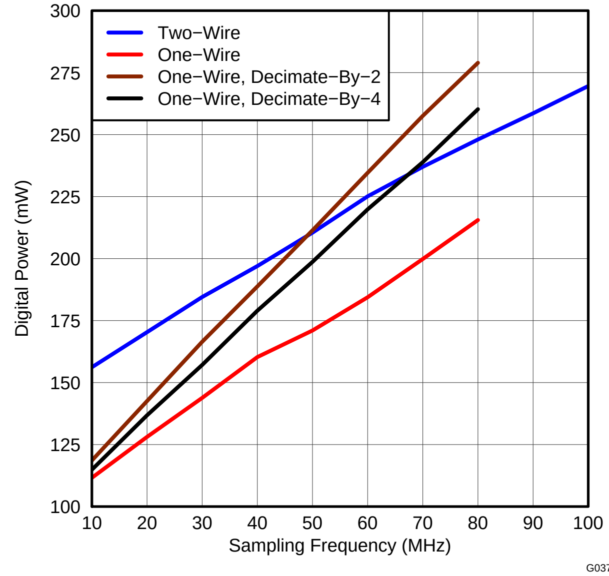



**Figure 37. DIGITAL SUPPLY POWER**

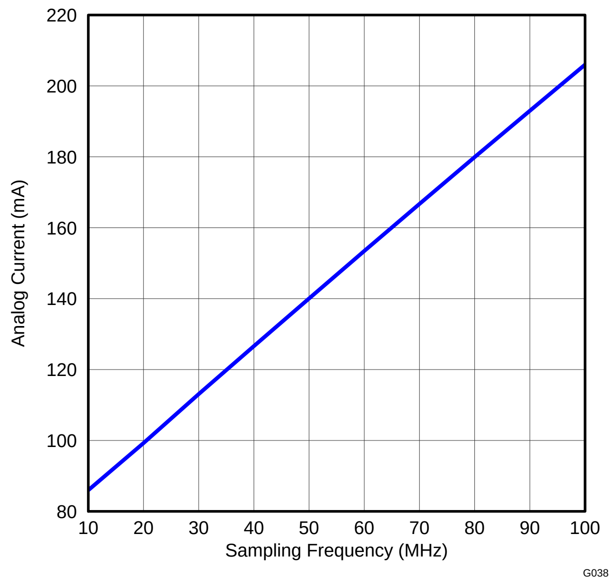



**Figure 38. ANALOG SUPPLY CURRENT**

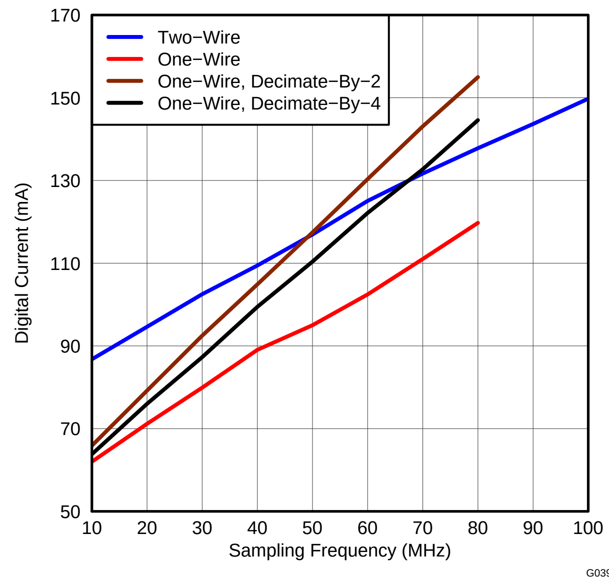



**Figure 39. DIGITAL SUPPLY CURRENT**

## TYPICAL CHARACTERISTICS: Power Consumption (continued)

Typical values are at $T_A$ = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, 100 MSPS, two-wire LVDS interface, and –1-dBFS differential analog input, unless otherwise noted.

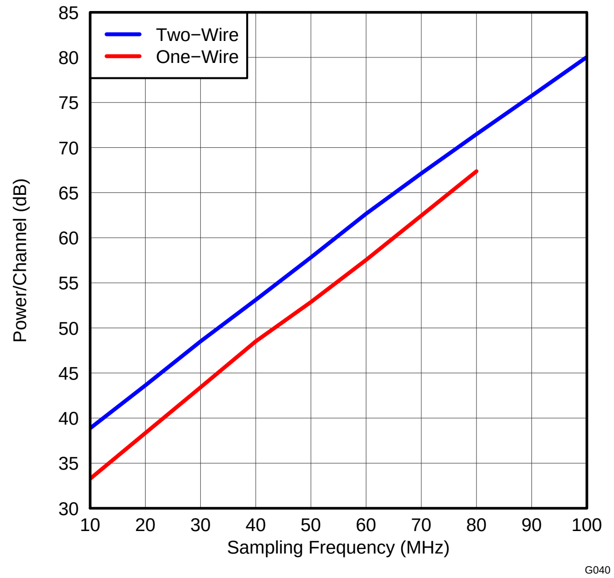



**Figure 40. TOTAL POWER PER CHANNEL**

## TYPICAL CHARACTERISTICS: Contour

Typical values are at $T_A$ = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, 100 MSPS, two-wire LVDS interface, and –1-dBFS differential analog input, unless otherwise noted.

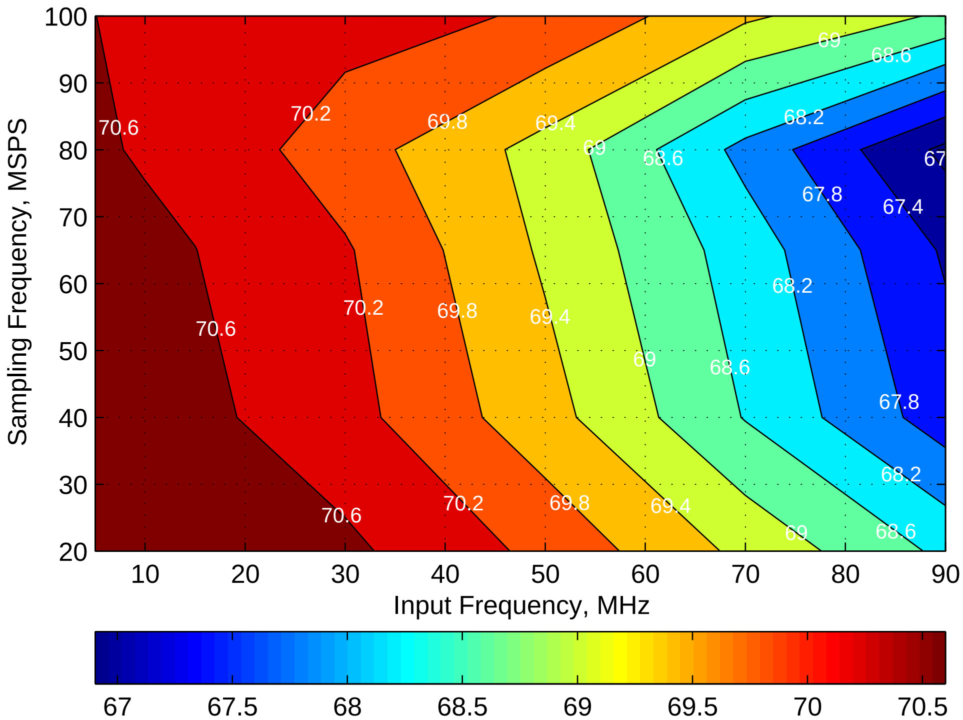



**Figure 41. SIGNAL-TO-NOISE RATIO vs INPUT AND SAMPLING FREQUENCIES**

## TYPICAL CHARACTERISTICS: Contour (continued)

Typical values are at $T_A$ = +25°C, AVDD = 1.8 V, LVDD = 1.8 V, 50% clock duty cycle, 100 MSPS, two-wire LVDS interface, and –1-dBFS differential analog input, unless otherwise noted.

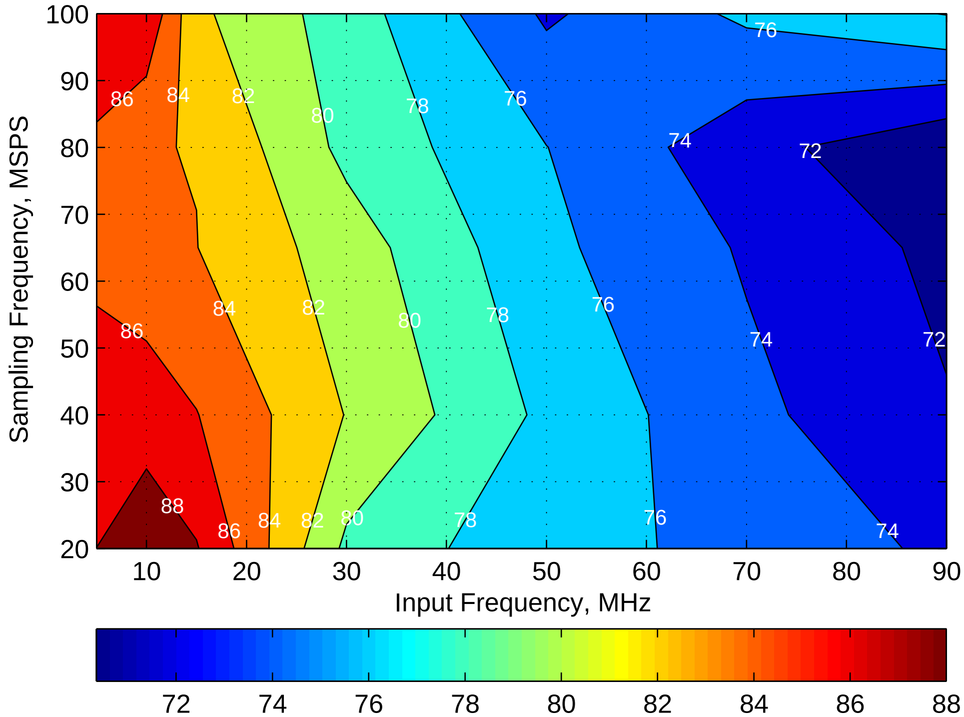



**Figure 42. SPURIOUS-FREE DYNAMIC RANGE vs INPUT AND SAMPLING FREQUENCIES**

# DEVICE CONFIGURATION

## SERIAL INTERFACE

The ADC has a set of internal registers that can be accessed by the serial interface formed by the $\overline{CS}$ (serial interface enable), SCLK (serial interface clock), and SDATA (serial interface data) pins. Serially shifting bits into the device is enabled when $\overline{CS}$ is low. The serial data (on the SDATA pin) are latched at every SCLK falling edge when $\overline{CS}$ is active (low). The serial data are loaded into the register at every 24th SCLK rising edge when $\overline{CS}$ is low. When the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active $\overline{CS}$ pulse. The first eight bits form the register address and the remaining 16 bits are the register data. The interface can function with SCLK frequencies from 15 MHz down to very low speeds (of a few hertz) and also with a non-50% SCLK duty cycle.

### Register Initialization

After power-up, the internal registers must be initialized to default values. This initialization can be accomplished in one of two ways:

1. Either through a hardware reset by applying a high pulse on the RESET pin (of widths greater than 10 ns), as shown in Figure 43; or
2. By applying a software reset. When using the serial interface, set the RESET bit (register 00h, bit D7) high. This setting initializes the internal registers to default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low (inactive).

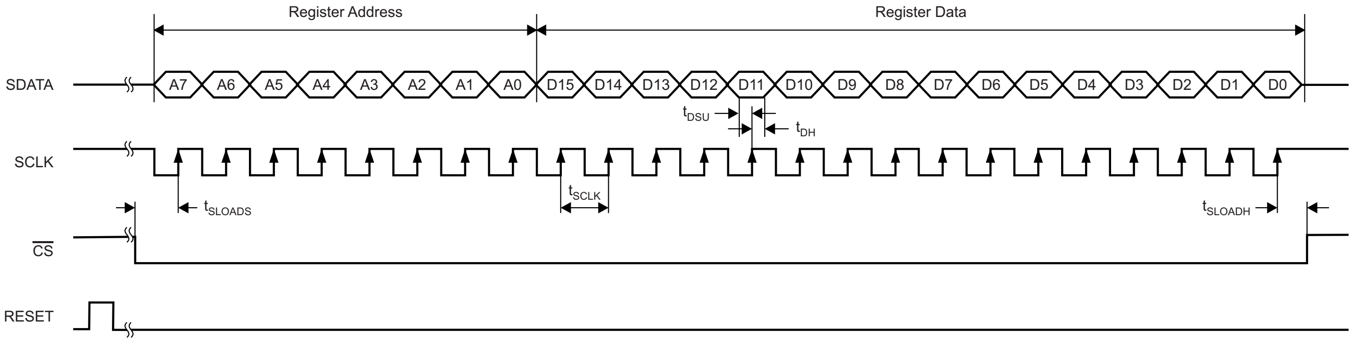



**Figure 43. Serial Interface Timing Diagram**

**Table 5. Timing Characteristics for Figure 43(1)**

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{SCLK}$ | SCLK frequency (equal to 1 / $t_{SCLK}$) | >dc | | 15 | MHz |
| $t_{SLOADS}$ | $\overline{CS}$ to SCLK setup time | 33 | | | ns |
| $t_{SLOADH}$ | SCLK to $\overline{CS}$ hold time | 33 | | | ns |
| $t_{DSU}$ | SDATA setup time | 33 | | | ns |
| $t_{DH}$ | SDATA hold time | 33 | | | ns |

(1) Typical values are at $T_A$ = +25°C, minimum and maximum values are across the full temperature range of $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, unless otherwise noted.

## Reset Timing

Figure 44 shows a timing diagram for the reset function.

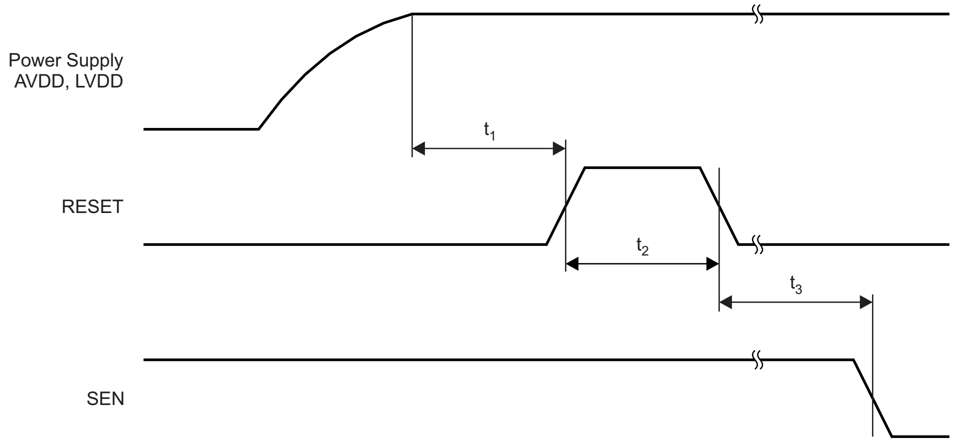



**Figure 44. Reset Timing Diagram**

**Table 6. Timing Characteristics for Figure 44**(1)(2)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_1$ | Power-on delay | Delay from AVDD and LVDD power-up to active RESET pulse | 1 | | | ms |
| $t_2$ | Reset pulse width | Pulse width of active RESET signal | 50 | | | ns |
| $t_3$ | Register write delay | Delay from RESET disable to $\overline{CS}$ active | | 100 | | ns |

(1) Typical values are at $T_A$ = +25°C, minimum and maximum values are across the full temperature range of $T_{MIN}$ = –40°C to $T_{MAX}$ = +85°C, unless otherwise noted.
(2) A high pulse on the RESET pin is required when initialization is done via a hardware reset.

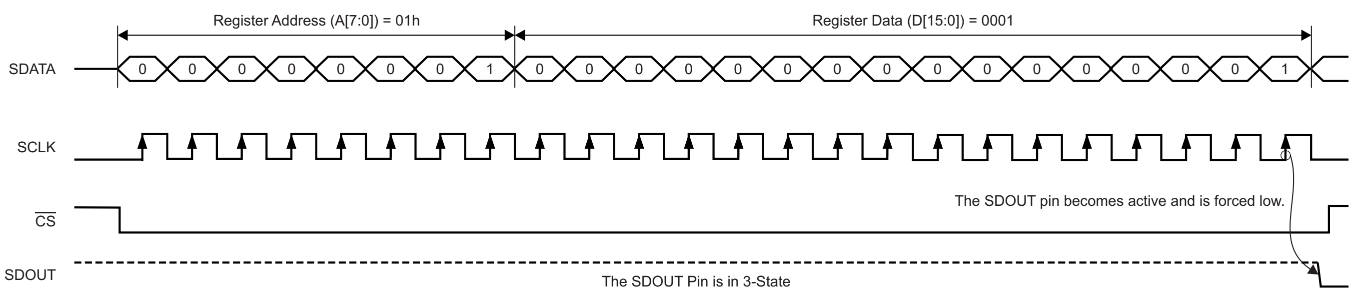
## Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back on the SDOUT pin. This readback mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

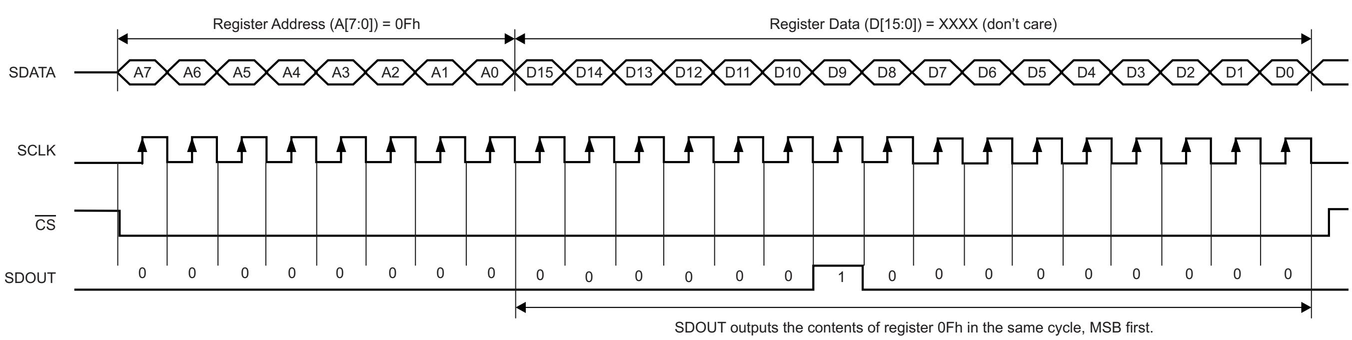
By default, the SDOUT pin is in 3-state after a device power-up or reset. When the readout mode is enabled using the READOUT register bit, SDOUT serially outputs the contents of the selected register. The following steps describe how to achieve this functionality:

1. Set the READOUT register bit to '1'. This setting puts the device in serial readout mode. This mode prevents any further writes to the internal registers, *except* for at register 01h. Note that the READOUT bit is also located in register 01h. The device can exit readout mode by setting the READOUT bit to '0'. Note that only the contents of register 01h are unable to be read in register readout mode.
2. Initiate a serial interface cycle specifying the address of the register (A[7:0]) whose content must be read.
3. The device serially outputs the contents (D[15:0]) of the selected register on the SDOUT pin.
4. The external controller can latch the contents at the SCLK rising edge.

To exit serial readout mode, reset the READOUT register bit to '0', which enables writes to all device registers. At this point, the SDOUT pin is in 3-state. A detailed timing diagram for the serial readout mode is shown in Figure 45.




a) Enable Serial Readout (READOUT = 1)




b) Read contents of register 0Fh. This register is initialized with 0200 (the device was previously put in global power-down).

**Figure 45. Serial Readout Timing Diagram**

## SERIAL INTERFACE REGISTERS MAP

Table 7 lists the ADS5295 registers.

### Table 7. Register Map

<table>
<tr><th>REGISTER ADDRESS (Hex)</th><th>D15</th><th>D14</th><th>D13</th><th>D12</th><th>D11</th><th>D10</th><th>D9</th><th>D8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>00</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>RST</td></tr>
<tr><td>01</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>EN_HIGH_ ADDRS</td><td>0</td><td>0</td><td>0</td><td>EN_ READOUT</td></tr>
<tr><td>0A</td><td colspan="16">RAMP_PAT_RESET_VAL</td></tr>
<tr><td>0F</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>PDN_PIN_ CFG</td><td>PDN_ COMPLETE</td><td>PDN_ PARTIAL</td><td colspan="8">PDN_CH[8:1]</td></tr>
<tr><td>14</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="8">LFNS_CH[8:1]</td></tr>
<tr><td>1C</td><td>0</td><td>EN_FRAME _PAT</td><td>0</td><td>0</td><td colspan="12">ADCLKOUT[11:0]</td></tr>
<tr><td>23</td><td colspan="16">PRBS_SEED[15:0]</td></tr>
<tr><td>24</td><td colspan="7">PRBS_SEED[22:16]</td><td>0</td><td colspan="8">INVERT_CH[8:1]</td></tr>
<tr><td>25</td><td>TP_HARD_ SYNC</td><td>PRBS_ SEED_ FROM_REG</td><td>PRBS_ MODE_2</td><td>PRBS_ TP_EN</td><td>0</td><td>0</td><td>0</td><td>TP_SOFT_ SYNC</td><td>0</td><td colspan="3">TEST_PATT[2:0]</td><td colspan="2">BITS_CUSTOM2[11:10]</td><td colspan="2">BITS_CUSTOM1[11:10]</td></tr>
<tr><td>26</td><td colspan="10">BITS_CUSTOM1[9:0]</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>27</td><td colspan="10">BITS_CUSTOM2[9:0]</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>28</td><td>EN_WORD _BIT_WISE</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>EN_BIT _WISE</td><td colspan="8">EN_WORDWISE_BY_CH[7:0]</td></tr>
<tr><td>29</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>EN_DIG_ FILTER</td><td>EN_ CHANNEL_ AVG</td></tr>
<tr><td>2A</td><td colspan="4">GAIN_CH4[3:0]</td><td colspan="4">GAIN_CH3[3:0]</td><td colspan="4">GAIN_CH2[3:0]</td><td colspan="4">GAIN_CH1[3:0]</td></tr>
<tr><td>2B</td><td colspan="4">GAIN_CH5[3:0]</td><td colspan="4">GAIN_CH6[3:0]</td><td colspan="4">GAIN_CH7[3:0]</td><td colspan="4">GAIN_CH8[3:0]</td></tr>
<tr><td>2C</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">AVG_OUT4[1:0]</td><td>0</td><td colspan="2">AVG_OUT3[1:0]</td><td>0</td><td colspan="2">AVG_OUT2[1:0]</td><td>0</td><td colspan="2">AVG_OUT1[1:0]</td></tr>
<tr><td>2D</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">AVG_OUT8[1:0]</td><td>0</td><td colspan="2">AVG_OUT7[1:0]</td><td>0</td><td colspan="2">AVG_OUT6[1:0]</td><td>0</td><td colspan="2">AVG_OUT5[1:0]</td></tr>
<tr><td>2E</td><td>0</td><td>HPF_EN_ CH1</td><td colspan="4">HPF_CORNER_CH1[3:0]</td><td colspan="3">FILTER_TYPE_CH1[2:0]</td><td colspan="3">DEC_RATE_CH1</td><td>0</td><td>SEL_ODD_ TAP_CH1</td><td>0</td><td>USE_ FILTER_ CH1</td></tr>
<tr><td>2F</td><td>0</td><td>HPF_EN_ CH2</td><td colspan="4">HPF_CORNER_CH2[3:0]</td><td colspan="3">FILTER_TYPE_CH2[2:0]</td><td colspan="3">DEC_RATE_CH2</td><td>0</td><td>SEL_ODD_ TAP_CH2</td><td>0</td><td>USE_ FILTER_ CH2</td></tr>
<tr><td>30</td><td>0</td><td>HPF_EN_ CH3</td><td colspan="4">HPF_CORNER_CH3[3:0]</td><td colspan="3">FILTER_TYPE_CH3[2:0]</td><td colspan="3">DEC_RATE_CH3</td><td>0</td><td>SEL_ODD_ TAP_CH3</td><td>0</td><td>USE_ FILTER_ CH3</td></tr>
<tr><td>31</td><td>0</td><td>HPF_EN_ CH4</td><td colspan="4">HPF_CORNER_CH4[3:0]</td><td colspan="3">FILTER_TYPE_CH4[2:0]</td><td colspan="3">DEC_RATE_CH4</td><td>0</td><td>SEL_ODD_ TAP_CH4</td><td>0</td><td>USE_ FILTER_ CH4</td></tr>
<tr><td>32</td><td>0</td><td>HPF_EN_ CH5</td><td colspan="4">HPF_CORNER_CH5[3:0]</td><td colspan="3">FILTER_TYPE_CH5[2:0]</td><td colspan="3">DEC_RATE_CH5</td><td>0</td><td>SEL_ODD_ TAP_CH5</td><td>0</td><td>USE_ FILTER_ CH5</td></tr>
<tr><td>33</td><td>0</td><td>HPF_EN_ CH6</td><td colspan="4">HPF_CORNER_CH6[3:0]</td><td colspan="3">FILTER_TYPE_CH6[2:0]</td><td colspan="3">DEC_RATE_CH6</td><td>0</td><td>SEL_ODD_ TAP_CH6</td><td>0</td><td>USE_ FILTER_ CH6</td></tr>
</table>

### Table 7. Register Map (continued)

| REGISTER ADDRESS (Hex) | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 34 | 0 | HPF_EN_CH7 | HPF_CORNER_CH7[3:0] | | | | FILTER_TYPE_CH7[2:0] | | | DEC_RATE_CH7 | | | 0 | SEL_ODD_TAP_CH7 | 0 | USE_FILTER_CH7 |
| 35 | 0 | HPF_EN_CH8 | HPF_CORNER_CH8[3:0] | | | | FILTER_TYPE_CH8[2:0] | | | DEC_RATE_CH8 | | | 0 | SEL_ODD_TAP_CH8 | 0 | USE_FILTER_CH8 |
| 38 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DATA_RATE[1:0] | |
| 42 | EN_PHASE DDR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PHASE_DDR1 | PHASE_DDR0 | 0 | 0 | 0 | 0 | 0 |
| 45 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PAT_DESKEW_SYNC[1:0] | |
| 46 | ENABLE 46 | 0 | FALL_SDR | 0 | BIT_SER_SEL | | | | 0 | 0 | 0 | EN_SDR | EN_MSB_FIRST | BTC_MODE | 0 | EN_2WIRE |
| 50 | ENABLE 50 | 0 | 0 | 0 | MAP_Ch1234_to_OUT2A | | | | MAP_Ch1234_to_OUT1B | | | | MAP_Ch1234_to_OUT1A | | | |
| 51 | ENABLE 51 | 0 | 0 | 0 | MAP_Ch1234_to_OUT3B | | | | MAP_Ch1234_to_OUT3A | | | | MAP_Ch1234_to_OUT2B | | | |
| 52 | ENABLE 52 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MAP_Ch1234_to_OUT4B | | | | MAP_Ch1234_to_OUT4A | | | |
| 53 | ENABLE 53 | 0 | 0 | 0 | MAP_Ch5678_to_OUT6B | | | | MAP_Ch5678_to_OUT5A | | | | MAP_Ch5678_to_OUT5B | | | |
| 54 | ENABLE 54 | 0 | 0 | 0 | MAP_Ch5678_to_OUT7A | | | | MAP_Ch5678_to_OUT7B | | | | MAP_Ch5678_to_OUT6A | | | |
| 55 | ENABLE 55 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MAP_Ch5678_to_OUT8A | | | | MAP_Ch5678_to_OUT8B | | | |
| 5A to 65 | EN_CUSTOM_FILT_CH1 | 0 | 0 | 0 | COEFF*n*_SET_CH1(1) | | | | | | | | | | | |
| 66 to 71 | EN_CUSTOM_FILT_CH2 | 0 | 0 | 0 | COEFF*n*_SET_CH2(1) | | | | | | | | | | | |
| 72 to 7D | EN_CUSTOM_FILT_CH3 | 0 | 0 | 0 | COEFF*n*_SET_CH3(1) | | | | | | | | | | | |
| 7E to 89 | EN_CUSTOM_FILT_CH4 | 0 | 0 | 0 | COEFF*n*_SET_CH4(1) | | | | | | | | | | | |
| 8A to 95 | EN_CUSTOM_FILT_CH5 | 0 | 0 | 0 | COEFF*n*_SET_CH5(1) | | | | | | | | | | | |
| 96 to A1 | EN_CUSTOM_FILT_CH6 | 0 | 0 | 0 | COEFF*n*_SET_CH6(1) | | | | | | | | | | | |
| A2 to AD | EN_CUSTOM_FILT_CH7 | 0 | 0 | 0 | COEFF*n*_SET_CH7(1) | | | | | | | | | | | |
| AE to B9 | EN_CUSTOM_FILT_CH8 | 0 | 0 | 0 | COEFF*n*_SET_CH8(1) | | | | | | | | | | | |
| BE | EN_LVDS_PROG | 0 | 0 | 0 | 0 | 0 | DELAY_DATA_R | | DELAY_LCLK_R | | | DELAY_DATA_F | | DELAY_LCLK_F | | |
| F0 | EN_EXT_REF | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

(1) n = 0 to 11.

## DESCRIPTION OF SERIAL INTERFACE REGISTERS

### Register 00h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | RST |

**Bits D[15:1]** **Must write '0'**

**Bit D0** **RST**

0 = Normal operation (default)
1 = Self-clearing software RESET; after reset, this bit is set to '0'

### Register 01h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | EN_HIGH_ ADDRS | 0 | 0 | 0 | EN_READOUT |

**Bits D[15:5]** **Must write '0'**

**Bit D4** **EN_HIGH_ADDRS**

0 = Access to register F0h disabled (default)
1 = Access to register F0h enabled

**Bits D[3:1]** **Must write '0'**

**Bit D0** **EN_READOUT**

0 = Normal operation (default)
1 = READOUT of registers mode using the SDOUT pin enabled

### Register 0Ah

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| RAMP_PAT_RESET_VAL | | | | | | | |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| RAMP_PAT_RESET_VAL | | | | | | | |

**Bits D[15:0]** **RAMP_PAT_RESET_VAL**

The starting value of digital ramp test pattern can be programmed using these register bits. By default, after a reset, the starting value is 0000h.

### Register 0Fh

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | PDN_PIN_CFG | PDN_COMPLETE | PDN_PARTIAL |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| PDN_CH[8:1] | | | | | | | |

All bits default to '0' after reset.

**Bits D[15:11]** **Must write '0'**

**Bit D10** **PDN_PIN_CFG**

0 = PD pin configured for complete power-down mode
1 = PD pin configured for partial power-down mode

**Bit D9** **PDN_COMPLETE**

0 = Normal operation
1 = Register mode for complete power-down; slow recovery from power-down

**Bit D8** **PDN_PARTIAL**

0 = Normal operation
1 = Partial power-down mode; fast recovery from power-down

**Bits D[7:0]** **PDN_CH[8:1]**

0 = Normal operation
1 = Individual channel ADC power-down mode

### Register 14h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| LFNS_CH[8:1] | | | | | | | |

**Bits D[15:8]** **Must write '0'**

**Bits D[7:0]** **LFNS_CH[8:1]**

0 = LFNS disabled (default)
1 = Low-frequency noise suppression (LFNS) mode enabled for individual channels

### Register 1Ch

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| 0 | EN_FRAME_PAT | 0 | 0 | ADCLKOUT[11:0] | | | |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| ADCLKOUT[11:0] | | | | | | | |

All bits default to '0' after reset.

**Bit D15** **Must write '0'**

**Bit D14** **EN_FRAME_PAT**

0 = Normal operation on frame clock (default)
1 = Enables output frame clock to be programmed through a pattern specified by ADCCLKOUT register bits

**Bits D[13:12]** **Must write '0'**

**Bits D[11:0]** **ADCLKOUT[11:0]**

These bits create the 12-bit pattern for the frame clock on the ADCLKP, ADCLKN pins.

### Register 23h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| PRBS_SEED[15:0] | | | | | | | |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| PRBS_SEED[15:0] | | | | | | | |

**Bits D[15:0]** **PRBS_SEED[15:0]**

These bits are the lower 16 bits of the PRBS pattern starting seed value.

The starting seed value of the PRBS test pattern can be specified using these register bits

### Register 24h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| PRBS_SEED[22:16] | | | | | | | 0 |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| INVERT_CH[8:1] | | | | | | | |

All bits default to '0' after reset.

**Bits D[15:9]** **PRBS_SEED[22:16]**

These bits are the seven upper bits of the PRBS seed starting value.

**Bit D8** **Must write '0'**

**Bits D[7:0]** **INVERT_CH[8:1]**

0 = Normal configuration
Normally, the INP pin represents the positive analog input pin and INN represents the complementary negative input.

1 = The polarity of the analog input pins is electrically swapped
Setting the INVERT_CH[8:1] bits causes the inputs to be swapped. INN now represents the positive input and INP represents the negative input.

### Register 25h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| TP_HARD_ SYNC | PRBS_SEED_ FROM_REG | PRBS_ MODE_2 | PRBS_TP_EN | 0 | 0 | 0 | TP_SOFT_ SYNC |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 0 | TEST_PATT[2:0] | | | BITS_CUSTOM2[11:10] | | BITS_CUSTOM1[11:10] | |

All bits default to '0' after reset.

**Bit D15** **TP_HARD_SYNC**

0 = Inactive
1 = The external SYNC feature is enabled for syncing test patterns

**Bit D14** **PRBS_SEED_FROM_REG**

0 = Disabled
1 = The PRBS seed is now able to be chosen from registers 23h and 24h

**Bit D13** **PRBS_MODE_2**

The PRBS 9-bit LFSR (23-bit LFSR) is the default mode.

**Bit D12** **PRBS_TP_EN**

0 = PRBS test pattern disabled
1 = PRBS test pattern enabled

**Bits D[11:9]** **Must write '0'**

**Bit D8** **TP_SOFT_SYNC**

0 = No sync
1 = Software sync bit for the test patterns on all eight channels

**Bit D7** **Must write '0'**

**Bit D6** **TEST_PATT2**

0 = Normal operation
1 = A repeating full-scale ramp pattern is enabled on the outputs; ensure that bits D4 and D5 are '0'

**Bit D5** **TEST_PATT1**

0 = Normal operation
1 = Enables a mode where the output toggles between two defined codes; ensure that bits D4 and D6 are '0'

**Bit D4** **TEST_PATT0**

0 = Normal operation
1 = Enables a mode where the output is a constant specified code; ensure that bits D5 and D6 are '0'

**Bits D[3:2]** **BITS_CUSTOM2[11:10]**

These bits are the two MSBs for the second code of the dual custom patterns.

**Bits D[1:0]** **BITS_CUSTOM1[11:10]**

These bits are the two MSBs for the single custom pattern (and for the first code of the dual custom patterns).

### Register 26h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| BITS_CUSTOM1[9:0] | | | | | | | |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| BITS_CUSTOM1[9:0] | | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits D[15:6]** **BITS_CUSTOM1[9:0]**

These bits are the 10 lower bits for the single custom pattern (and for the first code of the dual custom pattern).

**Bits D[5:0]** **Must write '0'**

### Register 27h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| BITS_CUSTOM2[9:0] | | | | | | | |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| BITS_CUSTOM2[9:0] | | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits D[15:6]** **BITS_CUSTOM2[9:0]**

These bits are the 10 lower bits for the second code of the dual custom pattern.

**Bits D[5:0]** **Must write '0'**

### Register 28h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| EN_WORD_ BIT_WISE | 0 | 0 | 0 | 0 | 0 | 0 | EN_BIT_WISE |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| EN_WORDWISE_BY_CH[7:0] | | | | | | | |

All bits default to '0' after reset.

**Bit D15** **EN_WORD_BIT_WISE**

This bit enables the bit order output in two-wire mode.
0 = Byte-wise
1 = Word-wise if D[7:0] = 1 (bit-wise if D8 = 1 and D[7:0] = 0)

**Bits D[14:9]** **Must write '0'**

**Bit D8** **EN_BIT_WISE**

1 = Bit-wise if D15 =1 and D[7:0] = 0

**Bits D[7:0]** **EN_WORDWISE_BY_CH[7:0]**

0 = Bit-wise if D15 = 1 and D8 = 1
1 = Word-wise if D15 = 1

### Register 29h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | EN_DIG_ FILTER | EN_CHANNEL _AVG |

**Bits D[15:2]** **Must write '0'**

**Bit D1** **EN_DIG_FILTER**

0 = Global control digital filter disabled(default)
1 = Global control digital filter enabled

**Bit D0** **EN_CHANNEL_AVG**

0 = Channel averaging is disabled (default)
1 = Channel averaging is enabled and specified by the AVG_OUT*n* register bits

### Register 2Ah

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| GAIN_CH4[3:0] | | | | GAIN_CH3[3:0] | | | |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| GAIN_CH2[3:0] | | | | GAIN_CH1[3:0] | | | |

**Bits D[15:12]** **GAIN_CH4[3:0]**

These bits set the programmable gain for channel 4.

**Bits D[11:8]** **GAIN_CH3[3:0]**

These bits set the programmable gain for channel 3.

**Bits D[7:4]** **GAIN_CH2[3:0]**

These bits set the programmable gain for channel 2.

**Bits D[3:0]** **GAIN_CH1[3:0]**

These bits set the programmable gain for channel 1.

### Register 2Bh

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| GAIN_CH5[3:0] | | | | GAIN_CH6[3:0] | | | |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| GAIN_CH7[3:0] | | | | GAIN_CH8[3:0] | | | |

**Bits D[15:12]** **GAIN_CH5[3:0]**

These bits set the programmable gain for channel 5.

**Bits D[11:8]** **GAIN_CH6[3:0]**

These bits set the programmable gain for channel 6.

**Bits D[7:4]** **GAIN_CH7[3:0]**

These bits set the programmable gain for channel 7.

**Bits D[3:0]** **GAIN_CH8[3:0]**

These bits set the programmable gain for channel 8.

### Register 2Ch

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | AVG_OUT4[1:0] | | 0 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| AVG_OUT3[1:0] | | 0 | AVG_OUT2[1:0] | | 0 | AVG_OUT1[1:0] | |

**Bits D[15:11]** **Must write '0'**

**Bits D[10:9]** **AVG_OUT4[1:0]**

These bits set the averaging control for what is transmitted on the LVDS output OUT4.

**Bit D8** **Must write '0'**

**Bits D[7:6]** **AVG_OUT3[1:0]**

These bits set the averaging control for what is transmitted on the LVDS output OUT3.

**Bit D5** **Must write '0'**

**Bits D[4:3]** **AVG_OUT2[1:0]**

These bits set the averaging control for what is transmitted on the LVDS output OUT2.

**Bit D2** **Must write '0'**

**Bits D[1:0]** **AVG_OUT1[1:0]**

These bits set the averaging control for what is transmitted on the LVDS output OUT1.

### Register 2Dh

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | AVG_OUT8[1:0] | | 0 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| AVG_OUT7[1:0] | | 0 | AVG_OUT6[1:0] | | 0 | AVG_OUT5[1:0] | |

**Bits D[15:11]** **Must write '0'**

**Bits D[10:9]** **AVG_OUT8[1:0]**

These bits set the averaging control for what is transmitted on the LVDS output OUT8.

**Bit D8** **Must write '0'**

**Bits D[7:6]** **AVG_OUT7[1:0]**

These bits set the averaging control for what is transmitted on the LVDS output OUT7.

**Bit D5** **Must write '0'**

**Bits D[4:3]** **AVG_OUT6[1:0]**

These bits set the averaging control for what is transmitted on the LVDS output OUT6.

**Bit D2** **Must write '0'**

**Bits D[1:0]** **AVG_OUT5[1:0]**

These bits set the averaging control for what is transmitted on the LVDS output OUT5.

### Register 2Eh

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| 0 | HPF_EN_CH1 | HPF_CORNER _CH1[3:0] | | | | FILTER_TYPE_CH1[2:0] | |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| FILTER_TYPE _CH1[2:0] | DEC_RATE_CH1[2:0] | | | 0 | SEL_ODD_ TAP_CH1 | 0 | USE_FILTER_ CH1 |

**Bit D15** **Must write '0'**

**Bit D14** **HPF_EN_CH1**

This bit enables the HPF filter for channel 1.

**Bits D[13:10]** **HPF_CORNER _CH1[3:0]**

These bits program the HPF corner for channel 1.

**Bits D[9:7]** **FILTER_TYPE_CH1[2:0]**

These bits select the type of filter on channel 1.

**Bits D[6:4]** **DEC_RATE_CH1[2:0]**

These bits set the decimation factor for the filter on channel 1.

**Bit D3** **Must write '0'**

**Bit D2** **SEL_ODD_TAP_CH1**

This bit enables the odd tap filter for channel 1.

**Bit D1** **Must write '0'**

**Bit D0** **USE_FILTER_CH1**

This bit enables the filter for channel 1.

### Register 2Fh

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| 0 | HPF_EN_CH2 | HPF_CORNER _CH2[3:0] | | | | FILTER_TYPE_CH2[2:0] | |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| FILTER_TYPE _CH2[2:0] | DEC_RATE_CH2[2:0] | | | 0 | SEL_ODD_ TAP_CH2 | 0 | USE_FILTER_ CH2 |

**Bit D15** **Must write '0'**

**Bit D14** **HPF_EN_CH2**

This bit enables the HPF filter for channel 2.

**Bits D[13:10]** **HPF_CORNER _CH2[3:0]**

These bits program the HPF corner for channel 2.

**Bits D[9:7]** **FILTER_TYPE_CH2[2:0]**

These bits select the type of filter on channel 2.

**Bits D[6:4]** **DEC_RATE_CH2[2:0]**

These bits set the decimation factor for the filter on channel 2.

**Bit D3** **Must write '0'**

**Bit D2** **SEL_ODD_TAP_CH2**

This bit enables the odd tap filter for channel 2.

**Bit D1** **Must write '0'**

**Bit D0** **USE_FILTER_CH2**

This bit enables the filter for channel 2.

### Register 30h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| 0 | HPF_EN_CH3 | HPF_CORNER _CH3[3:0] | | | | FILTER_TYPE_CH3[2:0] | |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| FILTER_TYPE _CH3[2:0] | DEC_RATE_CH3[2:0] | | | 0 | SEL_ODD_ TAP_CH3 | 0 | USE_FILTER_ CH3 |

**Bit D15** **Must write '0'**

**Bit D14** **HPF_EN_CH3**

This bit enables the HPF filter for channel 3.

**Bits D[13:10]** **HPF_CORNER _CH3[3:0]**

These bits program the HPF corner for channel 3.

**Bits D[9:7]** **FILTER_TYPE_CH3[2:0]**

These bits select the type of filter on channel 3.

**Bits D[6:4]** **DEC_RATE_CH3[2:0]**

These bits set the decimation factor for the filter on channel 3.

**Bit D3** **Must write '0'**

**Bit D2** **SEL_ODD_TAP_CH3**

This bit enables the odd tap filter for channel 3.

**Bit D1** **Must write '0'**

**Bit D0** **USE_FILTER_CH3**

This bit enables the filter for channel 3.

### Register 31h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| 0 | HPF_EN_CH4 | HPF_CORNER _CH4[3:0] | | | | FILTER_TYPE_CH4[2:0] | |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| FILTER_TYPE _CH4[2:0] | DEC_RATE_CH4[2:0] | | | 0 | SEL_ODD_ TAP_CH4 | 0 | USE_FILTER_ CH4 |

**Bit D15** **Must write '0'**

**Bit D14** **HPF_EN_CH4**

This bit enables the HPF filter for channel 4.

**Bits D[13:10]** **HPF_CORNER _CH4[3:0]**

These bits program the HPF corner for channel 4.

**Bits D[9:7]** **FILTER_TYPE_CH4[2:0]**

These bits select the type of filter on channel 4.

**Bits D[6:4]** **DEC_RATE_CH4[2:0]**

These bits set the decimation factor for the filter on channel 4.

**Bit D3** **Must write '0'**

**Bit D2** **SEL_ODD_TAP_CH4**

This bit enables the odd tap filter for channel 4.

**Bit D1** **Must write '0'**

**Bit D0** **USE_FILTER_CH4**

This bit enables the filter for channel 4.

### Register 32h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| 0 | HPF_EN_CH5 | HPF_CORNER _CH5[3:0] | | | | FILTER_TYPE_CH5[2:0] | |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| FILTER_TYPE _CH5[2:0] | DEC_RATE_CH5[2:0] | | | 0 | SEL_ODD_ TAP_CH5 | 0 | USE_FILTER_ CH5 |

**Bit D15** **Must write '0'**

**Bit D14** **HPF_EN_CH5**

This bit enables the HPF filter for channel 5.

**Bits D[13:10]** **HPF_CORNER _CH5[3:0]**

These bits program the HPF corner for channel 5.

**Bits D[9:7]** **FILTER_TYPE_CH5[2:0]**

These bits select the type of filter on channel 5.

**Bits D[6:4]** **DEC_RATE_CH5[2:0]**

These bits set the decimation factor for the filter on channel 5.

**Bit D3** **Must write '0'**

**Bit D2** **SEL_ODD_TAP_CH5**

This bit enables the odd tap filter for channel 5.

**Bit D1** **Must write '0'**

**Bit D0** **USE_FILTER_CH5**

This bit enables the filter for channel 5.

### Register 33h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| 0 | HPF_EN_CH6 | HPF_CORNER _CH6[3:0] | | | | FILTER_TYPE_CH6[2:0] | |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| FILTER_TYPE _CH6[2:0] | DEC_RATE_CH6[2:0] | | | 0 | SEL_ODD_ TAP_CH6 | 0 | USE_FILTER_ CH6 |

**Bit D15** **Must write '0'**

**Bit D14** **HPF_EN_CH6**

This bit enables the HPF filter for channel 6.

**Bits D[13:10]** **HPF_CORNER _CH6[3:0]**

These bits program the HPF corner for channel 6.

**Bits D[9:7]** **FILTER_TYPE_CH6[2:0]**

These bits select the type of filter on channel 6.

**Bits D[6:4]** **DEC_RATE_CH6[2:0]**

These bits set the decimation factor for the filter on channel 6.

**Bit D3** **Must write '0'**

**Bit D2** **SEL_ODD_TAP_CH6**

This bit enables the odd tap filter for channel 6.

**Bit D1** **Must write '0'**

**Bit D0** **USE_FILTER_CH6**

This bit enables the filter for channel 6.

### Register 34h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| 0 | HPF_EN_CH7 | HPF_CORNER _CH7[3:0] | | | | FILTER_TYPE_CH7[2:0] | |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| FILTER_TYPE _CH7[2:0] | DEC_RATE_CH7[2:0] | | | 0 | SEL_ODD_ TAP_CH7 | 0 | USE_FILTER_ CH7 |

**Bit D15** **Must write '0'**

**Bit D14** **HPF_EN_CH7**

This bit enables the HPF filter for channel 7.

**Bits D[13:10]** **HPF_CORNER _CH7[3:0]**

These bits program the HPF corner for channel 7.

**Bits D[9:7]** **FILTER_TYPE_CH7[2:0]**

These bits select the type of filter on channel 7.

**Bits D[6:4]** **DEC_RATE_CH7[2:0]**

These bits set the decimation factor for the filter on channel 7.

**Bit D3** **Must write '0'**

**Bit D2** **SEL_ODD_TAP_CH7**

This bit enables the odd tap filter for channel 7.

**Bit D1** **Must write '0'**

**Bit D0** **USE_FILTER_CH7**

This bit enables the filter for channel 7.

### Register 35h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| 0 | HPF_EN_CH8 | HPF_CORNER _CH8[3:0] | | | | FILTER_TYPE_CH8[2:0] | |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| FILTER_TYPE _CH8[2:0] | DEC_RATE_CH8[2:0] | | | 0 | SEL_ODD_ TAP_CH8 | 0 | USE_FILTER_ CH8 |

**Bit D15** **Must write '0'**

**Bit D14** **HPF_EN_CH8**

This bit enables the HPF filter for channel 8.

**Bits D[13:10]** **HPF_CORNER _CH8[3:0]**

These bits program the HPF corner for channel 8.

**Bits D[9:7]** **FILTER_TYPE_CH8[2:0]**

These bits select the type of filter on channel 8.

**Bits D[6:4]** **DEC_RATE_CH8[2:0]**

These bits set the decimation factor for the filter on channel 8.

**Bit D3** **Must write '0'**

**Bit D2** **SEL_ODD_TAP_CH8**

This bit enables the odd tap filter for channel 8.

**Bit D1** **Must write '0'**

**Bit D0** **USE_FILTER_CH8**

This bit enables the filter for channel 8.

### Register 38h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | DATA_RATE[1:0] | |

**Bits D[15:2]** **Must write '0'**

**Bits D[1:0]** **DATA_RATE[1:0]**

Bits D1 and D0 select the output data rate depending on the type of filter.

### Register 42h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| EN_PHASE_DDR | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 0 | PHASE_DDR1 | PHASE_DDR0 | 0 | 0 | 0 | 0 | 0 |

**Bit D15** **This bit enables LCLK phase programmability.**

**Bits D[14:7]** **Must write '0'**

**Bits D[6:5]** **PHASE_DDR[1:0]**

These bits control the LCLK output phase relative to data.
Refer to the *Programmable LCLK Phase* section.

**Bits D[4:0]** **Must write '0'**

### Register 45h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | PAT_DESKEW_SYNC[1:0] | |

**Bits D[15:2]** **Must write '0'**

**Bit D1** **PAT_DESKEW_SYNC1**

0 = Inactive
1 = Sync pattern mode enabled; ensure that D0 is '0'

**Bit D0** **PAT_DESKEW_SYNC0**

0 = Inactive
1 = Deskew pattern mode enabled; ensure that D1 is '0'

### Register 46h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| ENABLE 46 | 0 | FALL_SDR | 0 | BIT_SER_SEL | | | |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | EN_SDR | EN_MSB_FIRST | BTC_MODE | 0 | EN_2WIRE |

All bits default to '0' after reset. Note that bit D15 must be set to '1' to enable bits D[13:0].

**Bit D15** **ENABLE 46**

This bit enables register 46h.

**Bit D14** **Must write '0'**

**Bit D13** **FALL_SDR**

0 = The LCLK rising or falling edge comes at the edge of the data window when operating in SDR output mode
1 = The LCLK rising or falling edge comes in the middle of the data window when operating in SDR output mode

**Bit D12** **Must write '0'**

**Bits D[11:8]** **BIT_SER_SEL**

0001 = 10-bit serialization mode enabled
0010 = 12-bit serialization mode enabled
0100 = 14-bit serialization mode enabled
1000 = 16-bit serialization mode enabled
Do not use any other bit combinations.

**Bits D[7:5]** **Must write '0'**

**Bit D4** **EN_SDR**

0 = DDR bit clock
1 = SDR bit clock

**Bit D3** **EN_MSB_FIRST**

0 = LSB first
1 = MSB first

**Bit D2** **BTC_MODE**

0 = Binary offset (ADC data output format)
1 = Twos complement (ADC data output format)

**Bit D1** **Must write '0'**

**Bit D0** **EN_2WIRE**

0 = One-wire LVDS output
1 = Two-wire LVDS output

## Programmable LVDS Mapping Mode Registers

### *Register 50h*

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| ENABLE 50 | 0 | 0 | 0 | MAP_Ch1234_to_OUT2A | | | |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| MAP_Ch1234_to_OUT1B | | | | MAP_Ch1234_to_OUT1A | | | |

**Bit D15** **ENABLE 50**

This bit enables bits D[11:0] of register 50h.

**Bits D[14:12]** **Must write '0'**

**Bits D[11:8]** **MAP_Ch1234_to_OUT2A**

These bits set the OUT2A pin pair to the channel data mapping selection.

**Bits D[7:4]** **MAP_Ch1234_to_OUT1B**

These bits set the OUT1B pin pair to the channel data mapping selection.

**Bits D[3:0]** **MAP_Ch1234_to_OUT1A**

These bits set the OUT1A pin pair to the channel data mapping selection.

### *Register 51h*

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| ENABLE 51 | 0 | 0 | 0 | MAP_Ch1234_to_OUT3B | | | |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| MAP_Ch1234_to_OUT3A | | | | MAP_Ch1234_to_OUT2B | | | |

**Bit D15** **ENABLE 51**

This bit enables bits D[11:0] of register 51h.

**Bits D[14:12]** **Must write '0'**

**Bits D[11:8]** **MAP_Ch1234_to_OUT3B**

These bits set the OUT3B pin pair to the channel data mapping selection.

**Bits D[7:4]** **MAP_Ch1234_to_OUT3A**

These bits set the OUT3A pin pair to the channel data mapping selection.

**Bits D[3:0]** **MAP_Ch1234_to_OUT2B**

These bits set the OUT2B pin pair to the channel data mapping selection.

### *Register 52h*

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| ENABLE 52 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| MAP_Ch1234_to_OUT4B | | | | MAP_Ch1234_to_OUT4A | | | |

**Bit D15** **ENABLE 52**

This bit enables bits D[7:0] of register 52h.

**Bits D[14:8]** **Must write '0'**

**Bits D[7:4]** **MAP_Ch1234_to_OUT4B**

These bits set the OUT4B pin pair to the channel data mapping selection.

**Bits D[3:0]** **MAP_Ch1234_to_OUT4A**

These bits set the OUT4A pin pair to the channel data mapping selection.

### *Register 53h*

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| ENABLE 53 | 0 | 0 | 0 | MAP_Ch5678_to_OUT6B | | | |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| MAP_Ch5678_to_OUT5A | | | | MAP_Ch5678_to_OUT5B | | | |

**Bit D15** **ENABLE 53**

This bit enables bits D[11:0] of register 53h.

**Bits D[14:12]** **Must write '0'**

**Bits D[11:8]** **MAP_Ch5678_to_OUT6B**

These bits set the OUT6B pin pair to the channel data mapping selection.

**Bits D[7:4]** **MAP_Ch5678_to_OUT5A**

These bits set the OUT5A pin pair to the channel data mapping selection.

**Bits D[3:0]** **MAP_Ch5678_to_OUT5B**

These bits set the OUT5B pin pair to the channel data mapping selection.

### *Register 54h*

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| ENABLE 54 | 0 | 0 | 0 | MAP_Ch5678_to_OUT7A | | | |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| MAP_Ch5678_to_OUT7B | | | | MAP_Ch5678_to_OUT6A | | | |

**Bit D15** **ENABLE 54**

This bit enables bits D[11:0] of register 54h.

**Bits D[14:12]** **Must write '0'**

**Bits D[11:8]** **MAP_Ch5678_to_OUT7A**

These bits set the OUT7A pin pair to the channel data mapping selection.

**Bits D[7:4]** **MAP_Ch5678_to_OUT7B**

These bits set the OUT7B pin pair to the channel data mapping selection.

**Bits D[3:0]** **MAP_Ch5678_to_OUT6A**

These bits set the OUT6A pin pair to the channel data mapping selection.

### *Register 55h*

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| ENABLE 55 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| MAP_Ch5678_to_OUT8A | | | | MAP_Ch5678_to_OUT8B | | | |

**Bit D15** **ENABLE 55**

This bit enables bits D[7:0] of register 55h.

**Bits D[14:8]** **Must write '0'**

**Bits D[7:4]** **MAP_Ch5678_to_OUT8A**

These bits set the OUT8A pin pair to the channel data mapping selection.

**Bits D[3:0]** **MAP_Ch5678_to_OUT8B**

These bits set the OUT8B pin pair to the channel data mapping selection.

### Custom Coefficient Registers

#### *Registers 5Ah to 65h*[(1)]

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| EN_CUSTOM_FILT_CH1 | 0 | 0 | 0 | COEFF*n*_SET_CH1[11:0] | | | |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| COEFF*n*_SET_CH1[11:0] | | | | | | | |

(1) n = 0 to 11.

These registers are the custom coefficient registers for channel 1.

**Bit D15** **EN_CUSTOM_FILT_CH1**

0 = Built-in coefficients are used
1 = Enables custom coefficients to be used

**Bits D[14:12]** **Must write '0'**

**Bits D[11:0]** **COEFF*n*_SET_CH1[11:0]**

These bits set the custom coefficient *n* for the channel 1 digital filter.

#### *Registers 66h to 71h*[(1)]

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| EN_CUSTOM_FILT_CH2 | 0 | 0 | 0 | COEFF*n*_SET_CH2[11:0] | | | |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| COEFF*n*_SET_CH2[11:0] | | | | | | | |

(1) n = 0 to 11.

These registers are the custom coefficient registers for channel 2.

**Bit D15** **EN_CUSTOM_FILT_CH2**

0 = Built-in coefficients are used
1 = Enables custom coefficients to be used

**Bits D[14:12]** **Must write '0'**

**Bits D[11:0]** **COEFF*n*_SET_CH2[11:0]**

These bits set the custom coefficient *n* for the channel 2 digital filter.

### *Registers 72h to 7Dh*[1]

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| EN_CUSTOM_FILT_CH3 | 0 | 0 | 0 | COEFF*n*_SET_CH3[11:0] | | | |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| COEFF*n*_SET_CH3[11:0] | | | | | | | |

(1) n = 0 to 11.

These registers are the custom coefficient registers for channel 3.

**Bit D15** **EN_CUSTOM_FILT_CH3**

0 = Built-in coefficients are used
1 = Enables custom coefficients to be used

**Bits D[14:12]** **Must write '0'**

**Bits D[11:0]** **COEFF*n*_SET_CH3[11:0]**

These bits set the custom coefficient *n* for the channel 3 digital filter.

### *Registers 7Eh to 89h*[1]

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| EN_CUSTOM_FILT_CH4 | 0 | 0 | 0 | COEFF*n*_SET_CH4[11:0] | | | |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| COEFF*n*_SET_CH4[11:0] | | | | | | | |

(1) n = 0 to 11.

These registers are the custom coefficient registers for channel 4.

**Bit D15** **EN_CUSTOM_FILT_CH4**

0 = Built-in coefficients are used
1 = Enables custom coefficients to be used

**Bits D[14:12]** **Must write '0'**

**Bits D[11:0]** **COEFF*n*_SET_CH1[11:0]**

These bits set the custom coefficient *n* for the channel 4 digital filter.

### *Registers 8Ah to 95h*[(1)]

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| EN_CUSTOM_FILT_CH5 | 0 | 0 | 0 | COEFF*n*_SET_CH5[11:0] | | | |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| COEFF*n*_SET_CH5[11:0] | | | | | | | |

(1) n = 0 to 11.

These registers are the custom coefficient registers for channel 5.

**Bit D15** **EN_CUSTOM_FILT_CH5**

0 = Built-in coefficients are used
1 = Enables custom coefficients to be used

**Bits D[14:12]** **Must write '0'**

**Bits D[11:0]** **COEFF*n*_SET_CH5[11:0]**

These bits set the custom coefficient *n* for the channel 5 digital filter.

### *Registers 96h to A1h*[(1)]

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| EN_CUSTOM_FILT_CH6 | 0 | 0 | 0 | COEFF*n*_SET_CH6[11:0] | | | |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| COEFF*n*_SET_CH6[11:0] | | | | | | | |

(1) n = 0 to 11.

These registers are the custom coefficient registers for channel 6.

**Bit D15** **EN_CUSTOM_FILT_CH6**

0 = Built-in coefficients are used
1 = Enables custom coefficients to be used

**Bits D[14:12]** **Must write '0'**

**Bits D[11:0]** **COEFF*n*_SET_CH6[11:0]**

These bits set the custom coefficient *n* for the channel 6 digital filter.

### *Registers A2h to ADh*[(1)]

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| EN_CUSTOM_FILT_CH7 | 0 | 0 | 0 | COEFF*n*_SET_CH7[11:0] | | | |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| COEFF*n*_SET_CH7[11:0] | | | | | | | |

(1) n = 0 to 11.

These registers are the custom coefficient registers for channel 7.

**Bit D15** **EN_CUSTOM_FILT_CH7**

0 = Built-in coefficients are used
1 = Enables custom coefficients to be used

**Bits D[14:12]** **Must write '0'**

**Bits D[11:0]** **COEFF*n*_SET_CH7[11:0]**

These bits set the custom coefficient *n* for the channel 7 digital filter.

### *Registers AEh to B9h*[(1)]

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| EN_CUSTOM_FILT_CH8 | 0 | 0 | 0 | COEFF*n*_SET_CH8[11:0] | | | |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| COEFF*n*_SET_CH8[11:0] | | | | | | | |

(1) n = 0 to 11.

These registers are the custom coefficient registers for channel 8.

**Bit D15** **EN_CUSTOM_FILT_CH8**

0 = Built-in coefficients are used
1 = Enables custom coefficients to be used

**Bits D[14:12]** **Must write '0'**

**Bits D[11:0]** **COEFF*n*_SET_CH8[11:0]**

These bits set the custom coefficient *n* for the channel 8 digital filter.

### Register BEh

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| EN_LVDS_PROG | 0 | 0 | 0 | 0 | 0 | DELAY_DATA_R[1:0] | |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| DELAY_LCLK_R[2:0] | | | DELAY_DATA_F[1:0] | | DELAY_LCLK_F[2:0] | | |

**Bit D15** **This bit enables LVDS edge delay programmability.**

**Bits D[14:10]** **Must write '0'**

Bits D[9:8] Refer Table 22 for settings.

Bits D[7:5] Refer Table 23 for settings.

Bits D[4:3] Refer Table 22 for settings.

Bits D[2:0] Refer Table 23 for settings.

### Register F0h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|
| EN_EXT_REF | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The EN_HIGH_ADDRS register bit (register 01h, bit D4) must be set to '1' to allow access to this register.

**Bit D15** **EN_EXT_REF**

0 = Internal reference mode (default)
1 = External reference mode enabled; apply the reference voltages on the REFT and REFB pins

**Bits D[14:0]** **Must write '0'**

## APPLICATION INFORMATION

### THEORY OF OPERATION

The ADS5295 is a low-power, 8-channel, 12-bit analog-to-digital converter (ADC) with sample rates up to 100 MSPS that run off of a single 1.8-V supply. All eight channels simultaneously sample the analog inputs at the input clock rising edge. The sampled signal is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock edge, the sample propagates through the pipeline, resulting in a data latency of 12 clock cycles.

### ANALOG INPUT

The analog input consists of a switched-capacitor-based, differential sample-and-hold architecture, as shown in Figure 46. This differential topology results in very good ac performance even for high input frequencies at high sampling rates. The INP and INM pins must be externally biased around a common-mode voltage of 0.95 V, available on the VCM pin. For a full-scale differential input, each input pin (INP, INN) must swing symmetrically between VCM + 0.5 V and VCM – 0.5 V, resulting in a 2-$V_{PP}$ differential input swing. The input sampling circuit has a high 3-dB bandwidth that extends up to 500 MHz (measured from the input pins to the sampled voltage).

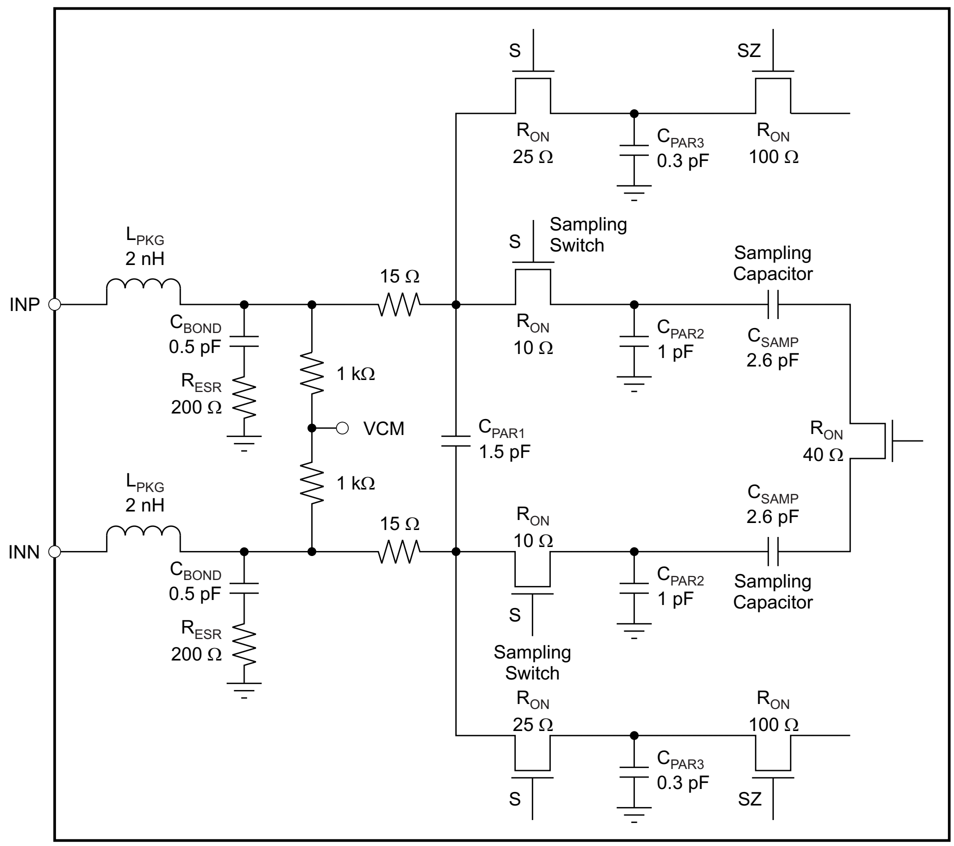



**Figure 46. Analog Input Equivalent Circuit**

### Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This architecture improves the common-mode noise immunity and even-order harmonic rejection. A small resistor (5 Ω to 10 Ω) in series with each input pin is recommended to damp out ringing caused by package parasitics. The drive circuits in Figure 47 and Figure 48 show an R-C filter across the analog input pins. The purpose of the filter is to absorb the glitches caused by the opening and closing of the sampling capacitors. Figure 49 and Figure 50 show the differential input resistance and capacitance across frequency.

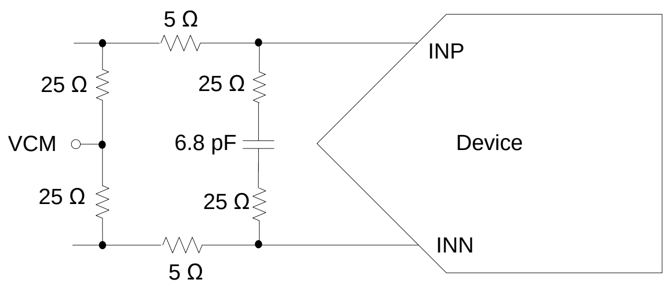



**Figure 47. DC-Coupled Drive Circuit with RCR**

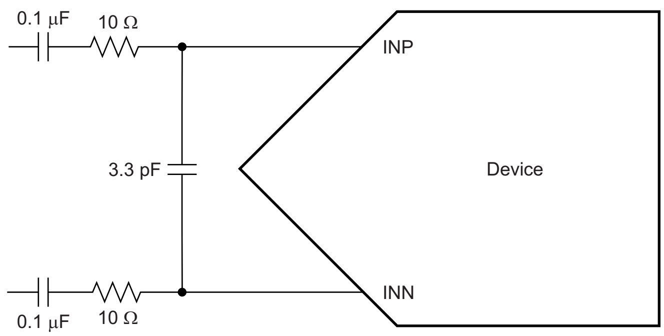



**Figure 48. AC-Coupled Drive Circuit**

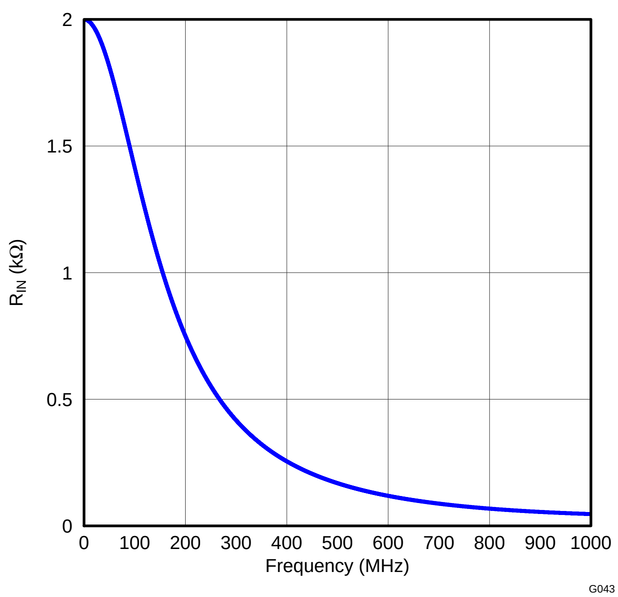



**Figure 49. ADC Differential Input Resistance ($R_{IN}$) vs Frequency**

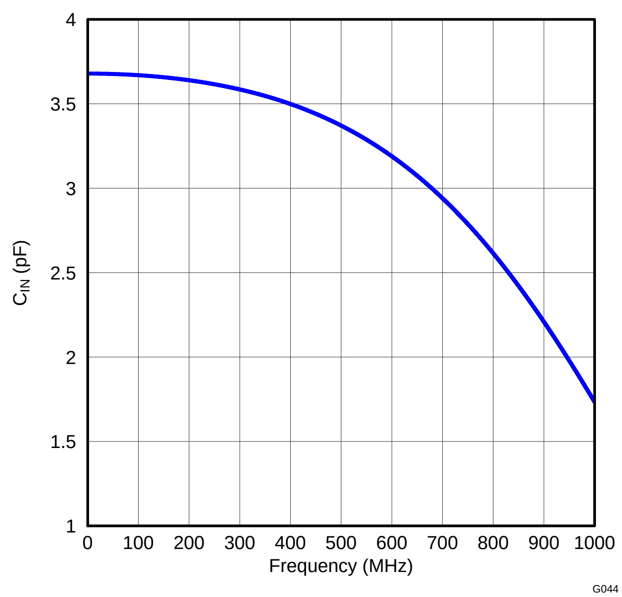



**Figure 50. ADC Differential Input Capacitance ($C_{IN}$) vs Frequency**

### Large- and Small-Signal Input Bandwidth

The small-signal bandwidth of the analog input circuit is high, approximately 500 MHz. When using an amplifier to drive the ADS5295, the total amplifier noise up to the small-signal bandwidth must be considered. The large-signal bandwidth of the device depends on the amplitude of the input signal. The ADS5295 supports a 2-$V_{PP}$ amplitude for input signal frequencies up to 90 MHz. For higher frequencies, the amplitude of the input signal must be decreased proportionally. For example, at 180 MHz, the device supports a maximum 1-$V_{PP}$ signal.

## CLOCK INPUT

The ADS5295 can operate with both single-ended (CMOS) and differential input clocks (such as sine wave, LVPECL, and LVDS). Operating with a low-jitter differential clock is recommended for good SNR performance, especially at input frequencies greater than 30 MHz. In the differential mode, the clock inputs are internally biased to a 0.95-V common-mode voltage. While driving with an external LVPECL or LVDS driver, TI recommends ac-coupling the clock signals so that the clock pins are correctly biased to the common-mode voltage (0.95 V). To operate using a single-ended clock, connect a CMOS clock source to CLKP and tie CLKN to GND. The device automatically detects the presence of a single-ended clock without requiring any configuration and disables the internal biasing. Typical clock termination schemes are shown in Figure 51, Figure 52, Figure 53, and Figure 54.

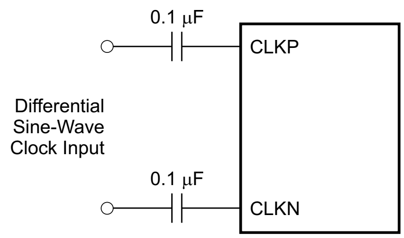



**Figure 51. Differential Sine-Wave Clock Driving Circuit**

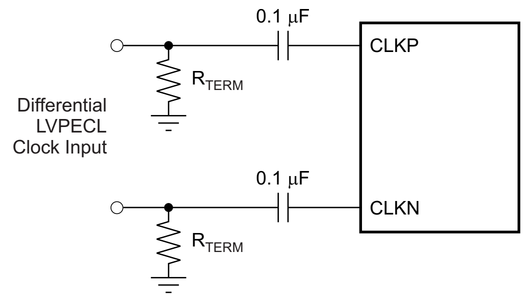



**Figure 52. Differential LVPECL Clock Driving Circuit**

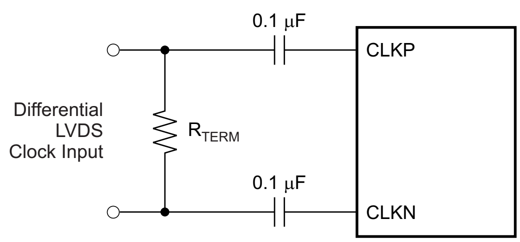



**Figure 53. Differential LVDS Clock Driving Circuit**

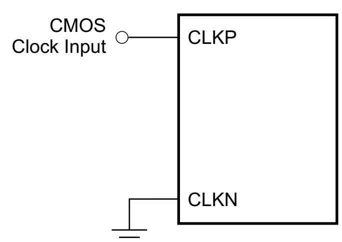



**Figure 54. Single-Ended Clock Driving Circuit**

## EXTERNAL REFERENCE MODE OF OPERATION

For normal operation, the device requires two reference voltages (REFT and REFB) that are generated internally by default, as shown in Figure 55. The value of the reference voltage determines the actual ADC full-scale input voltage, as shown in Equation 1:

$$\text{Full-Scale Input Voltage} = 2 \times (V_{REFT} - V_{REFB}) \quad (1)$$

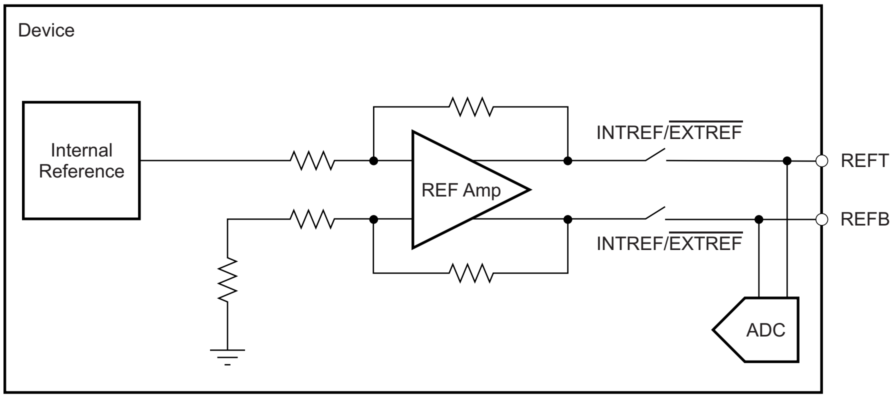



**Figure 55. Reference Equivalent Circuit**

Any error in the reference results in a deviation of the full-scale input range from its ideal value of 2.0 $V_{PP}$, as shown in Equation 2:

$$\text{Error in Full-Scale Voltage} = 2x\ [\text{Error in } (V_{REFT} - V_{REFB})] \quad (2)$$

The reference inaccuracy results in a gain error, which is defined as Equation 3:

$$\text{Gain Error (\%)} = \text{Error in Full-Scale Voltage} \times \frac{100}{\text{Ideal Full-Scale Voltage}}$$

$$= 2x\ [\text{Error in } (V_{REFT} - V_{REFB})] \times \frac{100}{2.0} \quad (3)$$

To minimize the gain error, the internal reference voltages are trimmed to an accuracy of ±1.5% (or ±30 mV). To obtain even lower gain error, the ADS5295 supports an external reference mode of operation. In this mode, the internal reference amplifiers are powered down and an external amplifier must force the reference voltages on the REFT and REFB pins. For example, this mode can be used to ensure that multiple ADS5295 chips in the system have nearly the same full-scale voltage.

To enable the external reference mode, set the register bits as shown in Table 8. These settings power down the internal reference amplifier and the two reference voltages can be forced directly on the REFT and REFB pins as $V_{REFT}$ = 1.45 V and $V_{REFB}$ = 0.45 V.

**Table 8. External Reference Function**

| FUNCTION | EN_HIGH_ADDRS | EN_EXT_REF |
|---|---|---|
| External reference using the REFT, REFB pins | 1 | 1 |

Because the internal reference amplifiers are powered down, the accuracy of the full-scale voltage is determined by the accuracy of ($V_{REFT}$ – $V_{REFB}$), where $V_{REFT}$ is the voltage forced on REFT and $V_{REFB}$ is the voltage forced on REFB.

Note that although the nominal value of ($V_{REFT}$ – $V_{REFB}$) = 1.0 V, ensure that:

[($V_{REFT}$ + $V_{REFB}$) / 2 = 0.950 V ± 50 mV].

Figure 56 shows an example of driving the reference pins. The 1-µF bypass capacitor helps provide the switching current drawn by the REFT and REFB pins. The external amplifier must provide an average current of 5 mA or less at 100 MSPS. The performance in the external reference mode depends on the sampling speed. At low sampling speeds (20 MSPS), the performance is the same as that of an internal reference. At higher speeds, the performance degrades because of the effect of the parasitic bond-wire inductance of the REF pins. Figure 57 highlights the difference in SNR between the external and internal reference modes.

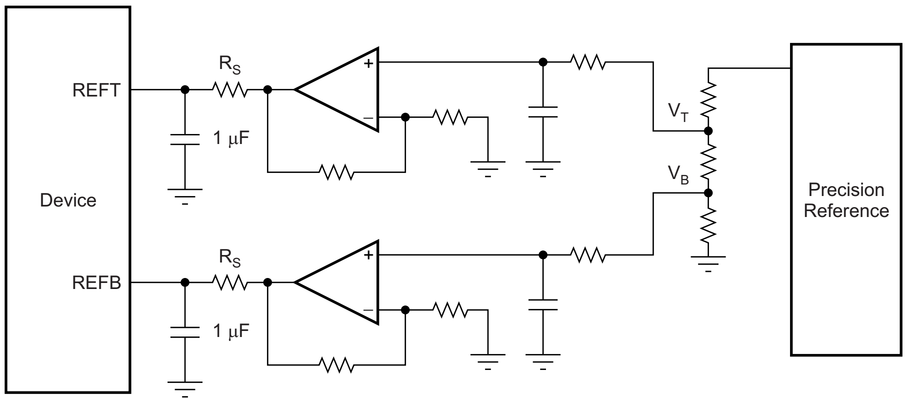



**Figure 56. Driving Reference Inputs in External Reference Mode**

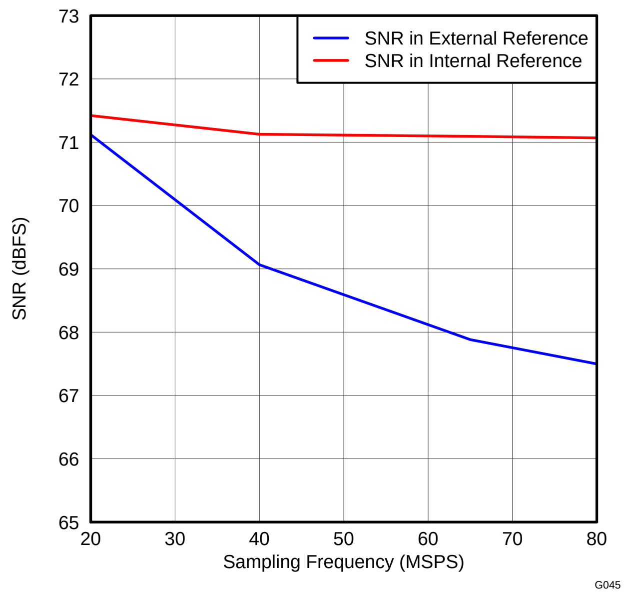



**Figure 57. SNR in Internal and External Reference Mode**

## LOW-FREQUENCY NOISE SUPPRESSION

The low-frequency noise suppression (LFNS) mode is particularly useful in applications where good noise performance is desired in the low-frequency band of dc to 1 MHz. By setting this mode, the low-frequency noise spectrum band around dc is shifted to a similar band around $f_S$ / 2 (or the Nyquist frequency). As a result, the noise spectrum from dc to approximately 1 MHz improves significantly, as shown in Figure 58, Figure 59, and Figure 60.

This function can be selectively enabled in each channel using the LFNS_CH register bits. Figure 58, Figure 59, and Figure 60 show the effect of this mode on the spectrum.

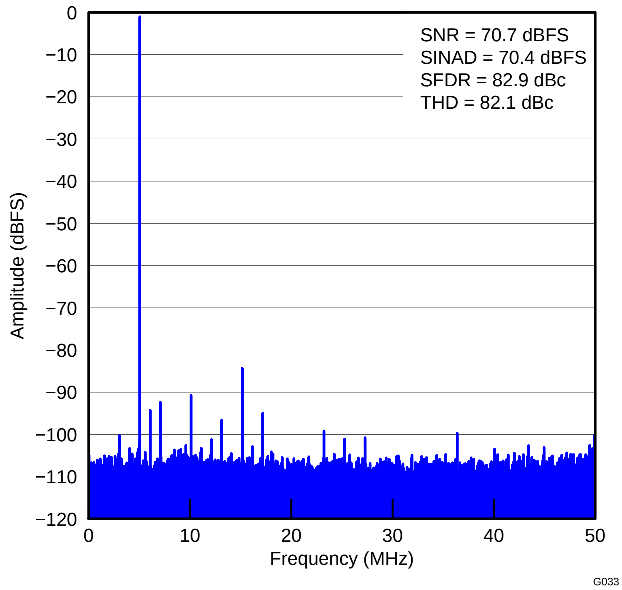



Figure 58. Full-Scale Input Amplitude

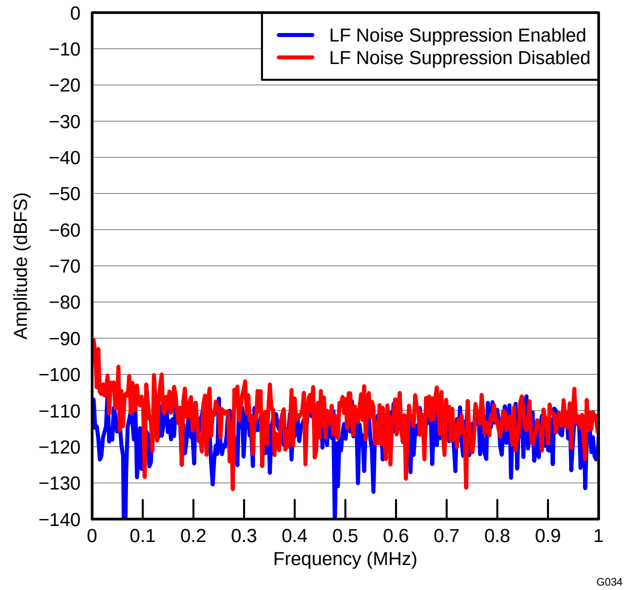



Figure 59. Spectrum (Zoomed) From DC to 1 MHz

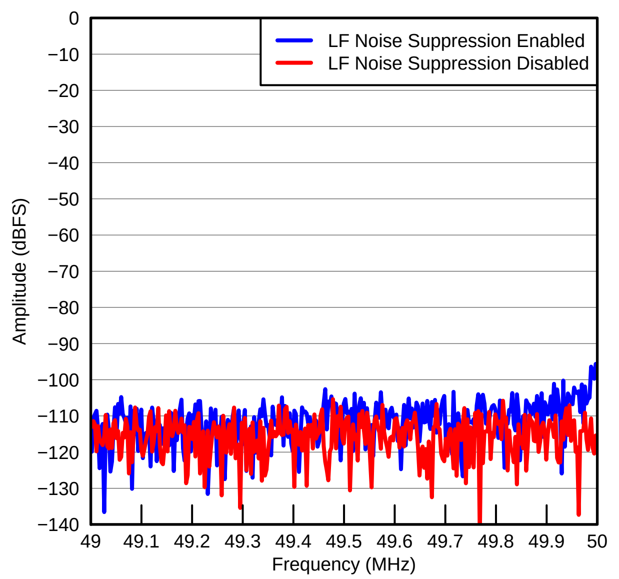



Figure 60. Spectrum (Zoomed) in 1-MHz Band from 49 MHz to 50 MHz ($f_S$ = 100 MSPS)

## DIGITAL PROCESSING BLOCKS

The ADS5295 integrates a set of commonly-used digital functions that can be used to ease system design. These functions are shown in Figure 61 and are described in the following sections.

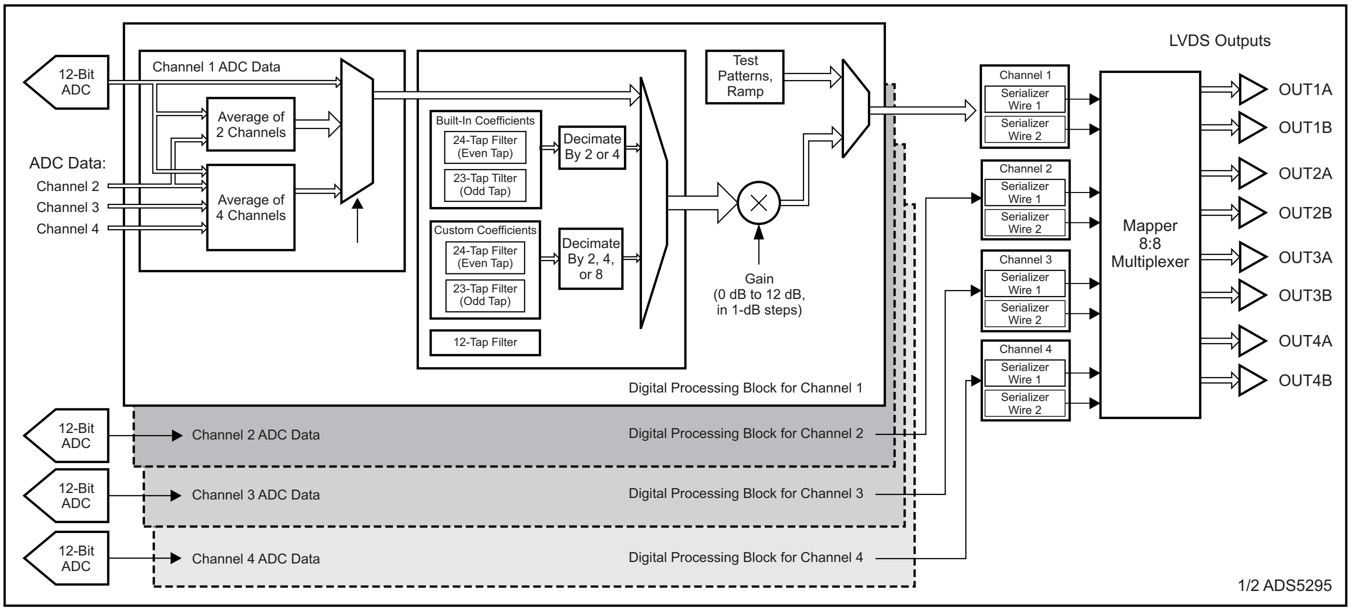



**Figure 61. Digital Processing Block Diagram**

### Digital Gain

The ADS5295 includes programmable digital gain settings from 0 dB to 12 dB in 1-dB steps. The benefit of digital gain is obtaining improved SFDR performance. However, SFDR improvement is achieved at the expense of SNR; for each gain setting, SNR degrades by approximately 1 dB. Therefore, the gain can be used to trade-off between SFDR and SNR.

For each gain setting, the supported analog input full-scale range scales proportionally, as shown in Table 9. After reset, the device comes up in 0-dB gain mode. To use other gain settings, program the GAIN_CH[3:0] register bits.

**Table 9. Analog Full-Scale Range Across Gains**

| GAIN_CH[3:0] | DIGITAL GAIN (dB) | ANALOG FULL-SCALE INPUT ($V_{PP}$) |
|---|---|---|
| 0000 | 0 | 2 |
| 0001 | 1 | 1.78 |
| 0010 | 2 | 1.59 |
| 0011 | 3 | 1.42 |
| 0100 | 4 | 1.26 |
| 0101 | 5 | 1.12 |
| 0110 | 6 | 1 |
| 0111 | 7 | 0.89 |
| 1000 | 8 | 0.8 |
| 1001 | 9 | 0.71 |
| 1010 | 10 | 0.63 |
| 1011 | 11 | 0.56 |
| 1100 | 12 | 0.5 |
| Other combinations | Do not use | — |

### Digital Filter

The digital processing block includes the option to filter and decimate the ADC data outputs digitally. Various filters and decimation rates are supported: decimation rates of 2, 4, and 8, and low-pass, high-pass, and band-pass filters are available.

The filters are internally implemented as 24-tap symmetric finite impulse response (FIR) filters (even-tap) using the predefined coefficients of Equation 4:

$$y(n) = \left(\frac{1}{2^{11}}\right) \times [h0.x(n) + h1.x(n-1) + h2.x(n-2) + ... + h11.x(n-11) + h12.x(n-12) + ... + h1.x(n-22) + h0.x(n-23)] \quad (4)$$

Alternatively, some filters can be configured as 23-tap symmetric FIR filters (odd-tap), as described in Equation 5:

$$y(n) = \left(\frac{1}{2^{11}}\right) \times [h0.x(n) + h1.x(n-1) + h2.x(n-2) + ... + h10.x(n-10) + h11.x(n-11) + h10.x(n-12) + ... + h1.x(n-21) + h0.x(n-22)] \quad (5)$$

In Equation 4 and Equation 5, h0 through h11 are 12-bit, signed, twos complement representations of the coefficients (–2048 to +2047). x(n) is the filter input data sequence and y(n) is the filter output sequence.

Details of the registers used for configuring the digital filters are described in the digital filter registers (registers 29h, 2Eh, 2Fh, 30h, 31h, and 38h) and Table 10. Table 10 gives a summary of the register bits to be used for each filter type.

**Table 10. Digital Filters**

| DECIMATION | TYPE OF FILTER | DATA_ RATE | DEC_RATE _CHn(1) | FILTER_ TYPE_CHn | ODD_ TAP_CH*n* | USE_ FILTER_ CH*n* | EN_ CUSTOM_ FILT_CH*n* | EN_DIG_ FILTER |
|---|---|---|---|---|---|---|---|---|
| Decimate-by-2 | Built-in, low-pass, odd-tap filter (pass band = 0 to $f_S$ / 4) | 01 | 000 | 000 | 1 | 1 | 0 | 1 |
| | Built-in, high-pass, odd-tap filter (pass band = 0 to $f_S$ / 4) | 01 | 000 | 001 | 1 | 1 | 0 | 1 |
| Decimate-by-4 | Built-in, low-pass, even-tap filter (pass band = 0 to $f_S$ / 8) | 10 | 001 | 010 | 0 | 1 | 0 | 1 |
| | Built-in, first band pass, even-tap filter (pass band = $f_S$ / 8 to $f_S$ / 4) | 10 | 001 | 011 | 0 | 1 | 0 | 1 |
| | Built-in, second band pass, even-tap filter (pass band = $f_S$ / 4 to 3 $f_S$ / 8) | 10 | 001 | 100 | 0 | 1 | 0 | 1 |
| | Built-in, high-pass, odd-tap filter (pass band = 3 $f_S$ / 8 to $f_S$ / 2) | 10 | 001 | 101 | 1 | 1 | 0 | 1 |
| Decimate-by-2 | Custom filter (user-programmable coefficients) | 01 | 000 | 000 | 0 or 1 | 1 | 1 | 1 |
| Decimate-by-4 | Custom filter (user-programmable coefficients) | 10 | 001 | 000 | 0 or 1 | 1 | 1 | 1 |
| Decimate-by-8 | Custom filter (user-programmable coefficients) | 11 | 100 | 000 | 0 or 1 | 1 | 1 | 1 |
| 12-tap filter without decimation | Custom filter (user-programmable coefficients) | 00 | 011 | 000 | 0 | 1 | 1 | 1 |

(1) The DEC_RATE_CH*n* value must be the same for all channels.

### *Predefined Coefficients*

The built-in filter types (low pass, high pass, and band pass) use predefined coefficients. The frequency response of the built-in filters is shown in Figure 62 and Figure 63.

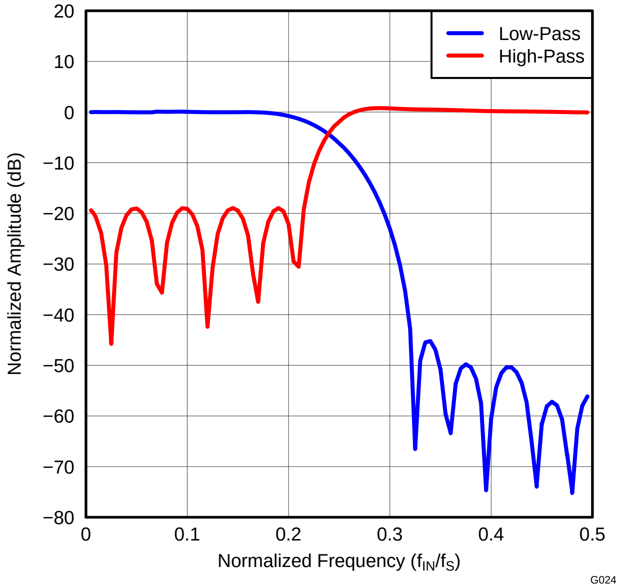



**Figure 62. Filter Response (Decimate-by-2)**

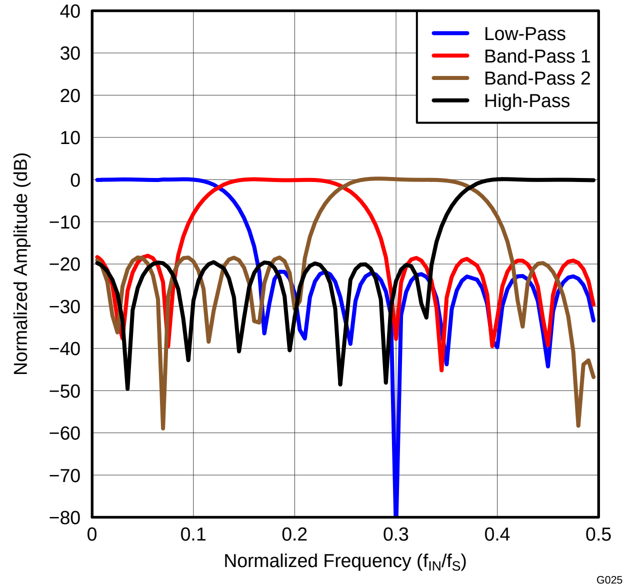



**Figure 63. Filter Response (Decimate-by-4)**

The predefined coefficients for the decimate-by-2 and decimate-by-4 filters are listed in Table 11 and Table 12, respectively.

**Table 11. Predefined Coefficients for Decimate-by-2 Filters**

| COEFFICIENTS | DECIMATE-BY-2 | |
|---|---|---|
| | LOW-PASS FILTER | HIGH-PASS FILTER |
| h0 | 3 | –22 |
| h1 | 0 | –65 |
| h2 | 5 | –52 |
| h3 | 1 | 30 |
| h4 | –27 | 66 |
| h5 | –2 | –35 |
| h6 | 73 | –107 |
| h7 | 3 | 38 |
| h8 | –178 | 202 |
| h9 | –4 | –41 |
| h10 | 636 | –644 |
| h11 | 1024 | 1061 |

**Table 12. Predefined Coefficients for Decimate-by-4 Filters**

| COEFFICIENTS | DECIMATE-BY-4 | | | |
|---|---|---|---|---|
| | LOW-PASS FILTER | 1st BAND-PASS FILTER | 2nd BAND-PASS FILTER | HIGH-PASS FILTER |
| h0 | –17 | –7 | –34 | 40 |
| h1 | –50 | 19 | –34 | –15 |
| h2 | 71 | –47 | –101 | –95 |
| h3 | 46 | 127 | 43 | 22 |
| h4 | 24 | 73 | 58 | –8 |
| h5 | –42 | 0 | –28 | –81 |
| h6 | –100 | 86 | –5 | 106 |
| h7 | –97 | 117 | –179 | –62 |
| h8 | 8 | –190 | 294 | –97 |
| h9 | 202 | –464 | 86 | 310 |
| h10 | 414 | –113 | –563 | –501 |
| h11 | 554 | 526 | 352 | 575 |

### Custom Filter Coefficients

In addition to the built-in filters described in the *Predefined Coefficients* section, customers also have the option of using their own custom, 12-bit, signed coefficients. Because of the symmetric FIR implementation of the filters, only 12 coefficients can be specified with the configuration of Equation 4 or Equation 5. These coefficients (h0 to h11) must be configured in the custom coefficient registers as shown in Equation 6:

$$\text{Register Content} = \text{12-Bit Signed Representation of (Real Coefficient Value} \times 2^{11}) \quad (6)$$

The 12 custom coefficients must be loaded into 12 separate registers for each channel (refer to the custom coefficient registers, 5Ah to B9h). The MSB bit of each coefficient register determines whether the built-in filters or custom filters are used. If the EN_CUSTOM_FILT MSB bit is reset to '0', then the built-in filter coefficients are used. Otherwise, the custom coefficients are used.

### Custom Filter without Decimation

Another mode is available that enables the use of the digital filter without decimation. In this mode, the filter behaves similar to a 12-tap symmetric FIR filter, as shown in Equation 7:

$$y(n) = \left(\frac{1}{2^{11}}\right) \times [h6.x(n) + h7.x(n-1) + h8.x(n-2) + h9.x(n-3) + h10.x(n-4) + h11.x(n-5) + h11.x(n-6) + h10.x(n-7) + h9.x(n-8) + h8.x(n-9) + h7.x(n-10) + h6.x(n-11)] \quad (7)$$

In Equation 7, h6 through h11 are 12-bit, signed, twos complement representations of the coefficients (–2048 to +2047). x(n) is the filter input data sequence and y(n) is the filter output sequence.

In this mode, because the filter is implemented as a 12-tap symmetric FIR, only six custom coefficients must be specified and loaded in registers h6 to h11 (refer to the custom coefficient registers, 5Ah to B9h). To enable this mode, use the register setting specified in bit 15 of registers AEh to B9h.

### Digital High-Pass Filter

In addition to the 12 tap filters described previously, the digital processing block also includes a separate high-pass filter for each channel. The high-pass corner frequency can be programmed using bits D[14:10] in register 2Eh.

### Digital Averaging

The ADS5295 includes an averaging function where the ADC digital data from two (or four) channels can be averaged. The averaged data are output on specific LVDS channels. Table 13 shows the combinations of the input channels that can be averaged and the LVDS channels on which the averaged data are available.

**Table 13. Using Channel Averaging**

| AVERAGED CHANNELS | OUTPUT WHERE AVERAGED DATA ARE AVAILABLE AT | REGISTER SETTINGS |
|---|---|---|
| 1, 2 | OUT1A, OUT1B | Set AVG_OUT1 = 10 and EN_CHANNEL_AVG = 1 |
| 1, 2 | OUT3A, OUT3B | Set AVG_OUT3 = 11 and EN_CHANNEL_AVG = 1 |
| 3, 4 | OUT4A, OUT4B | Set AVG_OUT4 = 10 and EN_CHANNEL_AVG = 1 |
| 3, 4 | OUT2A, OUT2B | Set AVG_OUT2 = 11 and EN_CHANNEL_AVG = 1 |
| 1, 2, 3, 4 | OUT1A, OUT1B | Set AVG_OUT1 = 11 and EN_CHANNEL_AVG = 1 |
| 1, 2, 3, 4 | OUT4A, OUT4B | Set AVG_OUT4 = 11 and EN_CHANNEL_AVG = 1 |
| 5, 6 | OUT5A, OUT5B | Set AVG_OUT5 = 10 and EN_CHANNEL_AVG = 1 |
| 5, 6 | OUT7A, OUT7B | Set AVG_OUT7 = 11 and EN_CHANNEL_AVG = 1 |
| 7, 8 | OUT8A, OUT8B | Set AVG_OUT8 = 10 and EN_CHANNEL_AVG = 1 |
| 7, 8 | OUT6A, OUT6B | Set AVG_OUT6 = 11 and EN_CHANNEL_AVG = 1 |
| 5, 6, 7, 8 | OUT5A, OUT5B | Set AVG_OUT5 = 11 and EN_CHANNEL_AVG = 1 |
| 5, 6, 7, 8 | OUT8A, OUT8B | Set AVG_OUT8 = 11 and EN_CHANNEL_AVG = 1 |

### Performance with Digital Processing Blocks

In applications where higher SNR performance is desired, digital processing blocks (such as averaging and decimation filters) can be used advantageously to achieve this. Table 14 shows the improvement in SNR that can be achieved compared to the default value, using these modes.

**Table 14. SNR Improvement Using Digital Processing**

| MODE(1) | TYPICAL SNR (dB)(2) | TYPICAL IMPROVEMENT IN SNR (dB) |
|---|---|---|
| Default | 70.6 | NA |
| With decimate-by-2 filter enabled | 74.64 | 4.04 |
| With decimate-by-4 filter enabled | 76.13 | 5.53 |
| With decimate-by-8 filter enabled | 77.04 | 6.44 |
| With two channels averaged and decimate-by-4 filter enabled | 77.43 | 6.83 |
| With four channels averaged | 76.14 | 5.54 |
| With four channels averaged and decimate-by-4 filter enabled | 79.27 | 8.67 |

(1) Custom coefficients are used for the decimate-by-8 filter.
(2) In all these modes (except the default one), 14x serialization is used to capture data.

## PROGRAMMABLE MAPPING BETWEEN INPUT CHANNELS AND OUTPUT PINS

The ADS5295 has 16 pairs of LVDS channel outputs. The mapping of ADC channels to LVDS output channels is programmable to allow for flexibility in board layout. The control register mapping is shown in Table 15. The 16 LVDS channel outputs are split into two groups of eight LVDS pairs. Within each group, four ADC input channels can be multiplexed to the eight LVDS pairs, depending on the mode of operation (one-wire mode or two-wire mode).

**Table 15. Mapping Control Registers**

| ADDRESS (Hex) | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | NAME |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 50 | 1 | | | | | | | | | | | | X | X | X | X | MAP_CH1234_TO_OUT1A |
| | 1 | | | | | | | | X | X | X | X | | | | | MAP_CH1234_TO_OUT1B |
| | 1 | | | | X | X | X | X | | | | | | | | | MAP_CH1234_TO_OUT2A |
| 51 | 1 | | | | | | | | | | | | X | X | X | X | MAP_CH1234_TO_OUT2B |
| | 1 | | | | | | | | X | X | X | X | | | | | MAP_CH1234_TO_OUT3A |
| | 1 | | | | X | X | X | X | | | | | | | | | MAP_CH1234_TO_OUT3B |
| 52 | 1 | | | | | | | | | | | | X | X | X | X | MAP_CH1234_TO_OUT4A |
| | 1 | | | | | | | | X | X | X | X | | | | | MAP_CH1234_TO_OUT4B |
| 53 | 1 | | | | | | | | | | | | X | X | X | X | MAP_CH5678_TO_OUT5B |
| | 1 | | | | | | | | X | X | X | X | | | | | MAP_CH5678_TO_OUT5A |
| | 1 | | | | X | X | X | X | | | | | | | | | MAP_CH5678_TO_OUT6B |
| 54 | 1 | | | | | | | | | | | | X | X | X | X | MAP_CH5678_TO_OUT6A |
| | 1 | | | | | | | | X | X | X | X | | | | | MAP_CH5678_TO_OUT7B |
| | 1 | | | | X | X | X | X | | | | | | | | | MAP_CH5678_TO_OUT7A |
| 55 | 1 | | | | | | | | | | | | X | X | X | X | MAP_CH5678_TO_OUT8B |
| | 1 | | | | | | | | X | X | X | X | | | | | MAP_CH5678_TO_OUT8A |

Input channels 1 to 4 can be mapped to any LVDS output (OUT1A, OUT1B to OUT4A, OUT4B) using the MAP_CH1234_TO_OUTnA, MAP_CH1234_TO_OUTnB bits, as shown in Table 16.

**Table 16. Multiplexing IN1 to IN4**

| MAP_CH1234_TO_OUTN[3:0](1) | MAPPING | USED IN ONE-WIRE MODE? | USED IN TWO-WIRE MODE? |
|---|---|---|---|
| 0000 | ADC input channel IN1 to OUT*n* | Y | Y (LSB byte) |
| 0001 | ADC input channel IN1 to OUT*n* (two-wire only) | N | Y (MSB byte) |
| 0010 | ADC input channel IN2 to OUT*n* | Y | Y (LSB byte) |
| 0011 | ADC input channel IN2 to OUT*n* (two-wire only) | N | Y (MSB byte) |
| 0100 | ADC input channel IN3 to OUT*n* | Y | Y (LSB byte) |
| 0101 | ADC input channel IN3 to OUT*n* (two-wire only) | N | Y (MSB byte) |
| 0110 | ADC input channel IN4 to OUT*n* | Y | Y (LSB byte) |
| 0111 | ADC input channel IN4 to OUT*n* (two-wire only) | N | Y (MSB byte) |
| 1xxx | LVDS output buffer OUT*n* powered down | — | — |

(1) n = 1A, 1B, 2A, 2B, 3A, 3B, 4A, or 4B.

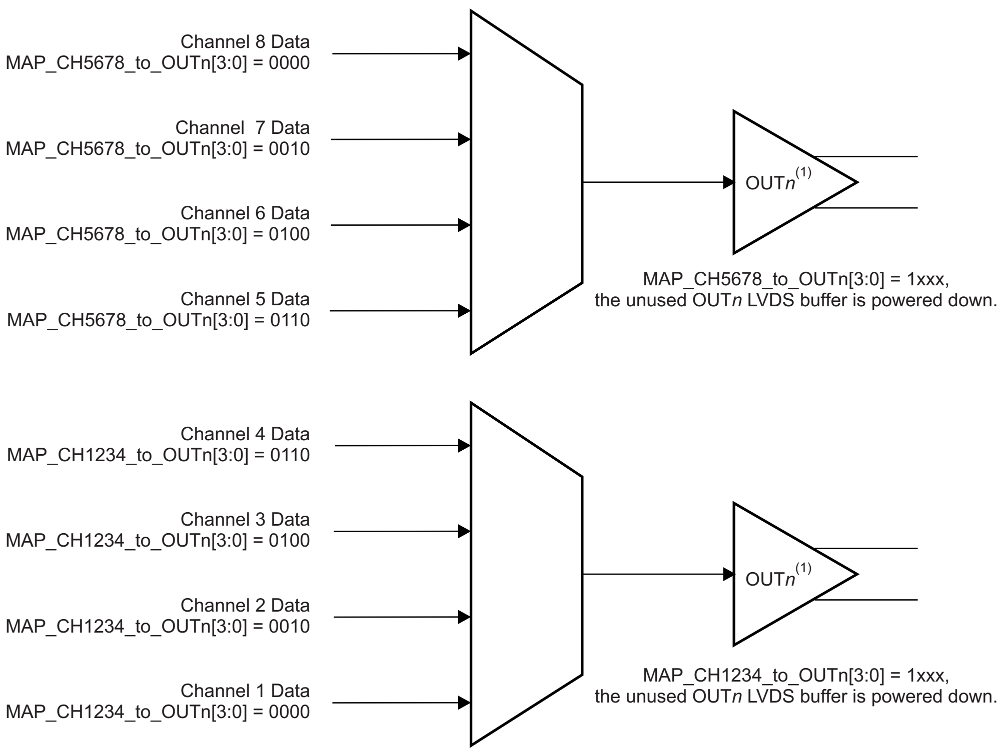
 

Similarly, input channels 5 to 8 can be mapped to any LVDS output (OUT5A, OUT5B to OUT8A, OUT8B) using the MAP_CH5678_TO_OUTnA, MAP_CH5678_TO_OUTnB bits, as shown in Table 17. Both multiplexing options are controlled by registers 50h to 55h. Channel mapping block diagrams for one-wire mode and two-wire mode are illustrated in Figure 64 and Figure 65, respectively.

**Table 17. Multiplexing IN5 to IN8**

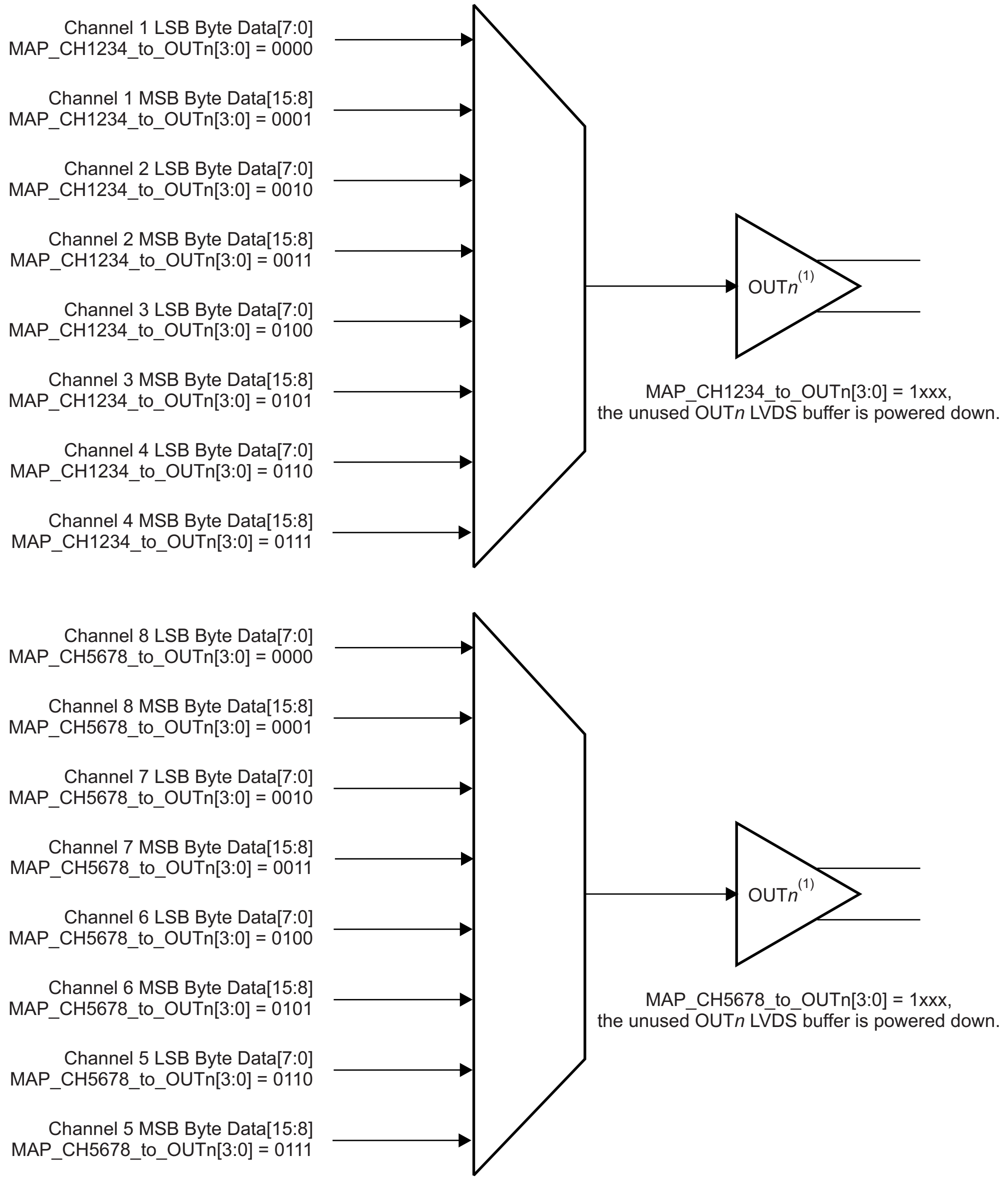
| MAP_CH5678_TO_OUTN[3:0](1) | MAPPING | USED IN ONE-WIRE MODE? | USED IN TWO-WIRE MODE? |
|---|---|---|---|
| 0000 | ADC input channel IN8 to OUT*n* | Y | Y (LSB byte) |
| 0001 | ADC input channel IN8 to OUT*n* (two-wire only) | N | Y (MSB byte) |
| 0010 | ADC input channel IN7 to OUT*n* | Y | Y (LSB byte) |
| 0011 | ADC input channel IN7 to OUT*n* (two-wire only) | N | Y (MSB byte) |
| 0100 | ADC input channel IN6 to OUT*n* | Y | Y (LSB byte) |
| 0101 | ADC input channel IN6 to OUT*n* (two-wire only) | N | Y (MSB byte) |
| 0110 | ADC input channel IN5 to OUT*n* | Y | Y (LSB byte) |
| 0111 | ADC input channel IN5 to OUT*n* (two-wire only) | N | Y (MSB byte) |
| 1xxx | LVDS output buffer OUT*n* powered down | — | — |

(1) n = 5A, 5B, 6A, 6B, 7A, 7B, 8A, or 8B.




(1) For channels 1 to 4, n = 1A, 1B, 2A, 2B, 3A, 3B, 4A, and 4B. For channels 5 to 8, n = 5A, 5B, 6A, 6B, 7A, 7B, 8A, and 8B.

**Figure 64. One-Wire Channel Mapping Mode**




(1) For channels 1 to 4, n = 1A, 1B, 2A, 2B, 3A, 3B, 4A, and 4B. For channels 5 to 8, n = 5A, 5B, 6A, 6B, 7A, 7B, 8A, and 8B.

**Figure 65. Two-Wire Channel Mapping Mode**

The default mapping for the one-wire and two-wire modes is shown in Table 18 and Table 19, respectfully.

**Table 18. Mapping for One-Wire Mode**

| ANALOG INPUT CHANNEL | LVDS OUTPUT(1) |
|---|---|
| Channel IN1 | OUT1A |
| Channel IN2 | OUT2A |
| Channel IN3 | OUT3A |
| Channel IN4 | OUT4A |
| Channel IN5 | OUT5A |
| Channel IN6 | OUT6A |
| Channel IN7 | OUT7A |
| Channel IN8 | OUT8A |

(1) ADC data are only available on OUT*n*A with default register settings.

**Table 19. Mapping for Two-Wire Mode**

| ANALOG INPUT CHANNEL | LVDS OUTPUT(1) |
|---|---|
| Channel IN1 | OUT1A, OUT1B |
| Channel IN2 | OUT2A, OUT2B |
| Channel IN3 | OUT3A, OUT3B |
| Channel IN4 | OUT4A, OUT4B |
| Channel IN5 | OUT5A, OUT5B |
| Channel IN6 | OUT6A, OUT6B |
| Channel IN7 | OUT7A, OUT7B |
| Channel IN8 | OUT8A, OUT8B |

(1) ADC data are available on both OUT*n*A and OUT*n*B.

## SYNCHRONIZATION USING THE SYNC PIN

The SYNC pin can be used to synchronize the data output from channels within the same chip or from channels across multiple chips when decimation filters are used with a reduced output data rate. When decimation filters are used (if the decimate-by-2 filter is enabled, for example), then effectively, the device outputs one digital code for every two analog input samples. If the SYNC pulse is not used, then the filters are not synchronized (even within a chip). When the filters are not synchronized, one channel may be transmitting codes corresponding to input samples N, N+1, and so on, while another channel may be transmitting codes corresponding to N+1, N+2, and so on.

To achieve synchronization across multiple chips, the SYNC pulse must arrive at all ADS5295 chips at the same time (as shown in Figure 66). The ADS5295 generates an internal synchronization signal that resets the internal clock dividers used by the decimation filter. Using the SYNC signal in this way ensures that all channels output digital codes corresponding to the same set of input samples.

Synchronizing the filters using the SYNC pin is enabled by default. No register bits are required to be written. The TP_HARD_SYNC register bit must be reset to '0' for this mode to function properly. As shown in Figure 66, the SYNC rising edge can be positioned anywhere within the window. SYNC width must be at least one clock cycle.

In addition, SYNC can also be used to synchronize the RAMP test patterns across channels. In order to synchronize the test patterns, TP_HARD_SYNC must be set to '1'. Setting TP_HARD_SYNC to '1' actually disables the sync of the filters.

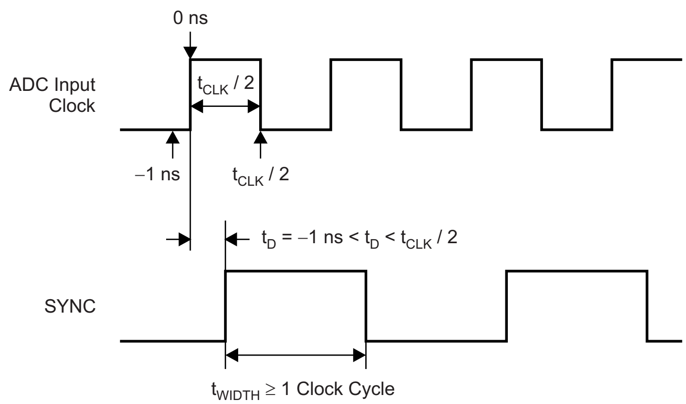



**Figure 66. SYNC Timing Diagram**

### Synchronizing ADC Sampling Instants

Note that SYNC does not and cannot be used to synchronize the ADC sampling instants across chips. All channels within a single chip sample the analog inputs simultaneously. To ensure that channels across two chips sample the analog inputs simultaneously, the input clock must be routed to both chips with an identical length. This layout ensures that the input clocks arrive at both chips at the same time. Therefore, the SYNC pin cannot be used to synchronize the sampling instants because the input clock routing must be implemented during board design.

# DIGITAL OUTPUT INTERFACE

## SERIAL LVDS INTERFACE

The ADS5295 offers several flexible output options, making the device easy to interface to an application-specific integrated circuit (ASIC) or a field-programmable gate array (FPGA). Each option can be easily programmed using the serial interface. A summary of all available options is listed in Table 20 along with the default values after power-up and reset. Following Table 20, each option is described in detail. Table 21 lists the two-wire register settings for the LVDS interface.

**Table 20. Summary of Output Interface Options**

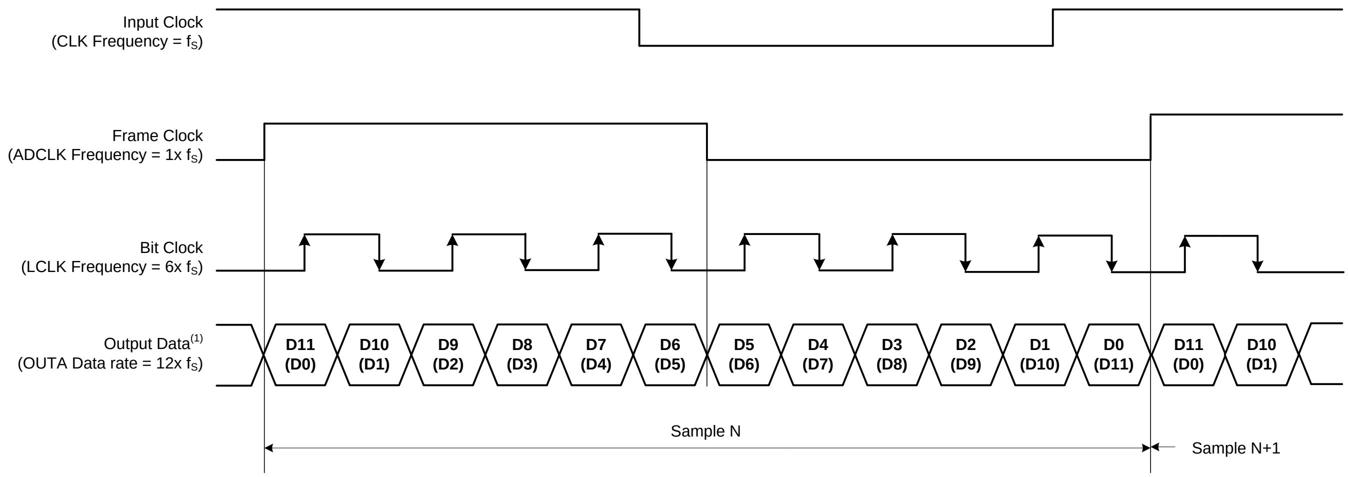
| FEATURE | OPTIONS | AVAILABLE IN: ONE-WIRE | AVAILABLE IN: TWO-WIRE | DEFAULT AFTER POWER-UP AND RESET | BRIEF DESCRIPTION |
|---|---|---|---|---|---|
| Wire interface | One- and two-wire | N | N | One-wire | One-wire: ADC data are sent serially over one pair of LVDS pins.<br>Two-wire: ADC data are split and sent serially over two pairs of LVDS pins. |
| Serialization factor | 12x | Y | Y | 12x | |
| | 10x | Y | Y | 12x | |
| | 14x | Y | Y | | To be used with digital processing functions, such as averaging and decimation filers. |
| | 16x | Y | N | | To be used with digital processing functions, such as averaging and decimation filers. |
| DDR bit clock frequency | 6x, 5x, 7x, 8x | Y | N | 6x | Only available with one-wire interface for 12x, 10x, 14x, and 16x serialization factors, respectively. |
| | 3x, 2.5x, 3.5x, 4x | N | Y | 6x | Only available with two-wire interface for 12x, 10x, 14x, and 16x serialization factors, respectively. |
| Frame clock frequency | 1x sample rate | Y | N | 1x | |
| | 1/2x sample rate | N | Y | 1x | |
| Bit sequence | Byte-wise | N | Y | Byte-wise | Only available with the two-wire interface.<br>Byte-wise: the ADC data are split into upper and lower bytes that are output on separate wires. |
| | Bit-wise | N | Y | Byte-wise | Only available with the two-wire interface.<br>Bit-wise: the ADC data are split into even and odd bits that are output on separate wires. |
| | Word-wise | N | Y | Byte-wise | Only available with the two-wire interface.<br>Word-wise: successive ADC data samples are sent over separate wires. |

**Table 21. Register Settings for Two-wire LVDS Interface**

| D15 (EN_WORD_BIT_WISE) | D8 (EN_BIT_WISE) | D[7:0] (EN_WORDWISE_BY_CH) | LVDS OUTPUT |
|---|---|---|---|
| 0 | X | X | Byte-wise mode |
| 1 | X | 1 | Word-wise mode |
| 1 | 1 | 0 | Bit-wise mode |

### One-Wire, 12x Serialization with DDR Bit Clock and 1x Frame Clock

The 12-bit ADC data are serialized and output over one LVDS pair per channel along with a 6x bit clock and a 1x frame clock, as shown in Figure 67. The output data rate is a 12x sample rate; therefore, it is suited for low sample rates.

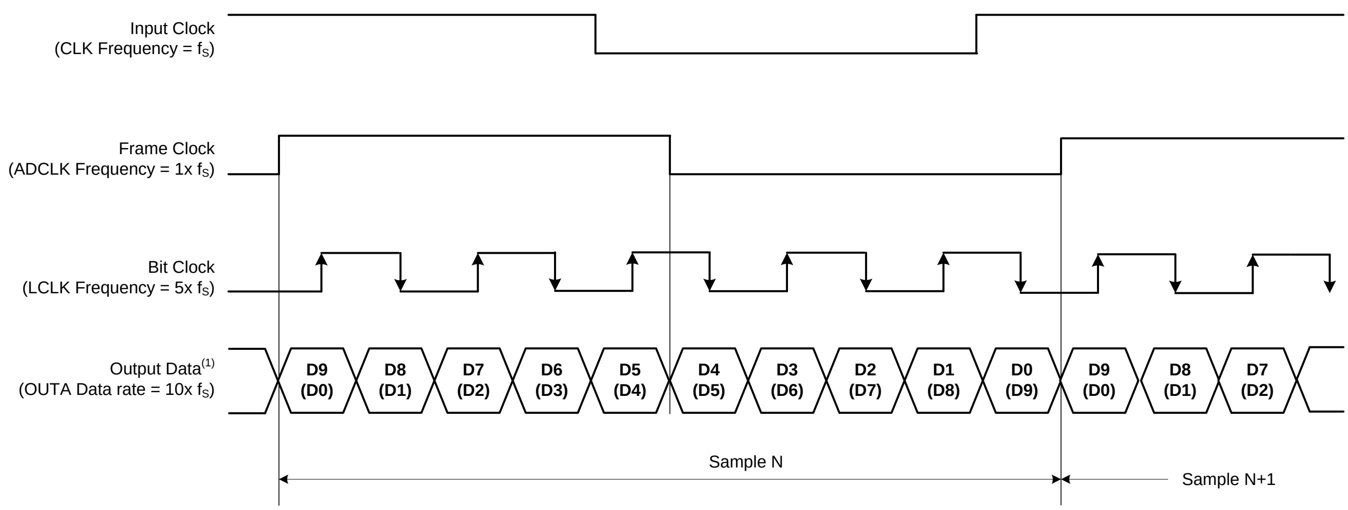



(1) The upper data bit is the MSB-first mode data bit and the lower data bit is the LSB-first mode data bit.

**Figure 67. LVDS Output Interface Timing Diagram (One-Wire, 12x Serialization)**

### One-Wire, 10x Serialization with DDR Bit Clock and 1x Frame Clock

The 10 upper bits of the 12-bit ADC data are serialized and output over one LVDS pair per channel along with a 5x bit clock and a 1x frame clock, as shown in Figure 68. The output data rate is a 10x sample rate; therefore, it is suited for low sample rates, typically up to 65 MSPS.

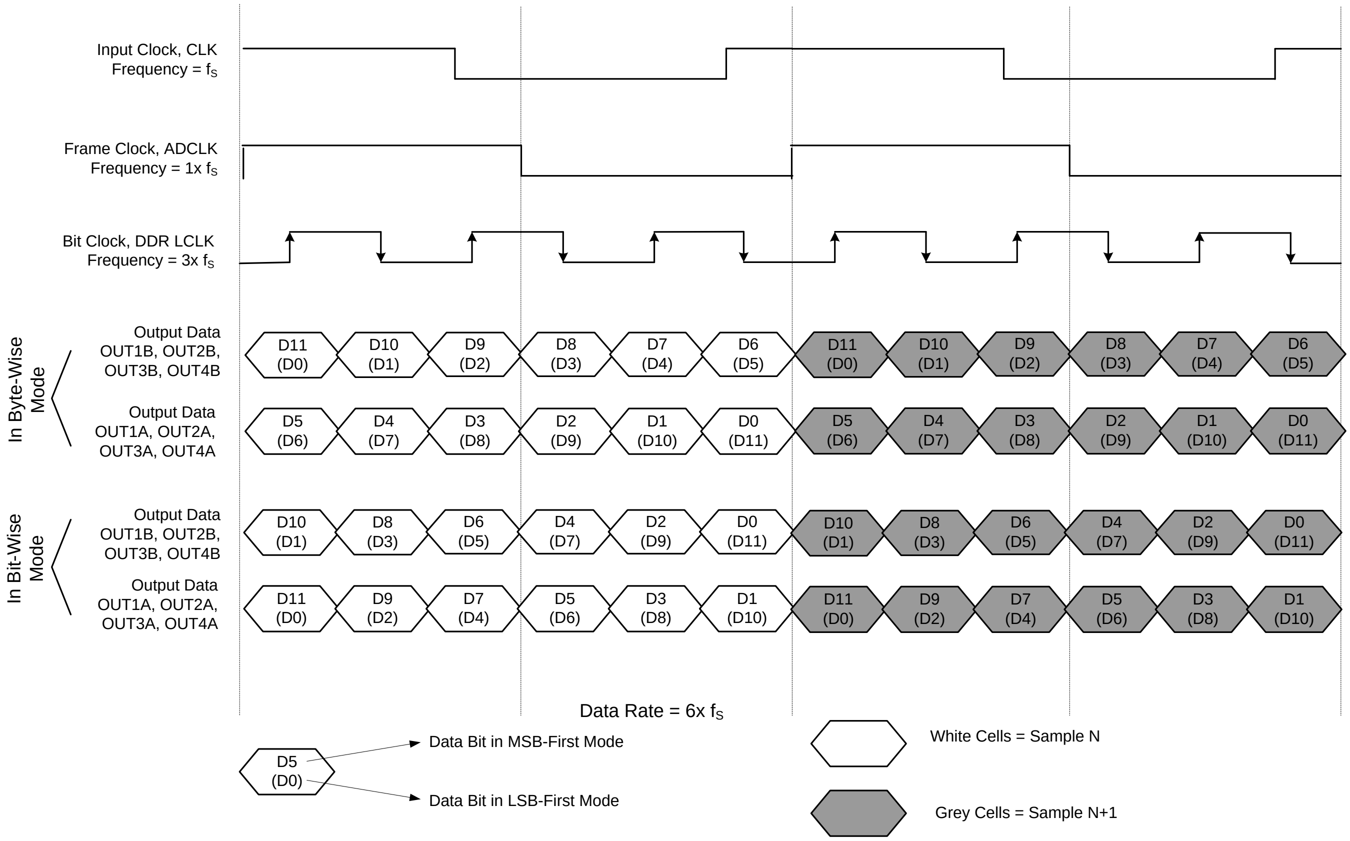



(1) The upper data bit is the MSB-first mode data bit and the lower data bit is the LSB-first mode data bit.

**Figure 68. LVDS Output Interface Timing Diagram (One-Wire, 10x Serialization)**

### Two-Wire, 12x Serialization with DDR Bit Clock and 1/2x Frame Clock

The 12-bit ADC data are serialized and output over two LVDS pairs per channel, as shown in Figure 69 and Figure 70. The output data rate is a 12x sample rate with a 3x bit clock and a 1/2x frame clock. This interface can be used up to the maximum sample rate of the device because the output data rate is half of the data rate in the one-wire case.




(1) The upper data bit is the MSB-first mode data bit and the lower data bit is the LSB-first mode data bit.

(2) Shaded cells correspond to N+1 samples. Unshaded cells correspond to N samples.

**Figure 69. LVDS Output Interface Timing Diagram (Two-Wire, 12x Serialization, Byte-Wise and Bit-Wise Modes)**

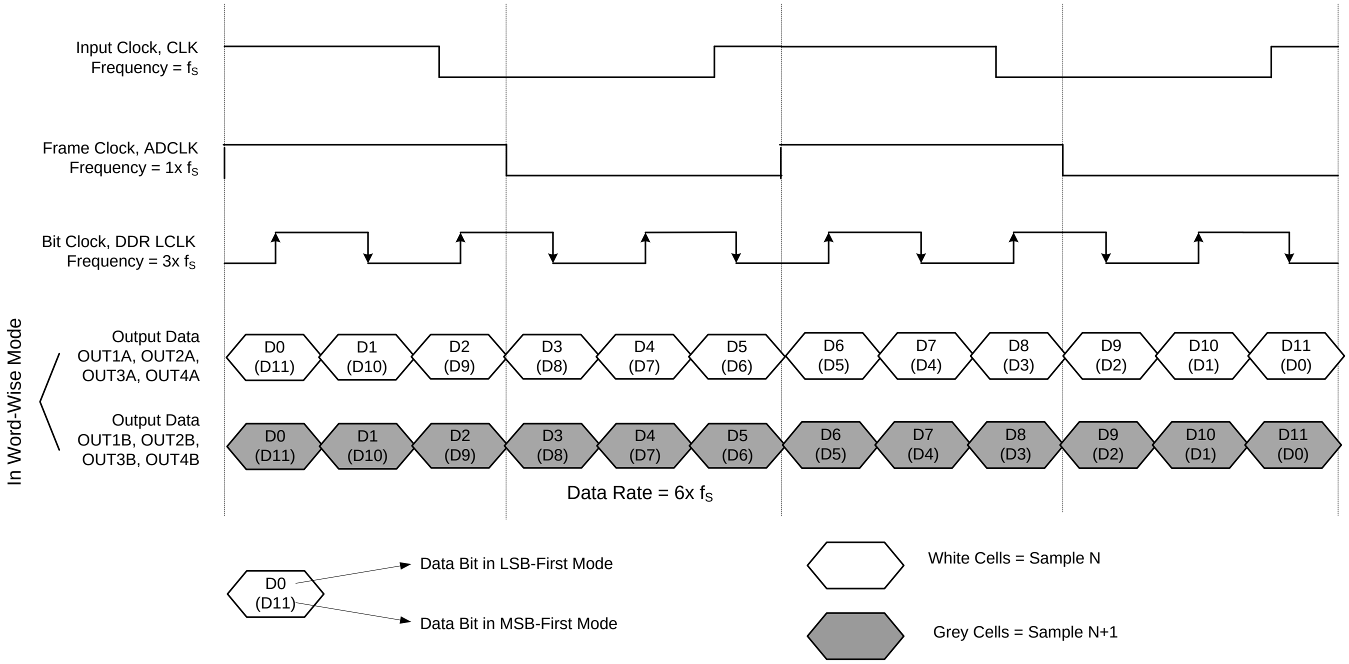
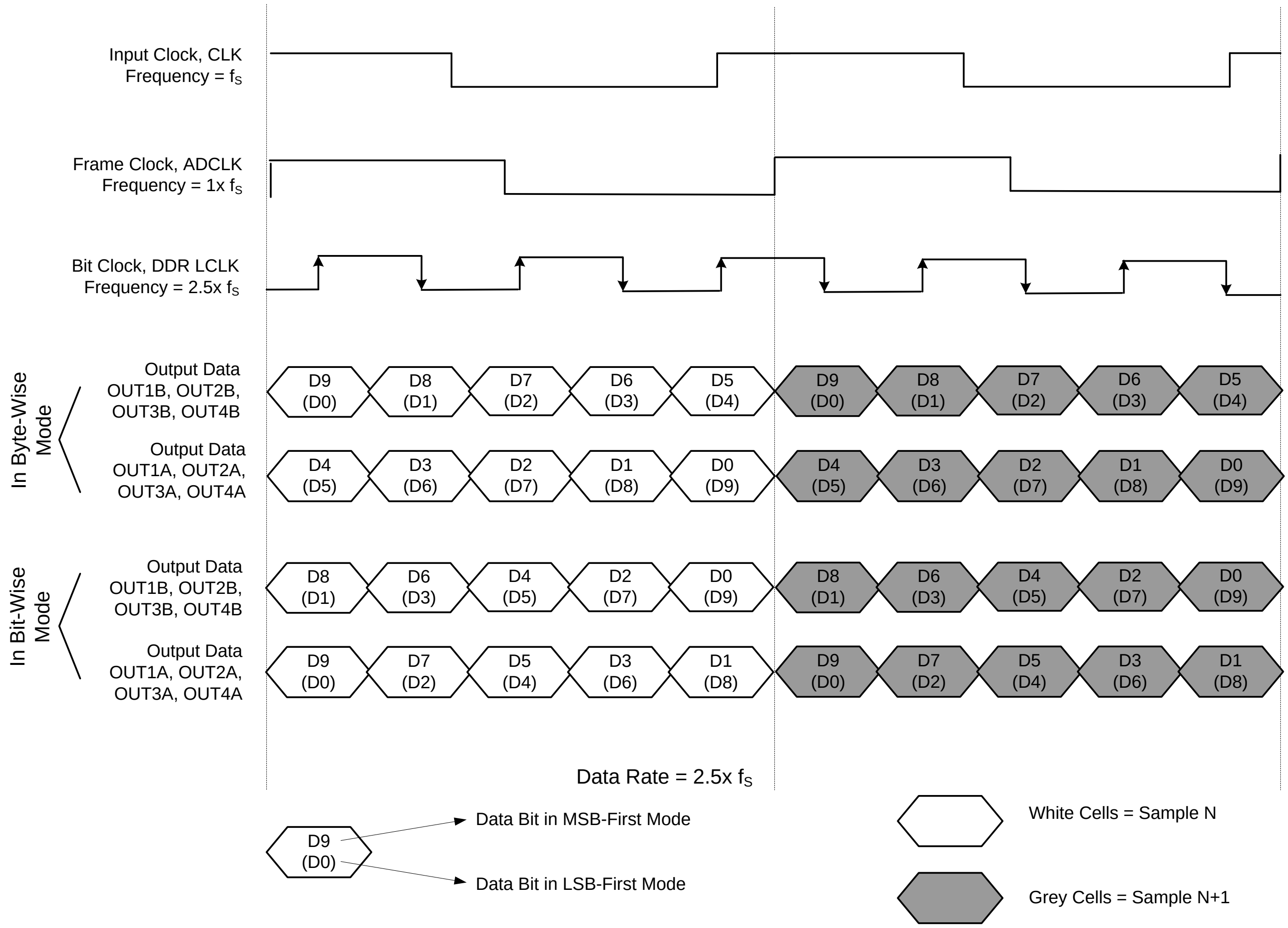



**Figure 70. LVDS Output Interface Timing Diagram (Two-Wire, 12x Serialization, Word-Wise Mode)**

### Two-Wire, 10x Serialization with DDR Bit Clock and 1/2x Frame Clock

The 10 upper bits of the 12-bit ADC data are serialized and output over two LVDS pairs per channel, as shown in Figure 71. The output data rate is a 5x sample rate per wire with a 2.5x bit clock and a 1/2x frame clock. This interface can be used up to the maximum sample rate of the device because the output data rate is half of the data rate in the one-wire case.




(1) The upper data bit is the MSB-first mode data bit and the lower data bit is the LSB-first mode data bit.

(2) Shaded cells correspond to N+1 samples. Unshaded cells correspond to N samples.

**Figure 71. LVDS Output Interface Timing Diagram (Two-Wire, 10x Serialization)**

When digital signal processing functions are used, the 14x and 16x serialization modes can also be used. These modes are:

- One-wire, 14x and 16x serialization with DDR bit clock and 1x frame clock mode, and
- Two-wire, 14x with DDR bit clock and 1/2x frame clock mode.

## PROGRAMMABLE LCLK PHASE

The ADS5295 enables the edge of the output bit clock (LCLK) to be programmed with the PHASE_DDR register bits. The default value of PHASE_DDR after reset is '10'. The default phase is shown in Figure 72.

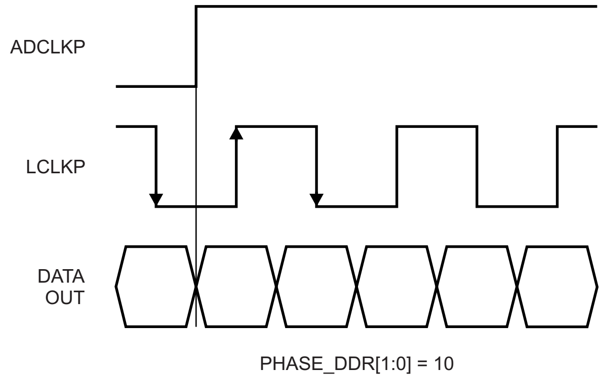



**Figure 72. Default LCLK Phase**

The phase can also be changed by changing the value of the PHASE_DDR[1:0] bits, as shown in Figure 73.

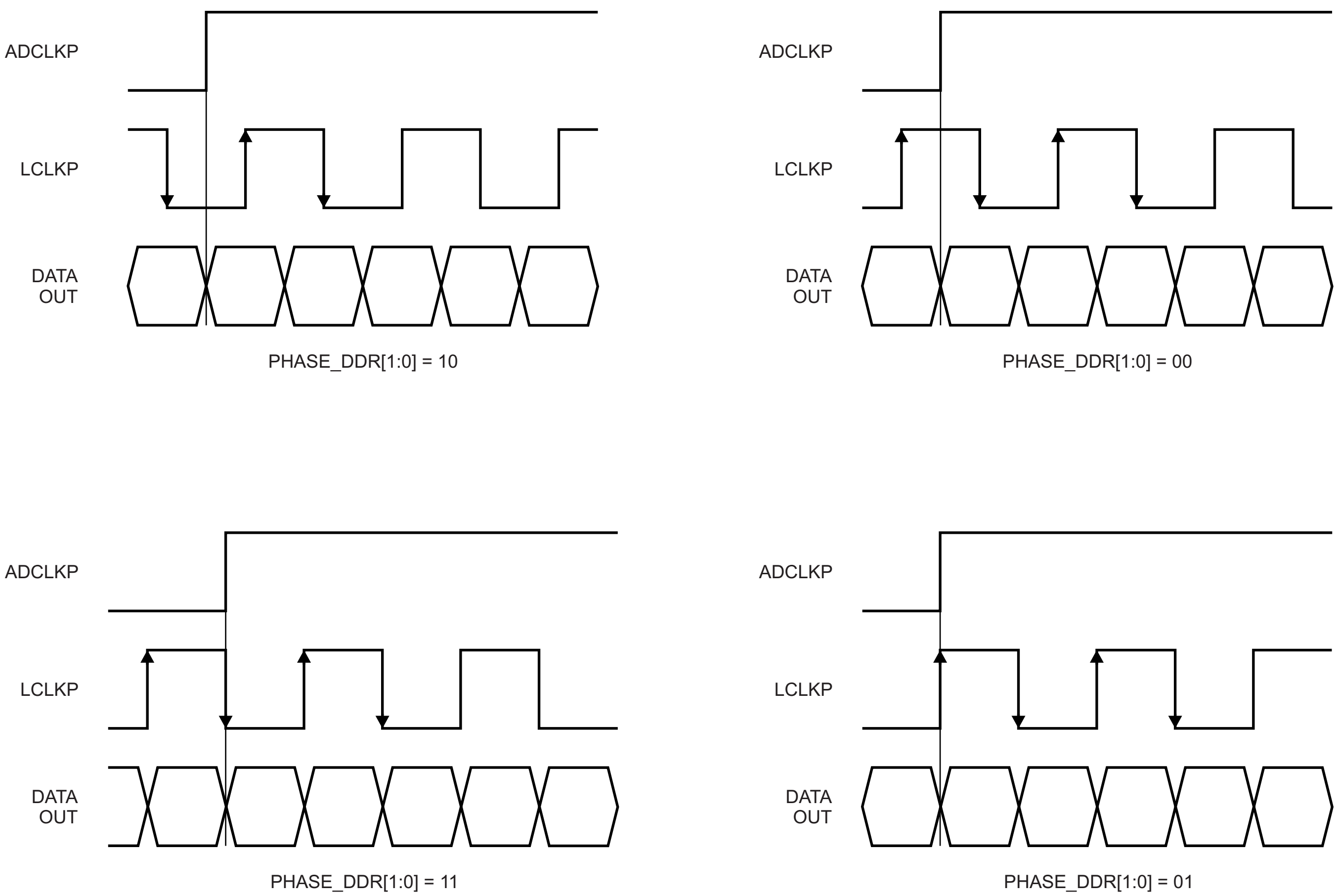



**Figure 73. Programmable LCLK Phases**

## PROGRAMMABLE LVDS OUTPUT CLOCK AND DATA EDGES

The ADS5295 enables the edges of the output data and output bit clock to be programmed with the DELAY_DATA and DELAY_LCLK register bits.

Figure 74 details the timing of the output data and clock edge movements. Table 22 and Table 23 show the register settings and corresponding delay values for the data and clock edge movements.

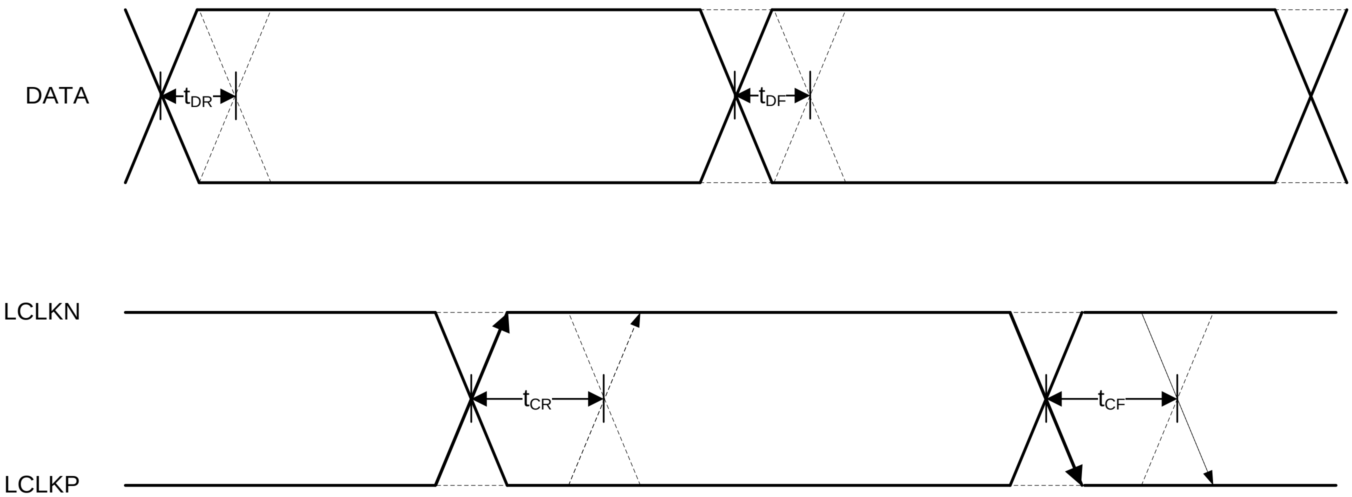



**Figure 74. LVDS Interface Output Data and Clock Edge Movement**

**Table 22. LVDS Interface Output Data Delay Settings(1)**

| DELAY_DATA_R[1:0] | | DATA DELAY, RISING CLOCK EDGE $t_{DR}$, Typical (ps) | DELAY_DATA_F[1:0] | | DATA DELAY, FALLING CLOCK EDGE $t_{DF}$, Typical (ps) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 33 | 0 | 1 | 33 |
| 1 | 0 | 72 | 1 | 0 | 72 |
| 1 | 1 | 120 | 1 | 1 | 120 |

(1) Delay settings are the same for both 10x and 12x serialization modes.

**Table 23. LVDS Interface Output Clock Delay Settings(1)**

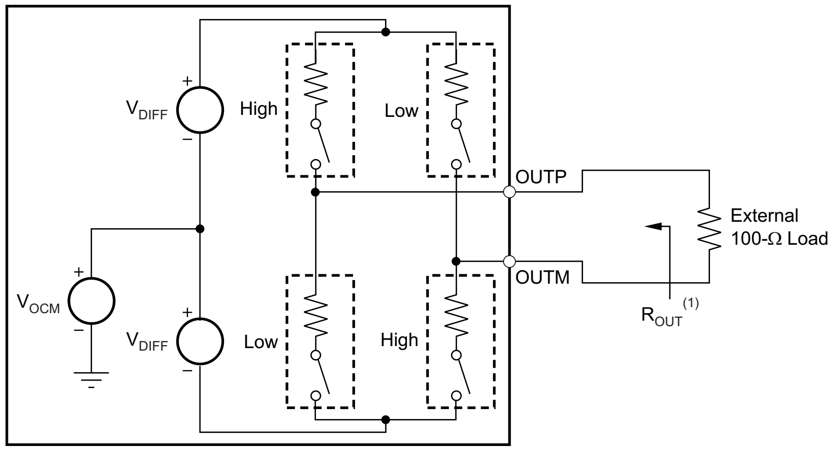
| DELAY_LCLK_R[2:0] | | | CLOCK RISING EDGE DELAY $t_{CR}$, Typical (ps) | DELAY_LCLK_F[2:0] | | | CLOCK FALLING EDGE DELAY $t_{CF}$, Typical (ps) |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 33 | 0 | 0 | 1 | 33 |
| 0 | 1 | 0 | 72 | 0 | 1 | 0 | 72 |
| 0 | 1 | 1 | 120 | 0 | 1 | 1 | 120 |
| 1 | 0 | 0 | 106 | 1 | 0 | 0 | 106 |
| 1 | 0 | 1 | 159 | 1 | 0 | 1 | 159 |
| 1 | 1 | 0 | 202 | 1 | 1 | 0 | 202 |
| 1 | 1 | 1 | 244 | 1 | 1 | 1 | 244 |

(1) Delay settings are the same for both 10x and 12x serialization modes.

## LVDS OUTPUT DATA AND CLOCK BUFFERS

The equivalent circuit of each LVDS output buffer is shown in Figure 75. After reset, the buffer presents an output impedance of 100 Ω to match with the external 100-Ω termination.

The $V_{DIFF}$ voltage is nominally 350 mV, resulting in an output swing of ±350 mV with a 100-Ω external termination. The buffer output impedance behaves in the same way as a source-side series termination. By absorbing reflections from the receiver end, this impedance helps improve signal integrity.




(1) $R_{OUT}$ = 100 Ω.

**Figure 75. LVDS Buffer Equivalent Circuit**

## OUTPUT DATA FORMAT

Two output data formats are supported: twos complement and offset binary. These formats can be selected by the BTC_MODE serial interface register bit. In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level. For a positive overload, the 12-bit output data (D[11:0]) is FFFh in offset binary output format and 7FFh in twos complement output format. For a negative input overload, the output data is 000h in offset binary output format and 800h in twos complement output format.

## BOARD DESIGN CONSIDERATIONS

### Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See the EVM User Guide (*ADS5295, 8-Channel ADC Evaluation Module*, SLAU442) for details on layout and grounding.

### Supply Decoupling

Minimal external decoupling can be used without loss in performance because the ADS5295 already includes internal decoupling. Note that decoupling capacitors can help filter external power-supply noise; thus, the optimum number of capacitors would depend on the actual application. The decoupling capacitors should be placed very close to the converter supply pins.

### Exposed Pad

In addition to providing a path for heat dissipation, the pad is also electrically connected to the digital ground internally. Therefore, the exposed pad must be soldered to the ground plane for best thermal and electrical performance.

## DEFINITION OF SPECIFICATIONS

**Analog Bandwidth:** The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value.

**Aperture Delay:** The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay is different across channels. The maximum variation is specified as aperture delay variation (channel-to-channel).

**Aperture Uncertainty (jitter):** The sample-to-sample variation in aperture delay.

**Clock Pulse Width (duty cycle):** The duty cycle of a clock signal is the ratio of the time that the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

**Maximum Conversion Rate:** The maximum sampling rate at which specified operation is given. All parametric testing is performed at this sampling rate, unless otherwise noted.

**Minimum Conversion Rate:** The minimum sampling rate at which the ADC functions.

**Differential Nonlinearity (DNL):** An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

**Integral Nonlinearity (INL):** INL is the deviation of the ADC transfer function from a best-fit line determined by a least-squares curve fit of that transfer function, measured in units of LSBs.

**Gain Error:** Gain error is the deviation of the actual ADC input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error as a result of reference inaccuracy and error as a result of the channel. Both errors are specified independently as $E_{GREF}$ and $E_{GCHAN}$, respectively. To a first-order approximation, the total gain error is ($E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$). For example, if $E_{TOTAL} = \pm 0.5\%$, then the full-scale input varies from $[(1 – 0.5 / 100) \times FS_{IDEAL}]$ to $[(1 + 0.5 / 100) \times FS_{IDEAL}]$.

**Offset Error:** Offset error is the difference, given in number of LSBs, between the actual average ADC idle channel output code and the ideal average idle channel output code. This quantity is often mapped into millivolts.

**Temperature Drift:** The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from $T_{MIN}$ to $T_{MAX}$. Drift is calculated by dividing the maximum deviation of the parameter across the $T_{MIN}$ to $T_{MAX}$ range by the difference of $T_{MAX} – T_{MIN}$.

**Signal-to-Noise Ratio (SNR):** SNR is the ratio of the power of the fundamental ($P_S$) to the noise floor power ($P_N$), excluding the power at dc and the first nine harmonics. SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

$$SNR = 10\, Log^{10} \frac{P_S}{P_N} \quad (8)$$

**Signal-to-Noise and Distortion (SINAD):** SINAD is the ratio of the power of the fundamental ($P_S$) to the power of all the other spectral components, including noise ($P_N$) and distortion ($P_D$), but excluding dc. SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

$$SINAD = 10\, Log^{10} \frac{P_S}{P_N + P_D} \quad (9)$$

**Effective Number of Bits (ENOB):** ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (10)$$

**Total Harmonic Distortion (THD):** THD is the ratio of the power of the fundamental ($P_S$) to the power of the first nine harmonics ($P_D$). THD is typically given in units of dBc (dB to carrier).

$$THD = 10\, Log^{10} \frac{P_S}{P_N} \quad (11)$$

**Spurious-Free Dynamic Range (SFDR):** SFDR is the ratio of power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

**Two-Tone Intermodulation Distortion (IMD3):** IMD3 is the ratio of the power of the fundamental (at frequencies $f_1$ and $f_2$) to the power of the worst spectral component at either frequency $2f_1 – f_2$ or $2f_2 – f_1$. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

**AC Power-Supply Rejection Ratio (AC PSRR):** AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If $\Delta V_{SUP}$ is the change in supply voltage and $\Delta V_{OUT}$ is the resultant change of the ADC output code (referred to the input), then:

$$PSRR = 20\ Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{SUP}} \qquad \text{(Expressed in dBc)} \tag{12}$$

**Voltage Overload Recovery:** The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. This recovery is tested by separately applying a sine-wave signal with 6-dB positive and negative overload. The deviation of the first few samples after the overload (from the expected values) is noted.

**Common-Mode Rejection Ratio (CMRR):** CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If $\Delta V_{CM\_IN}$ is the change in the common-mode voltage of the input pins and $\Delta V_{OUT}$ is the resulting change of the ADC output code (referred to the input), then:

$$CMRR = 20\ Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{CM}} \qquad \text{(Expressed in dBc)} \tag{13}$$

**CROSSTALK:** (only for multichannel ADCs) Crosstalk is a measure of the internal coupling of a signal from an adjacent channel into the channel of interest. Crosstalk is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from a channel across the package (far-channel). Crosstalk is usually measured by applying a full-scale signal in the adjacent channel. Crosstalk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. Crosstalk is typically expressed in dBc.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS5295PFP | ACTIVE | HTQFP | PFP | 80 | 96 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | ADS5295 | Samples |
| ADS5295PFPR | ACTIVE | HTQFP | PFP | 80 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | ADS5295 | Samples |
| ADS5295PFPT | ACTIVE | HTQFP | PFP | 80 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | ADS5295 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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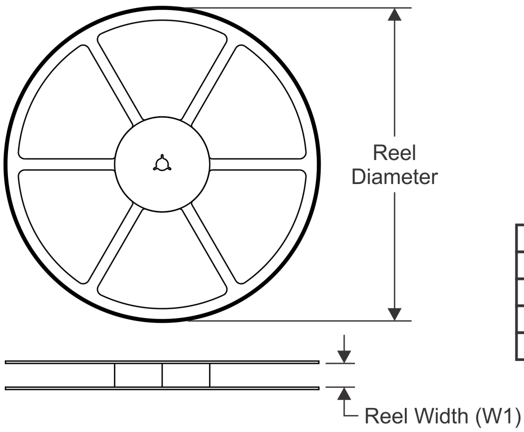
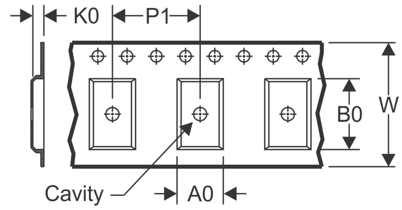
## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

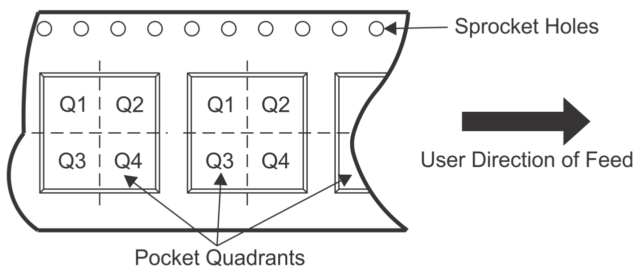



### TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

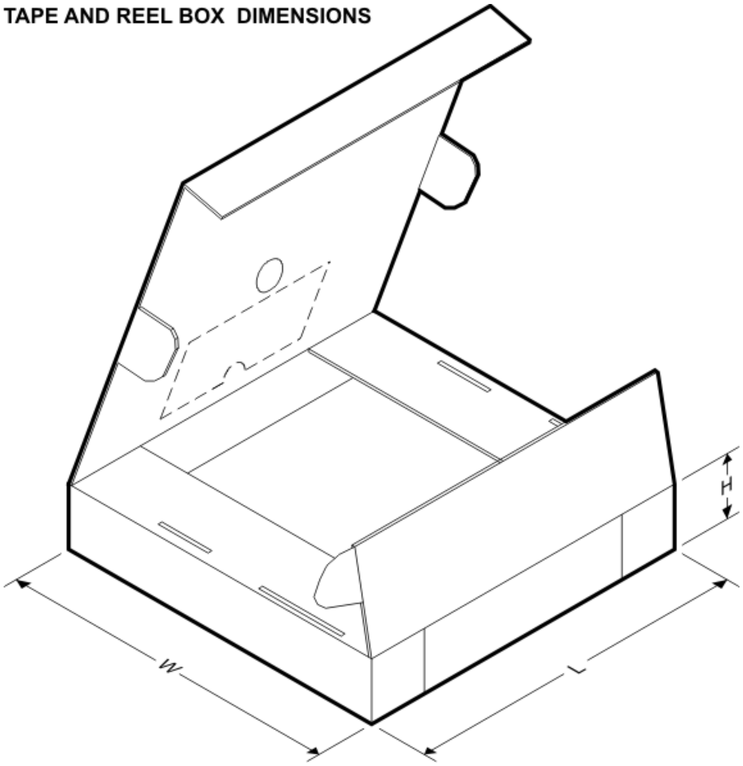
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS5295PFPR | HTQFP | PFP | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 1.5 | 20.0 | 24.0 | Q2 |
| ADS5295PFPT | HTQFP | PFP | 80 | 250 | 330.0 | 24.4 | 15.0 | 15.0 | 1.5 | 20.0 | 24.0 | Q2 |

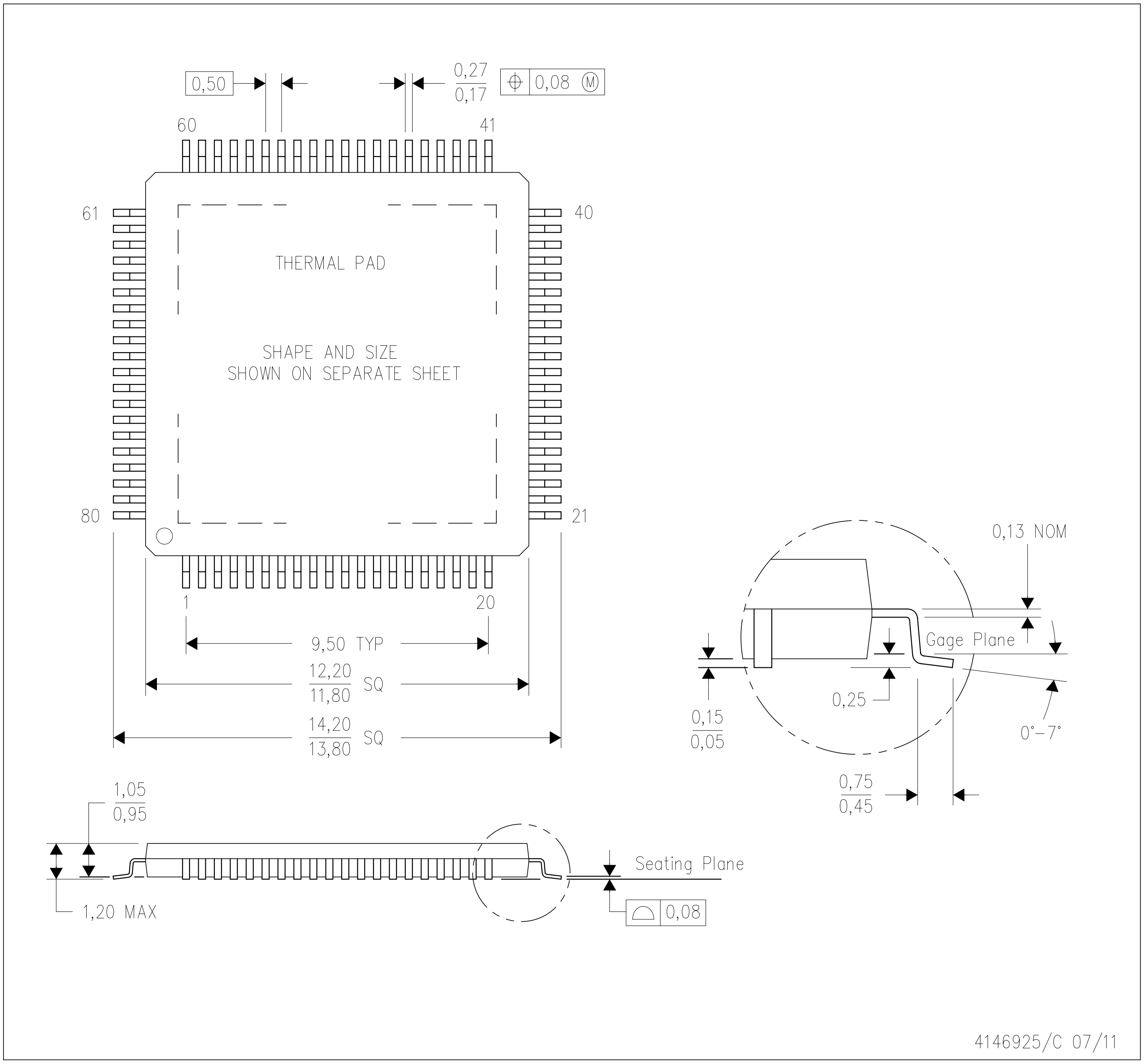
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ADS5295PFPR | HTQFP | PFP | 80 | 1000 | 367.0 | 367.0 | 45.0 |
| ADS5295PFPT | HTQFP | PFP | 80 | 250 | 367.0 | 367.0 | 45.0 |

PFP (S-PQFP-G80) PowerPAD™ PLASTIC QUAD FLATPACK




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS-026

**PowerPAD is a trademark of Texas Instruments.**

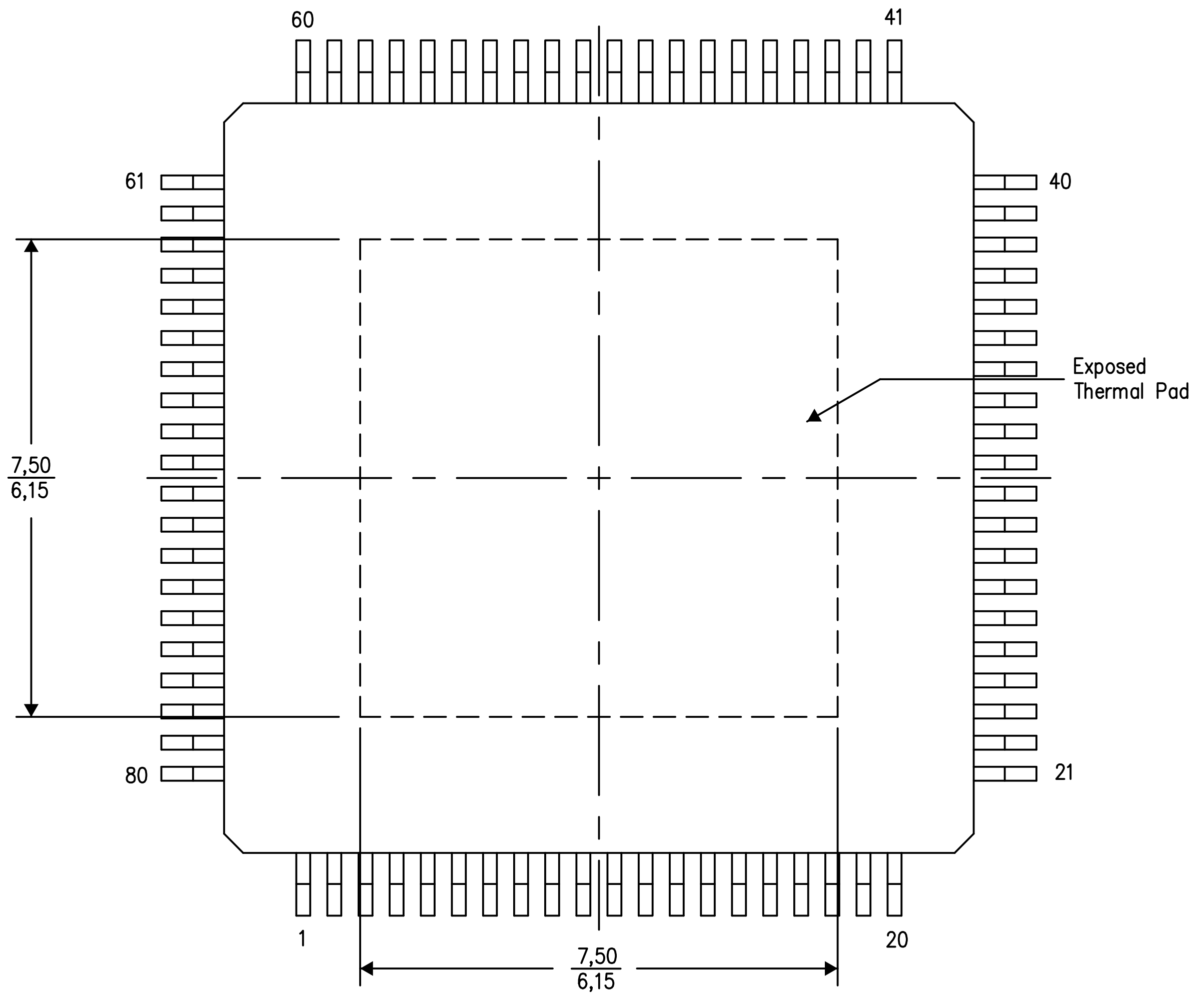
PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



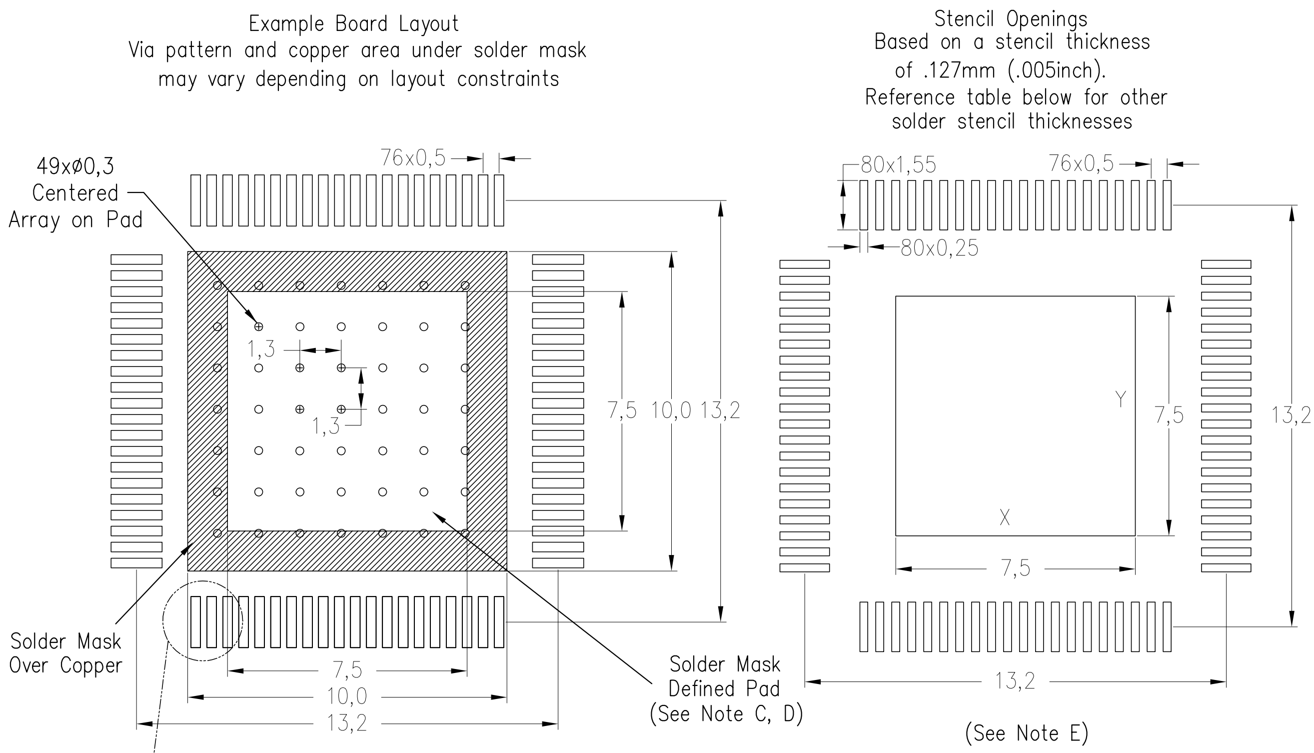

Exposed Thermal Pad Dimensions

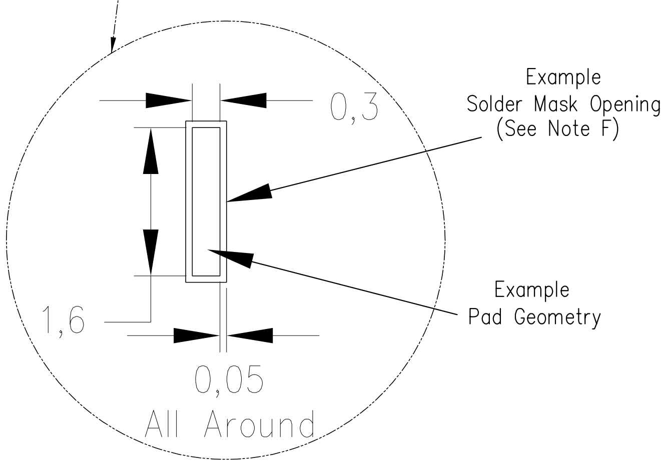
4206327–2/O 07/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 8.0 | 8.0 |
| 0.127mm | 7.5 | 7.5 |
| 0.152mm | 7.0 | 7.0 |
| 0.178mm | 6.6 | 6.6 |

4208544-2/F 09/11

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE



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