CCD ANALOG FRONT-END FOR DIGITAL CAMERAS

FEATURES

- **CCD Signal Processing:**
  - **36-MHz Correlated Double Sampling (CDS)**
- **Output Resolution:**
  - **VSP2560 (10-Bit)**
  - **VSP2562 (12-Bit)**
  - **VSP2566 (16-Bit)**
- **16-Bit Analog-to-Digital Conversion:**
  - **36-MHz Conversion Rate**
  - **No Missing Codes Ensured**
- **80-dB Input-Referred SNR (at Gain = 12 dB)**
- **Programmable Black Level Clamping**
- **Programmable Gain Amp (PGA):**
  - **–9 dB to +44 dB**
  - **–3 dB to +18 dB (Analog Front Gain)**
  - **–6 dB to +26 dB (Digital Gain)**
- **Portable Operation:**
  - **Low Voltage: 2.7 V to 3.6 V**
  - **Low Power: 86 mW at 3.0 V, 36 MHz**
  - **Low Power: 6 mW (Standby Mode)**
- **Two-Channel, General-Purpose, 8-Bit DAC**
- **QFP-48 Package**

DESCRIPTION

The VSP2560/62/66 are a family of complete mixed-signal processing ICs for digital cameras that provide correlated double sampling (CDS) and analog-to-digital conversion for the output of CCD arrays. The CDS extracts the pixel video information from the CCD signal, and the analog-to-digital converter (ADC) converts the digital signal. For varying illumination conditions, a very stable gain control of –9 dB to 44 dB is provided. The gain control is linear in dB. Input signal clamping and offset correction of the input CDS are also provided.

Offset correction is performed by the optical black (OB) level calibration loop, and is held in calibrated black level clamping for an accurate black level reference. Additionally, the black level is quickly recovered after gain changes. The VSP2560/62/66 are available in LQFP-48 packages and operate from single +3 V supplies.

PRODUCT PREVIEW

FEATURE COMPARISON BY DEVICE

DEVICE	RESOLUTION (Bits)	TRANSFER CHARACTERISTICS (LSB)		OB CLAMP LOOP (LSB)		
		DNL	INL	PROGRAMMABLE RANGE	OBCLP LEVEL	OB LEVEL
VSP2560	10	±0.5	±1	16 to 78	32	2
VSP2562	12	±0.5	±2	64 to 312	128	8
VSP2566	16	±2	±32	1024 to 4992	2048	128

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
VSP2560	QFP-48	PT	–25°C to +85°C	VSP2560	VSP2560PT	Tray, 250 Pieces
					VSP2560PTR	Tape and Reel
VSP2562	QFP-48	PT	–25°C to +85°C	VSP2562	VSP2562PT	Tray, 250 Pieces
					VSP2562PTR	Tape and Reel
VSP2566	QFP-48	PT	–25°C to +85°C	VSP2566	VSP2566PT	Tray, 250 Pieces
					VSP2566PTR	Tape and Reel

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

	VSP2560, VSP2562, VSP2566	UNIT
Supply voltage (VCC, VDD)	+4	V
Supply voltage differences (among VCC pins)	±0.1	V
Ground voltage differences (AGND, DGND)	±0.1	V
Digital input voltage	–0.3 to (VCC + 0.3)	V
Analog input voltage	–0.3 to (VCC + 0.3)	V
Input current (all pins except supplies)	±10	mA
Ambient temperature under bias	–25 to +85	°C
Storage temperature	–55 to +125	°C
Junction temperature	+150	°C
Package temperature (IR reflow, peak)	+260	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS: VSP2560

All specifications at T_A = +25°C, all power-supply voltages = +3.0 V, and conversion rate = 36 MHz, no load, unless otherwise noted.

PARAMETER	TEST CONDITIONS	VSP2560PT			UNIT
		MIN	TYP	MAX	
RESOLUTION					
Resolution			10		Bits
CONVERSION/CLOCK RATE					
Conversion/clock rate				36	MHz
ANALOG INPUT (CCDIN)					
Input signal level for full-scale out	CDS gain = 0 dB, DPGA gain = 0 dB			1000	mV
Maximum input range	CDS gain = –3 dB , DPGA gain = 0 dB			1300	mV
Input capacitance			15		pF
Input limit		–0.3		3.3	V
TRANSFER CHARACTERISTICS					
Differential nonlinearity (DNL)	CDS gain = 0 dB, DPGA gain = 0 dB		±0.5		LSB
Integral nonlinearity (INL)	CDS gain = 0 dB, DPGA gain = 0 dB		±1		LSB
No missing codes			Ensured		
Step response settling time	Full-scale step input		1		Pixel
Overload recovery time	Step input from 1.8 V to 0 V		2		Pixels
Data latency			6		Clock
Signal-to-noise ratio (1)	Grounded input capacitor, PGA gain = 0 dB		76		dB
	Grounded input capacitor, CDS gain = +12 dB		68		dB
CCD offset correction range		–200		200	mV
INPUT CLAMP					
Clamp on-resistance			400		Ω
Clamp level			1.25		V
PROGRAMMABLE ANALOG FRONT GAIN (CDS)					
Minimum gain	Gain code = 111		–3		dB
Default gain	Gain code = 000		0		dB
Medium gain 1	Gain code = 001		6		dB
Medium gain 2	Gain code = 010		12		dB
Maximum gain	Gain code = 011		18		dB
Gain control error			0.5		dB
PROGRAMMABLE DIGITAL GAIN (DPGA)					
Programmable gain range		–6		26	dB
Gain step			0.032		dB
OPTICAL BLACK CLAMP LOOP					
Control DAC resolution			10		Bits
Loop time constant	OB loop IDAC is x1		40.7		µs
Optical black clamp level	Programmable range of clamp level	16		78	LSB
	OBCLP level at code = 01000b		32		LSB
	OB level program step		2		LSB

(1) SNR = 20 log (full-scale voltage/rms noise).

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS: VSP2562

All specifications at T_A = +25°C, all power-supply voltages = +3.0 V, and conversion rate = 36 MHz, no load, unless otherwise noted.

PARAMETER	TEST CONDITIONS	VSP2562PT			UNIT
		MIN	TYP	MAX	
RESOLUTION					
Resolution			12		Bits
CONVERSION/CLOCK RATE					
Conversion/clock rate				36	MHz
ANALOG INPUT (CCDIN)					
Input signal level for full-scale out	CDS gain = 0 dB, DPGA gain = 0 dB			1000	mV
Maximum input range	CDS gain = –3 dB , DPGA gain = 0 dB			1300	mV
Input capacitance			15		pF
Input limit		–0.3		3.3	V
TRANSFER CHARACTERISTICS					
Differential nonlinearity (DNL)	CDS gain = 0 dB, DPGA gain = 0 dB		±0.5		LSB
Integral nonlinearity (INL)	CDS gain = 0 dB, DPGA gain = 0 dB		±2		LSB
No missing codes			Ensured		
Step response settling time	Full-scale step input		1		Pixel
Overload recovery time	Step input from 1.8 V to 0 V		2		Pixels
Data latency			6		Clock
Signal-to-noise ratio (1)	Grounded input capacitor, PGA gain = 0 dB		76		dB
	Grounded input capacitor, CDS gain = +12 dB		68		dB
CCD offset correction range		–200		200	mV
INPUT CLAMP					
Clamp on-resistance			400		Ω
Clamp level			1.25		V
PROGRAMMABLE ANALOG FRONT GAIN (CDS)					
Minimum gain	Gain code = 111		–3		dB
Default gain	Gain code = 000		0		dB
Medium gain 1	Gain code = 001		6		dB
Medium gain 2	Gain code = 010		12		dB
Maximum gain	Gain code = 011		18		dB
Gain control error			0.5		dB
PROGRAMMABLE DIGITAL GAIN (DPGA)					
Programmable gain range		–6		26	dB
Gain step			0.032		dB
OPTICAL BLACK CLAMP LOOP					
Control DAC resolution			10		Bits
Loop time constant	OB loop IDAC is x1		40.7		µs
Optical black clamp level	Programmable range of clamp level	64		312	LSB
	OBCLP level at code = 01000b		128		LSB
	OB level program step		8		LSB

(1) SNR = 20 log (full-scale voltage/rms noise).

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS: VSP2566

All specifications at T_A = +25°C, all power-supply voltages = +3.0 V, and conversion rate = 36 MHz, no load, unless otherwise noted.

PARAMETER	TEST CONDITIONS	VSP2566PT			UNIT
		MIN	TYP	MAX	
RESOLUTION					
Resolution			16		Bits
CONVERSION/CLOCK RATE					
Conversion/clock rate				36	MHz
ANALOG INPUT (CCDIN)					
Input signal level for full-scale out	CDS gain = 0 dB, DPGA gain = 0 dB			1000	mV
Maximum input range	CDS gain = –3 dB , DPGA gain = 0 dB			1300	mV
Input capacitance			15		pF
Input limit		–0.3		3.3	V
TRANSFER CHARACTERISTICS					
Differential nonlinearity (DNL)	CDS gain = 0 dB, DPGA gain = 0 dB		±2		LSB
Integral nonlinearity (INL)	CDS gain = 0 dB, DPGA gain = 0 dB		±32		LSB
No missing codes			Ensured		
Step response settling time	Full-scale step input		1		Pixel
Overload recovery time	Step input from 1.8 V to 0 V		2		Pixels
Data latency			6		Clock
Signal-to-noise ratio (1)	Grounded input capacitor, PGA gain = 0 dB		76		dB
	Grounded input capacitor, CDS gain = +12 dB		68		dB
CCD offset correction range		–200		200	mV
INPUT CLAMP					
Clamp on-resistance			400		Ω
Clamp level			1.25		V
PROGRAMMABLE ANALOG FRONT GAIN (CDS)					
Minimum gain	Gain code = 111		–3		dB
Default gain	Gain code = 000		0		dB
Medium gain 1	Gain code = 001		6		dB
Medium gain 2	Gain code = 010		12		dB
Maximum gain	Gain code = 011		18		dB
Gain control error			0.5		dB
PROGRAMMABLE DIGITAL GAIN (DPGA)					
Programmable gain range		–6		26	dB
Gain step			0.032		dB
OPTICAL BLACK CLAMP LOOP					
Control DAC resolution			10		Bits
Loop time constant	OB loop IDAC is x1		40.7		µs
Optical black clamp level	Programmable range of clamp level	1024		4992	LSB
	OBCLP level at code = 01000b		2048		LSB
	OB level program step		128		LSB

(1) SNR = 20 log (full-scale voltage/rms noise).

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS: GENERAL

All specifications at T_A = +25°C, all power supply voltages = +3.0 V, and conversion rate = 36 MHz, no load, unless otherwise noted.

PARAMETER		TEST CONDITIONS	VSP2560PT, VSP2562PT, VSP2566PT MIN	TYP	MAX	UNIT
GENERAL-PURPOSE, 8-BIT DAC (CHANNELS A, B)						
Minimum output voltage		Input code = 0000 0000		0.1		V
Maximum output voltage		Input code = 1111 1111		2.9		V
Differential nonlinearity (DNL)		At input code = 0Fh to E0h		±0.25		LSB
Integral nonlinearity (INL)		At input code = 0F to E0h		±1		LSB
Offset error				±100		mV
Gain error				±5		%
Monotonicity				Ensured		
Minimum load resistance			10			kΩ
Maximum load capacitance					1000	pF
DIGITAL INPUTS						
Logic family				CMOS		
Input voltage	V_{T+}	Low-to-high threshold voltage		1.7		V
	V_{T-}	High-to-low threshold voltage		1.0		V
Input current	I_{IH}	Logic high, V_{IN} = +3 V			±20	µA
	I_{IL}	Logic low, V_{IN} = 0 V			±20	µA
Input capacitance				5		pF
Maximum input voltage			–3.0		V_{CC} + 0.3	V
DIGITAL OUTPUTS						
Logic family				CMOS		
Logic coding				Straight binary		
Output voltage	V_{OH}	Logic high	2.4			V
	V_{OL}	Logic low			0.4	V
Additional output data delay		Output data delay code = 00		0		ns
		Output data delay code = 01		2		ns
		Output data delay code = 10		4		ns
		Output data delay code = 11		6		ns
POWER SUPPLY						
Supply voltage	VCC		2.7	3.0	3.6	V
	VDD					
Power dissipation		(at 3.0 V, 36 MHz)		86		mW
Standby mode power dissipation		Clocks (SHP/SHD/ADCCK) off mode: (at 3.0 V)		6		mW
TEMPERATURE RANGE						
Operation temperature			–25		+85	°C
Thermal resistance, QFP	θ_{JA}			100		°C/W

PRODUCT PREVIEW

TIMING CHARACTERISTICS

TG HIGH-SPEED PULSE

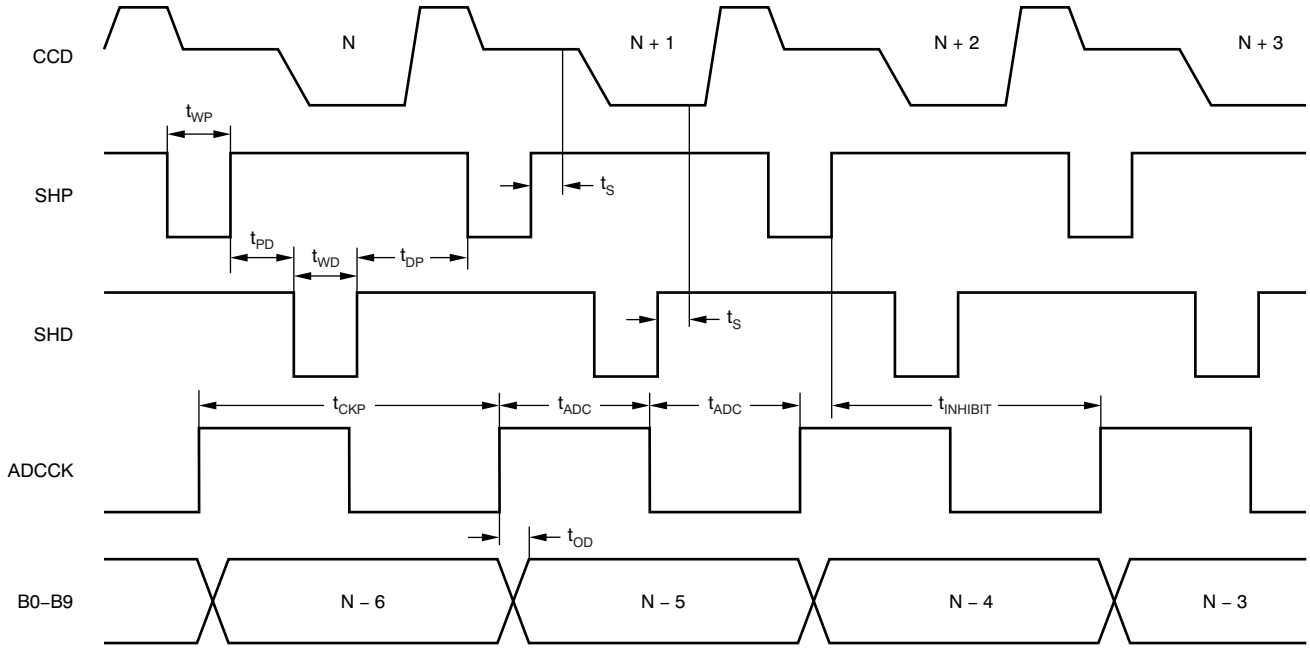


Figure 1. TG High-Speed Pulse Timing

TIMING CHARACTERISTICS FOR Figure 1

PARAMETER(1)(2)		MIN	TYP	MAX	UNIT
t_{CKP}	Clock period	27.7			ns
t_{ADC}	ADCCK high or low level		13.8		ns
t_{WP}	SHP pulse width		6.9		ns
t_{WD}	SHD pulse width		6.9		ns
t_{PD}	SHP trailing edge to SHD leading edge		6.9		ns
t_{DP}	SHD trailing edge to SHP leading edge		6.9		ns
t_S	Sampling delay		3		ns
$t_{INHIBIT}$	Inhibited clock period (from rising edge of SHP to rising edge of ADCCK)	–3		10	ns
t_{OD}	Output delay(3)	0		5	ns
DL	Data latency		6		Clocks

(1) $t_{PD} + t_{WD}$ should be nearly equal to $t_{DP} + t_{WP}$.
(2) The t_{WP} and t_{WD} specifications assume a driving impedance of less than 30 Ω at CCDIN.
(3) Data output delay by AFE-ctrl(2) register is 0 ns.

PRODUCT PREVIEW

SERIAL INTERFACE TIMING

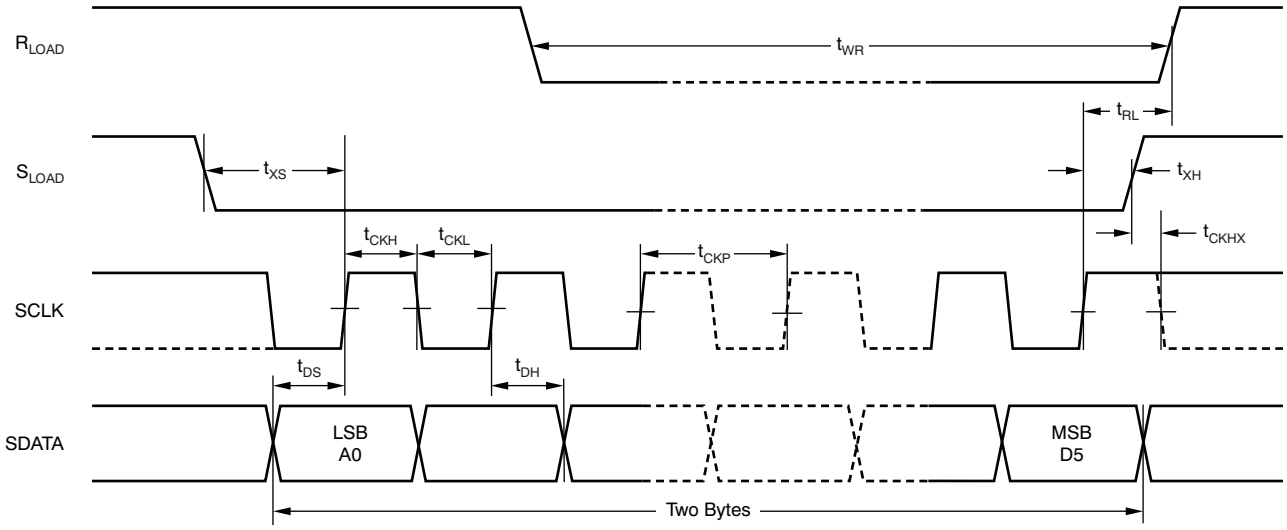


Figure 2. Serial Interface Timing

TIMING CHARACTERISTICS FOR Figure 2

PARAMETER(1)(2)		MIN	TYP	MAX	UNIT
t_{CKP}	Clock period	50			ns
t_{CKH}	Clock high pulse width	25			ns
t_{CKL}	Clock low pulse width	25			ns
t_{DS}	Data setup time	15			ns
t_{DH}	Data hold time	15			ns
t_{XS}	S_{LOAD} to SCLK setup time	20			ns
t_{XH}	SCLK to S_{LOAD} hold time	20			ns
t_{CKHX}	SCLK hold time of final SCLK	0			ns
t_{RL}	SCLK to R_{LOAD} setup time	20			ns
t_{WR}	R_{LOAD} pulse width	20			ns

(1) $t_{PD} + t_{WD}$ should be nearly equal to $t_{DP} + t_{WP}$.

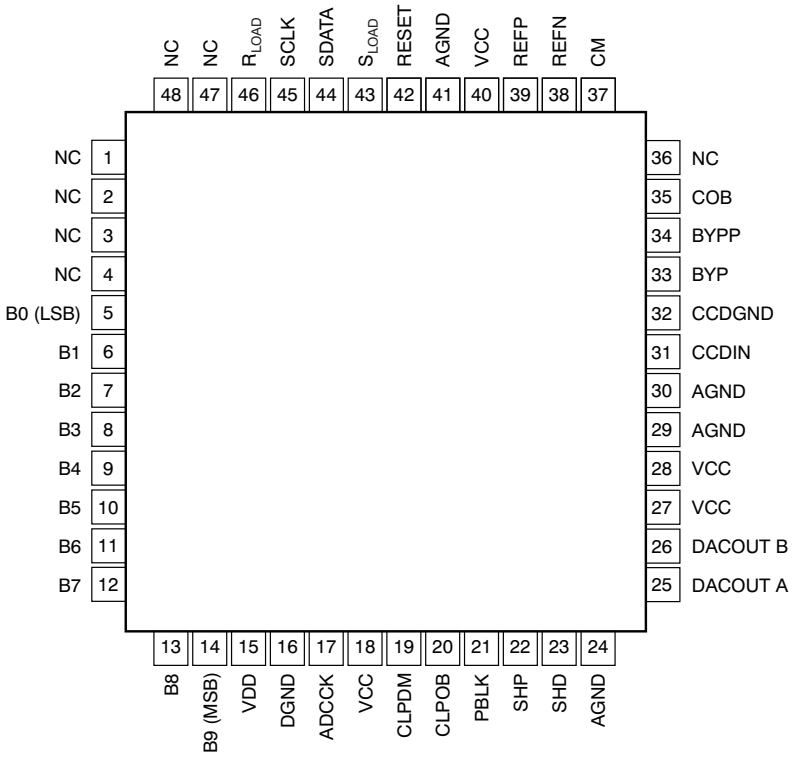
(2) The t_{WP} and t_{WD} specifications assume a driving impedance of less than 30 Ω at CCDIN.

The data shift operation should decode at the rising edges of SCLK while S_{LOAD} is low. Furthermore, the input address and data of the serial data stream are loaded to the parallel latch in the VSP2560/62/66 at the rising edge of S_{LOAD}.

PRODUCT PREVIEW

DEVICE INFORMATION

VSP2560
PT PACKAGE (QFP-48)
(TOP VIEW)



TERMINAL FUNCTIONS (VSP2560)

TERMINAL		TYPE[1]	DESCRIPTION
NAME	PIN		
NC	1	—	No connection
NC	2	—	No connection
NC	3	—	No connection
NC	4	—	No connection
B0	5	DO	Data out bit 0 (LSB)
B1	6	DO	Data out bit 1
B2	7	DO	Data out bit 2
B3	8	DO	Data out bit 3
B4	9	DO	Data out bit 4
B5	10	DO	Data out bit 5
B6	11	DO	Data out bit 6
B7	12	DO	Data out bit 7
B8	13	DO	Data out bit 8
B9	14	DO	Data out bit 9(MSB)
VDD	15	P	Digital power supply for data output
DGND	16	P	Digital ground for data output
ADCCK	17	DI	Clock for digital output buffer
VCC	18	P	Analog power supply
CLPDM	19	DI	CLPDM signal

(1) Designators in TYPE: P = power supply and ground; DI = digital input; DO = digital output; AI = analog input; and AO = analog output.

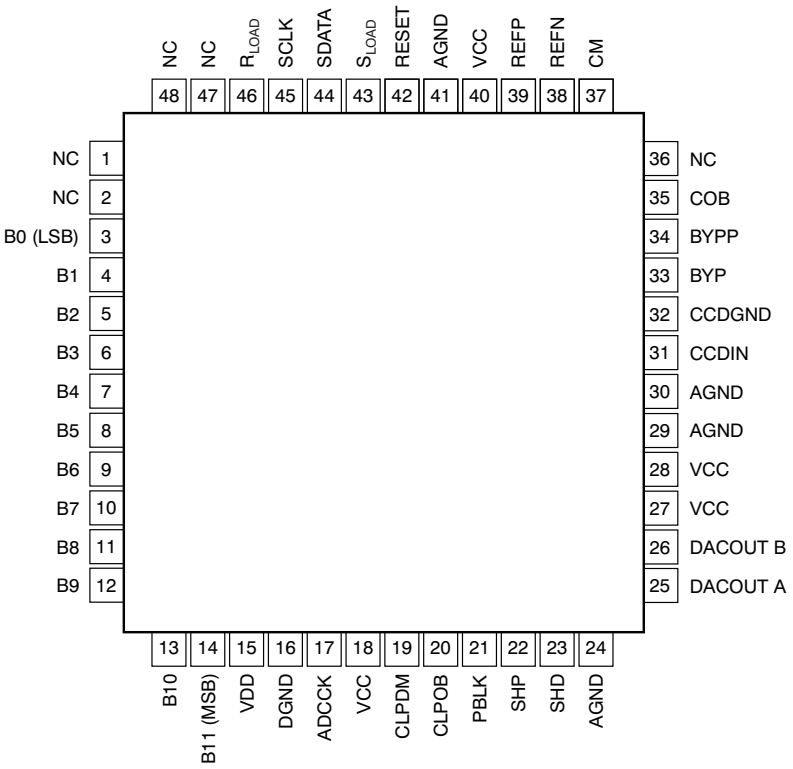
PRODUCT PREVIEW

TERMINAL FUNCTIONS (VSP2560) (continued)

TERMINAL		TYPE[1]	DESCRIPTION
NAME	PIN		
CLPOB	20	DI	CLPOB signal
PBLK	21	DI	PBLK signal
SHP	22	DI	Sampling clock for reference level of CCD signal
SHD	23	DI	Sampling clock for data level of CCD signal
AGND	24	P	Analog ground
DACOUT A	25	AO	General-purpose 8-bit DAC output A
DACOUT B	26	AO	General-purpose 8-bit DAC output B
VCC	27	P	Analog power supply
VCC	28	P	Analog power supply
AGND	29	P	Analog ground
AGND	30	P	Analog ground
CCDIN	31	AI	CCD signal input
CCDGND	32	AI	CCD signal input ground
BYP	33	AO	Internal reference bypass to ground (0.1 μF)
BYPP	34	AO	Internal reference bypass to ground (1000 pF)
COB	35	AO	OB loop feedback capacitor
NC	36	—	No connection
CM	37	AO	Internal reference bypass to ground (0.1 μF)
REFN	38	AO	Internal reference bypass to ground (0.1 μF)
REFP	39	AO	Internal reference bypass to ground (0.1 μF)
VCC	40	P	Analog power supply
AGND	41	P	Analog ground
RESET	42	DI	System reset
S_{LOAD}	43	DI	Serial data latch signal
SDATA	44	DI	Serial data input
SCLK	45	DI	Serial data clock
R_{LOAD}	46	DI	Serial data update control signal
NC	47	—	No connection
NC	48	—	No connection

PRODUCT PREVIEW

VSP2562
PT PACKAGE (QFP-48)
(TOP VIEW)



TERMINAL FUNCTIONS (VSP2562)

TERMINAL		TYPE[1]	DESCRIPTION
NAME	PIN		
NC	1	—	No connection
NC	2	—	No connection
B0	3	DO	Data out bit 0 (LSB)
B1	4	DO	Data out bit 1
B2	5	DO	Data out bit 2
B3	6	DO	Data out bit 3
B4	7	DO	Data out bit 4
B5	8	DO	Data out bit 5
B6	9	DO	Data out bit 6
B7	10	DO	Data out bit 7
B8	11	DO	Data out bit 8
B9	12	DO	Data out bit 9
B10	13	DO	Data out bit 10
B11	14	DO	Data out bit 11 (MSB)
VDD	15	P	Digital power supply for data output
DGND	16	P	Digital ground for data output
ADCCK	17	DI	Clock for digital output buffer
VCC	18	P	Analog power supply
CLPDM	19	DI	CLPDM signal
CLPOB	20	DI	CLPOB signal

(1) Designators in TYPE: P = power supply and ground; DI = digital input; DO = digital output; AI = analog input; and AO = analog output.

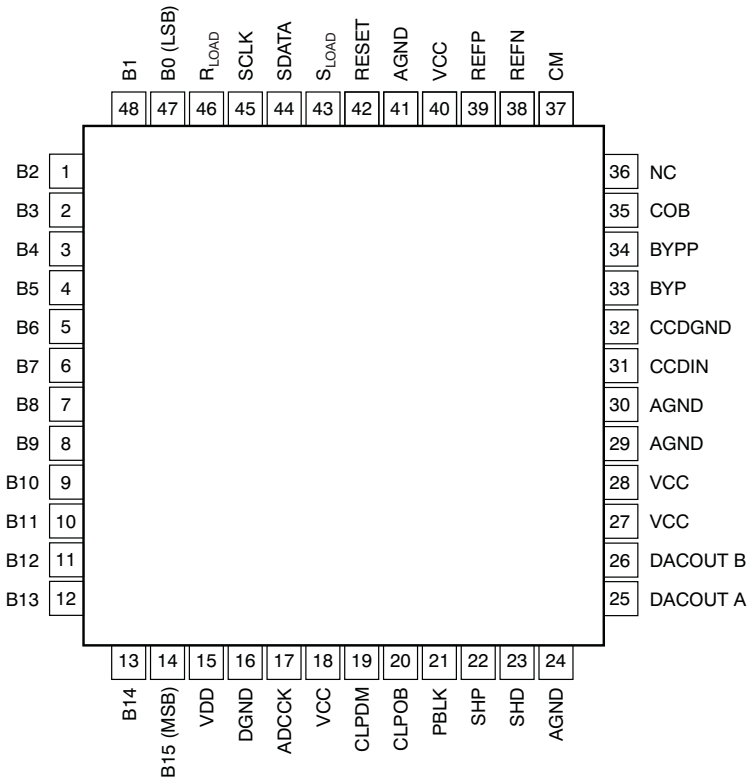
PRODUCT PREVIEW

TERMINAL FUNCTIONS (VSP2562) (continued)

TERMINAL		TYPE[1]	DESCRIPTION
NAME	PIN		
PBLK	21	DI	PBLK signal
SHP	22	DI	Sampling clock for reference level of CCD signal
SHD	23	DI	Sampling clock for data level of CCD signal
AGND	24	P	Analog ground
DACOUT A	25	AO	General-purpose 8-bit DAC output A
DACOUT B	26	AO	General-purpose 8-bit DAC output B
VCC	27	P	Analog power supply
VCC	28	P	Analog power supply
AGND	29	P	Analog ground
AGND	30	P	Analog ground
CCDIN	31	AI	CCD signal input
CCDGND	32	AI	CCD signal input ground
BYP	33	AO	Internal reference bypass to ground (0.1 μF)
BYPP	34	AO	Internal reference bypass to ground by (1000 pF)
COB	35	AO	OB loop feedback capacitor
NC	36	—	Non connection
CM	37	AO	Internal reference bypass to ground (0.1 μF)
REFN	38	AO	Internal reference bypass to ground (0.1 μF)
REFP	39	AO	Internal reference bypass to ground (0.1 μF)
VCC	40	P	Analog power supply
AGND	41	P	Analog ground
RESET	42	DI	System reset
S_{LOAD}	43	DI	Serial data latch signal
SDATA	44	DI	Serial data input
SCLK	45	DI	Serial data clock
R_{LOAD}	46	DI	Serial data update control signal
NC	47	—	No connection
NC	48	—	No connection

PRODUCT PREVIEW

VSP2566
PT PACKAGE (QFP-48)
(TOP VIEW)



TERMINAL FUNCTIONS (VSP2566)

TERMINAL		TYPE[1]	DESCRIPTION
NAME	PIN		
B2	1	DO	Data out bit 2
B3	2	DO	Data out bit 3
B4	3	DO	Data out bit 4
B5	4	DO	Data out bit 5
B6	5	DO	Data out bit 6
B7	6	DO	Data out bit 7
B8	7	DO	Data out bit 8
B9	8	DO	Data out bit 9
B10	9	DO	Data out bit 10
B11	10	DO	Data out bit 11
B12	11	DO	Data out bit 12
B13	12	DO	Data out bit 13
B14	13	DO	Data out bit 14
B15	14	DO	Data out bit 15(MSB)
VDD	15	P	Digital power supply for data output
DGND	16	P	Digital ground for data output
ADCCK	17	DI	Clock for digital output buffer
VCC	18	P	Analog power supply
CLPDM	19	DI	CLPDM signal
CLPOB	20	DI	CLPOB signal

(1) Designators in TYPE: P = power supply and ground; DI = digital input; DO = digital output; AI = analog input; and AO = analog output.

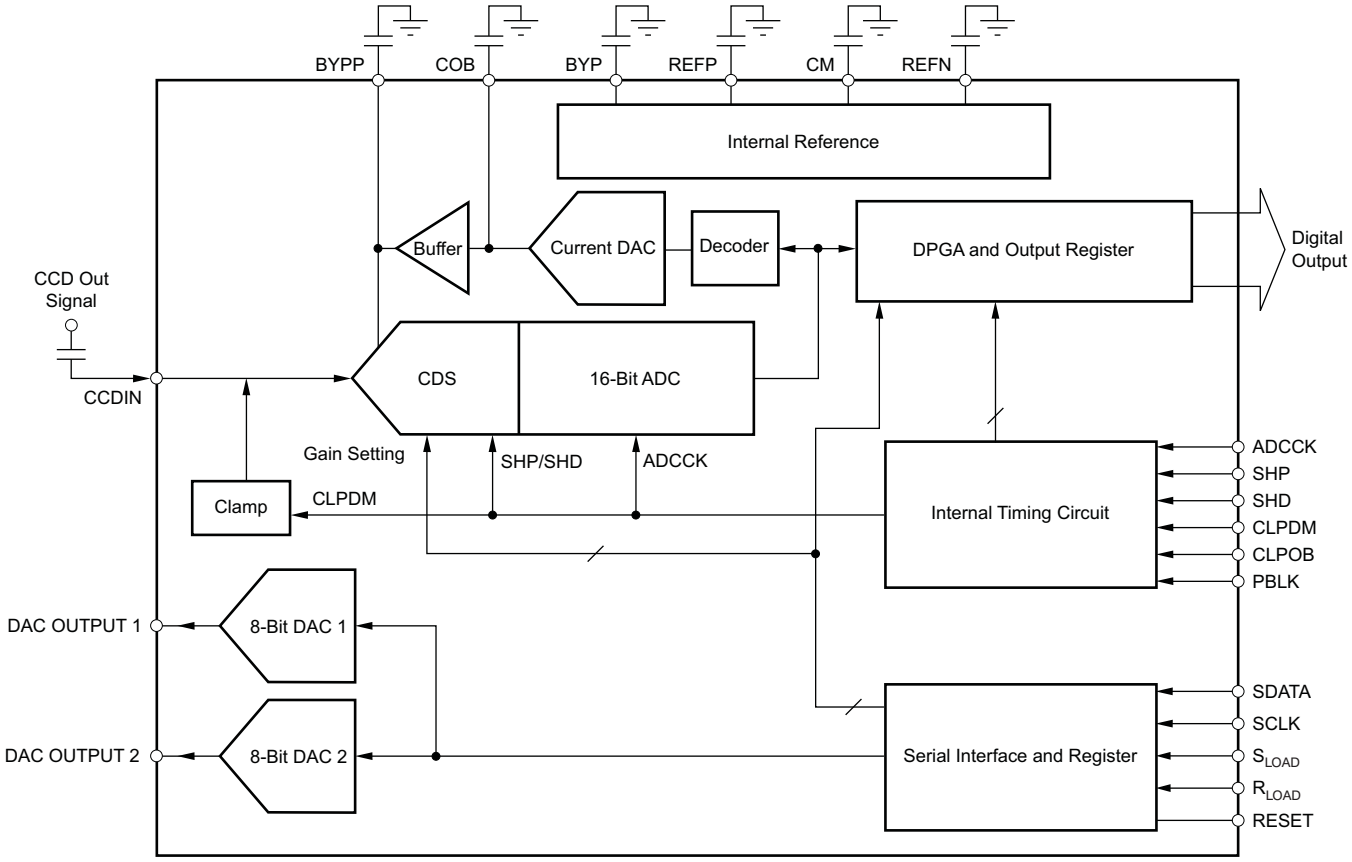
PRODUCT PREVIEW

TERMINAL FUNCTIONS (VSP2566) (continued)

TERMINAL		TYPE[1]	DESCRIPTION
NAME	PIN		
PBLK	21	DI	PBLK signal
SHP	22	DI	Sampling clock for reference level of CCD signal
SHD	23	DI	Sampling clock for data level of CCD signal
AGND	24	P	Analog ground
DACOUT 1	25	AO	General-purpose 8-bit DAC (1) output
DACOUT 2	26	AO	General-purpose 8-bit DAC (2) output
VCC	27	P	Analog power supply
VCC	28	P	Analog power supply
AGND	29	P	Analog ground
AGND	30	P	Analog ground
CCDIN	31	AI	CCD signal input
CCDGND	32	AI	CCD signal input ground
BYP	33	AO	Internal reference bypass to ground (0.1 μF)
BYPP	34	AO	Internal reference bypass to ground by (1000 pF)
COB	35	AO	OB loop feedback capacitor
NC	36	—	Non connection
CM	37	AO	Internal reference bypass to ground (0.1 μF)
REFN	38	AO	Internal reference bypass to ground (0.1 μF)
REFP	39	AO	Internal reference bypass to ground (0.1 μF)
VCC	40	P	Analog power supply
AGND	41	P	Analog ground
RESET	42	DI	System reset
S_{LOAD}	43	DI	Serial data latch signal
SDATA	44	DI	Serial data input
SCLK	45	DI	Serial data clock
R_{LOAD}	46	DI	Serial data update control signal
B0	47	DO	Data out bit 0 (LSB)
B1	48	DO	Data out bit 1

PRODUCT PREVIEW

FUNCTIONAL BLOCK DIAGRAM



PRODUCT PREVIEW

SYSTEM DESCRIPTION

OVERVIEW

The VSP2560/62/66 are a family of complete mixed-signal ICs that contain all of the key features associated with the processing of the charge-coupled device (CCD) imager output signal in a video camera, digital still camera, security camera, or other similar applications. Figure 3 shows a simplified block diagram of the VSP2560/62/66. The VSP2560/62/66 include a correlated double sampler (CDS), a programmable gain amplifier (PGA), an analog-to-digital converter (ADC), an input clamp, an optical black (OB) level clamp loop, a serial interface, timing control, and a reference voltage generator. It is recommend that an off-chip emitter follower be placed between the CCD output and the VSP2560/62/66 CCDIN input. All of the functions and parameters (such as PGA gain control, operation mode, and other settings) can be changed through the serial interface. All parameters are reset to the default value when the RESET pin goes to low asynchronously from the clocks.

The VSP2560/62/66 also provide a two-channel, general-purpose, 8-bit digital-to-analog converter (DAC). This DAC can be applied to various applications, such as CCD bias control, iris control, and so forth.

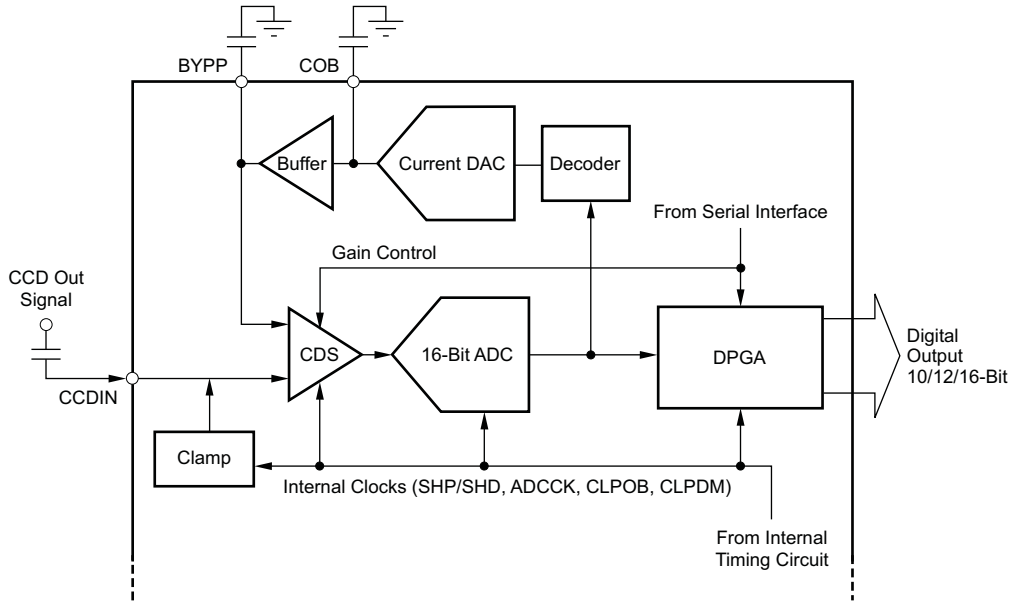


Figure 3. Simplified Block Diagram

CORRELATED DOUBLE SAMPLER (CDS)

The output signal of a CCD image sensor is sampled twice during one pixel period: once at the reference interval, and again at the data interval. Subtracting these two samples extracts the pixel video information and removes any noise that is common (or correlated) to both intervals. Thus, it is very important to reduce the reset noise and low-frequency noises that are present on the CCD output signal through the CDS. Figure 4 shows a block diagram of the CDS.

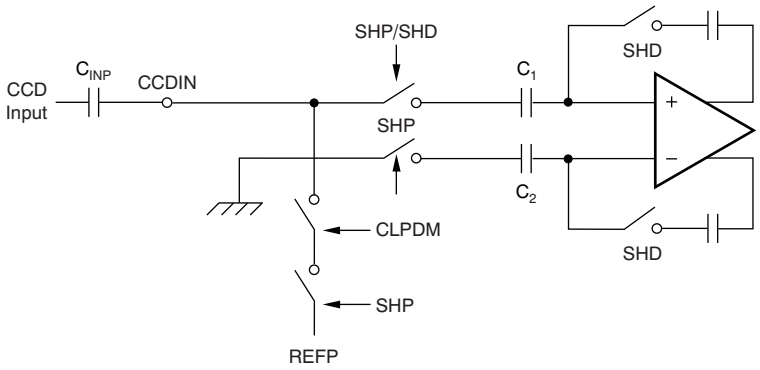


Figure 4. CDS and Input Clamp Block Diagram

INPUT CLAMP

The buffered CCD output is capacitively coupled to the VSP2560/62/66. The purpose of the input clamp is to restore the dc component of the input signal that was lost with the ac coupling, and establish the desired dc bias point for the CDS. The block diagram of Figure 4 also shows the input clamp. The input level is clamped to the internal reference voltage, REFP (1.5 V), during the dummy pixel interval. More specifically, the clamping function becomes active when both CLPDM and SHP are active.

Immediately after device power-on, the input capacitor clamp voltage is not charged. For fast charge-up of the clamp voltage, the VSP2560/62/66 provide a boost-up circuit.

16-BIT ADC

The VSP2560/62/66 include a high-speed, 16-bit ADC. This ADC uses a fully-differential pipelined architecture with correction. This architecture, incorporating ADC correction, is very advantageous for realizing better linearity for a smaller signal level as a result of the large linearity errors that tend to occur at specific points in the full-scale range; linearity also improves for a signal level below that specific point. The ADC ensures 16-bit resolution across the entire full-scale range.

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OPTICAL BLACK LEVEL (OB) LOOP AND OB CLAMP LEVEL

The VSP2560/62/66 have a built-in optical black (OB) offset self-calibration circuit (OB loop) that compensates the OB level by using OB pixels output from the CCD image sensor. A block diagram of the OB loop and OB clamp circuit is shown in Figure 5. CCD offset is compensated by converging this calibration circuit while activating the CLPOB pin during a period when the OB pixels are output from the CCD.

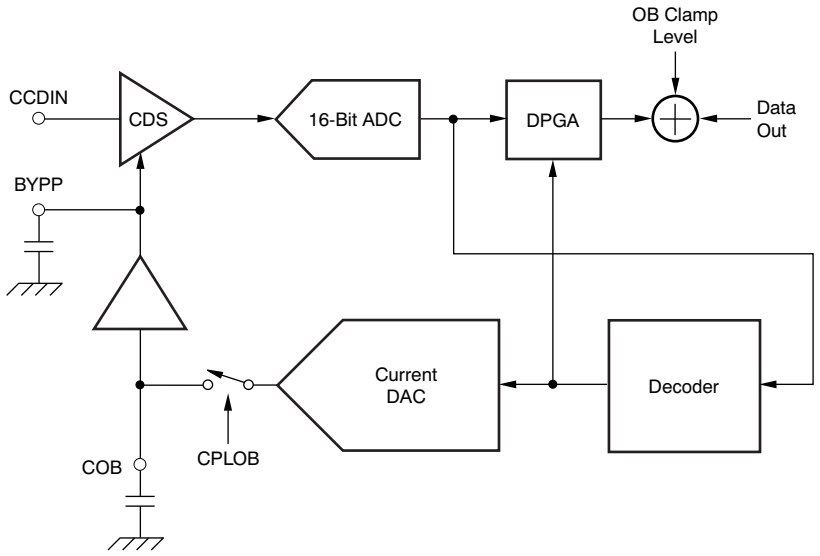

Figure 5. OB Loop and OB Level Clamp

At the CDS circuit, the CCD offset is compensated as a difference between the reference level and the OB pixel data level. These compensated signal levels are recognized as actual *OB levels*, and the outputs are clamped to the OB levels set by the serial interface. These OB levels are the base of black for the effective pixel period thereafter. Because DPGA, which is a gain stage, is outside the OB loop, the OB levels are not affected even when the gain is changed.

The converging time of the OB loop is determined based on the capacitor value connected to the COB terminal and output from the current output DAC (IDAC) of the loop. The time constant can be obtained from Equation 1:

$$T = \frac{C}{16384 \times I_{MIN}} \quad (1)$$

Where:

- C is the capacitor value connected to COB
- I_{MIN} is the minimum current (0.15 µA) of the IDAC, which is the current equivalent to 1 LSB of the IDAC output.

When C = 0.1 µF, T is 40.7 µs. Slew rate (SR) can be obtained from Equation 2:

$$SR = \frac{I_{MAX}}{C} \quad (2)$$

Where:

- C is the capacitor value connected to COB
- I_{MAX} is the maximum current (153 µA) of the IDAC, which is the current equivalent to 1023 LSB of the IDAC output.

IDAC output current multiplication is provided by the VSP2560/62/66. This function increases the IDAC output current through the serial interface in multiples of 2, 4, and 8. Increased IDAC current shortens the time constant of the OB loop. In this case, the OB level is drastically changed and must quickly settle the OB loop; this function is effective.

Immediately after power-on, the COB capacitor voltage is not charged. For fast start up, a COB voltage boost-up circuit is provided.

The OB clamp level (digital output value) can be externally set through the serial interface by inputting the digital code to the OB clamp level register. The digital codes to be input and the corresponding OB clamp levels are shown in Table 1.

Table 1. Input Codes and OB Clamp Levels to be Set

CODE	CLAMP LEVEL		
	VSP2560 (10-Bit)	VSP2562 (12-Bit)	VSP2566 (16-Bit)
00000b	16 LSB	64 LSB	1024 LSB
00001b	18 LSB	72 LSB	1152 LSB
—	—	—	—
00110b	28 LSB	112 LSB	1792 LSB
00111b	30 LSB	120 LSB	1920 LSB
01000b (default)	32 LSB	128 LSB	2048 LSB
01001b	34 LSB	136 LSB	2176 LSB
—	—	—	—
11110b	76 LSB	304 LSB	4864 LSB
11111b	78 LSB	312 LSB	4992 LSB

PROGRAMMABLE GAIN

The VSP2560/62/66 have gains that range from –9 dB to 44 dB. The desired gain is set as a combination of CDS gain and the digital programmable gain amplifier (DPGA). The CDS gain can be programmed from 0 dB to 18 dB in 6-dB steps, and has a –3-dB gain for the large input signal (such as over 1 V). Digital gain can be programmed from –6 dB to 26 dB in 0.032-dB steps. Both gain controls are managed through the serial interface. The digital gain changes linearly in proportion to the settling code. Figure 6 shows the relationship of input code to digital gain.

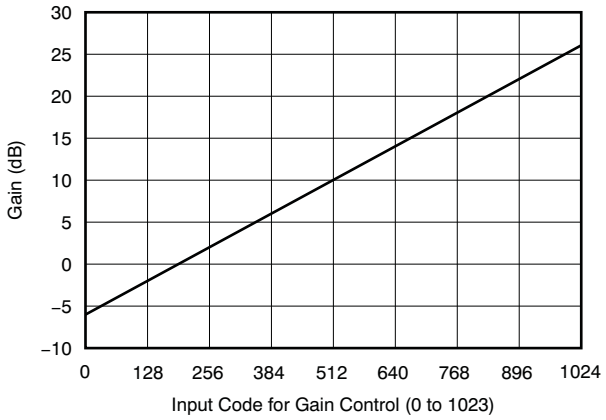

Figure 6. Settling Code versus Digital Gain

The recommended usage of the combination of CDS and digital gain is to adjust the CDS gain first, primarily as an image signal amplification; afterwards, use the digital gain as an adaptive gain control. The wide range of digital gain covers the necessary gain range on most typical applications. If the CDS gain must be changed, however, it is recommended to change it during a period that does not affect picture quality (such as a blanking period).

PRE-BLANKING AND DATA LATENCY

The VSP2560/62/66 have a pre-blanking function. When PBLK is low, the digital outputs all become '0' at the eighth rising edge of ADCCK after PBLK goes low, to accommodate the clock latency of the VSP2560/62/66. The data latency of this family of devices is six clock cycles. The digital output data are transmitted at the rising edge of ADCCK with a delay of six clock cycles.

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STANDBY MODE AND POWER TRIM FUNCTION

For the purpose of saving power, the VSP2560/62/66 devices can be put into a standby mode through the serial interface control when the device is not in use. In this mode, all the functional blocks are disabled and the digital outputs are set to '0'. The consumption current drops to approximately 2 mA. Only 10 ms is required to restore the device from standby mode. A general-purpose DAC also enables standby mode independently, which allows the device to enter standby mode and resume normal operation through the serial interface.

The VSP2560/62/66 provide a power trim function. This function trims the power of the CDS, ADC, reference source, and gain boost amplifier of the ADC (GBA). Power consumption can be reduced through this trim function, though it is not recommended at 36-MHz operation because accuracy may degrade. This function is useful for low sampling rate operation.

TIMINGS

The CDS and ADC are operated by SHP and SHD, and the derivative timing clocks are generated by the on-chip timing generator. The output register and decoder are operated by ADCCK. The digital output data are synchronized with ADCCK. The timing relationship between the CCD signal, SHP, SHD, ADCCK, and the output data is described in the *Timing Characteristics* section. CLPOB is used to activate the black level clamp loop during the OB pixel interval and CLPDM is used to activate the input clamping during the dummy pixel interval. In standby mode ADCCK, SHP, SHD, CLPOB, and CLPDM are internally masked and pulled high.

The data output timing can be delayed by the AFE-Ctrl(2) register. Fundamentally, the data output timing should be adjusted through ADCCK timing, although that is effective when exceeding adjust range is needed.

As explained in the *Input Clamp* and *Optical Black Level (OB) Loop and OB Clamp Level* sections, CLPOB is used for controlling the OB loop that compensates CCD offset automatically, and CLPDM is used for charging the input clamp voltage to the capacitor C_{IN} that is connected to CCDIN. To obtain proper operation, both CLPOB and CLPDM should be active immediately before the timing begins, as described in the following paragraphs.

The CCD has several dummy and OB pixels. Typically, the dummy pixel is placed at the start of the line and the OB pixel is placed after the effective pixel. The timing recommendation is for CLPDM to activate during the dummy pixel period, and for CLPOB to activate during the OB pixel period. Any active period should include the dummy and OB pixels in the same period.

In some cases, the dummy pixel is defined as only '2' or some other small value. The VSP2560/62/66 may operate with a small defined dummy pixel value, but '2' is too small. For instance, if the discharge of the input clamp from C_{IN} is large, the VSP2560/62/66 could not recover from it. In this case, CLPDM can share the OB pixel with CLPOB. Although a longer CLPOB period is preferred, approximately 20 pixels are theoretically enough to return stable operation to normal conditions, depending on the situation (such as the noise of OB pixels). CLPDM also requires 10 to 20 pixels. In the event the OB pixel is only approximately 30 pixels, it should be shared as 20 pixels for CLPOB and 10 pixels for CLPDM. In order to get stable OB levels, CLPOB and CLPDM need to be active during different parts of the CCD pixels.

Figure 7 shows a timing diagram for CLPOB and CLPDM. The functionality of SHP, SHD, CLPOB, CLPDM, and R_{LOAD} is active at low periods or at the rising edge of the default setting of the serial interface; each active polarity can be selected by register settings.

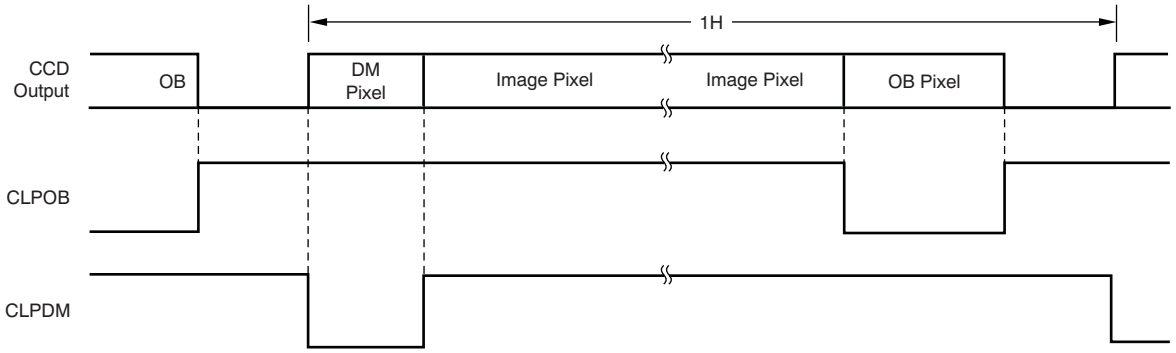

Figure 7. CLPOB and CLPDM Timing Diagram

VOLTAGE REFERENCE

All reference voltages and bias currents used in these devices are created from internal bandgap circuitry. The VSP2560/62/66 have symmetrical, independent voltage references for each channel.

Both channels of the CDS and the ADC use three primary reference voltages: REFP (1.5 V), REFN (1.0 V), and CM (1.25 V) of an individual reference. REFP and REFN are buffered on-chip. CM is derived as the mid-voltage of the resistor chain internally connecting REFP and REFN. The ADC full-scale range is determined by twice the difference voltage between REFP and REFN. REFP, REFN, and CM should be heavily decoupled with appropriate capacitors.

HOT PIXEL REJECTION

Sometimes the OB pixel output signal from the CCD includes an unusual level signal that is caused by pixel defection. If this level reaches a full-scale level, it may affect OB level stability. The VSP2560/62/66 has a function that rejects any unusually large pixel level (hot pixels) in the OB pixel. This function may contribute to CCD yield improvement, caused by OB pixel failure.

Rejection levels for hot pixels are programmed through the serial interface. When a hot pixel comes from the CCD, the VSP2560/62/66 omit it and replaces the previous pixel level for OB level calculation.

GENERAL-PURPOSE, 8-BIT DAC (DAC1, DAC2)

The VSP2560/62/66 incorporate two identical 8-bit DACs. These DACs are for user-definable options such as iris control and sub-bias voltage control of the CCD imager. The input data for these DACs are set by the written data through the serial interface (refer to the *Serial Interface* section for more detail). DAC input data that are all '0's correspond to a minimum output voltage of 0.1 V. In a similar manner, all '1's correspond to a maximum output voltage of 2.9 V. For minimizing power consumption, DAC standby is recommend when the application does not use a DAC.

SERIAL INTERFACE

All functionality and parameters of the VSP2560/62/66 are controlled through the serial interface. The serial interface of the VSP2560/62/66 is composed of three signals: SDATA, SCLK, and S_{LOAD}. SDATA data are sequentially stored in the shift register at the rising edge of SCLK, and shift register data are stored in the parallel latch of the rising edge of S_{LOAD}. Before a writing operation, S_{LOAD} must go low, and remain low during writing (refer to the Serial Interface Timing description of the Timing Characteristics).

The serial interface command is composed of a 10-bit address and 6-bit data. Fundamentally, the writing operation is a two-byte write mode. In this mode, one serial interface command is sent by a combination of address and data. The 10-bits address should be sent primarily as LSB first, and followed 6-bit data also sent as LSB first. The 6-bits command data is stored to respective register by 10-bits of address when rising edge of S_{LOAD}. The stored serial command data immediately affects the rising edge of S_{LOAD}.

The VSP2560/62/66 are also supported by a continuous writing mode. When the input serial data are longer than two bytes (16-bits), the following data stream is automatically recognized as the data of the next address. In this mode, 6-bit serial command data are stored in the respective register immediately when the data are fetched. Address and data should be sent as LSB-first as well as in a two-byte writing mode. If the data bits do not fill up six bits at the end of the data stream, any blank data bits are ignored.

Register updates can be controlled by R_{LOAD}. When D1 of the Clk-Pol-Ctrl register is set to '1', the register data update timing synchronizes the rising edge of R_{LOAD}. In this operation, serial interface data are stored in the buffer register until the next rising edge of R_{LOAD}, and are updated simultaneously by that rising edge. If the rising edge of R_{LOAD} occurs during continuous writing, any updated data are completed during the data streams before the rising edge of R_{LOAD}. The setting for the serial interface registers is described in the *Serial Interface Register Description* section.

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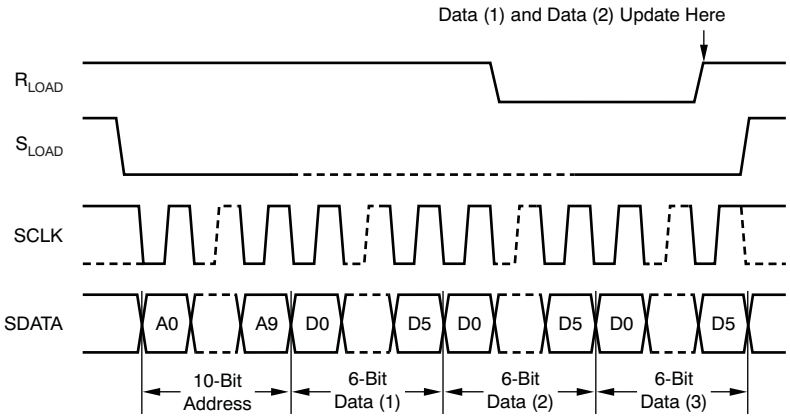

Figure 8. Continuous Writing Mode

SERIAL INTERFACE REGISTER DESCRIPTION

The serial interface command data format is shown in Table 2. Descriptions of each register are provided in the following sections.

Table 2. Serial Interface Data Format

	ADDRESS										DATA					
REGISTER	MSB A9	A8	A7	A6	A5	A4	A3	A2	A1	LSB A0	MSB D5	D4	D3	D2	D1	LSB D0
Clk-Pol-Ctrl	0	0	0	0	0	0	0	0	0	0	D5	D4	D3	D2	D1	0
AFE-Ctrl(1)	0	0	0	0	0	0	0	0	0	1	0	D4	D3	D2	D1	D0
AFE-Ctrl(2)	0	0	0	0	0	0	0	0	1	0	D5	0	0	D2	D1	D0
S-Delay	0	0	0	0	0	0	0	0	1	1	0	0	0	D2	D1	D0
Clamp	0	0	0	0	0	0	0	1	0	0	D5	D4	D3	D2	D1	D0
Hot-Pixel	0	0	0	0	0	0	0	1	0	1	D5	D4	D3	D2	D1	D0
D-PGA_L	0	0	0	0	0	0	0	1	1	0	D5	D4	D3	D2	D1	D0
D-PGA_U	0	0	0	0	0	0	0	1	1	1	0	D4	D3	D2	D1	D0
A-PGA	0	0	0	0	0	0	1	0	0	0	0	0	D3	D2	D1	D0
Power	0	0	0	0	0	0	1	0	0	1	D5	D4	D3	D2	D1	D0
DAC A_L	0	0	0	0	0	0	1	0	1	0	D5	D4	D3	D2	D1	D0
DAC A_U	0	0	0	0	0	0	1	0	1	1	0	0	0	D2	D1	D0
DAC B_L	0	0	0	0	0	0	1	1	0	0	D5	D4	D3	D2	D1	D0
DAC B_U	0	0	0	0	0	0	1	1	0	1	0	0	0	D2	D1	D0
Reserved	This address is reserved										Do not use					

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Clk-Pol-Ctrl Register Description (Address = 000h)

The Clk-Pol-Ctrl register selects the active polarity of CLPDM, CLPOB, and SHP/SHD, as shown in Table 3.

Table 3. Active Polarity Selection

DATA BIT	NAME	DESCRIPTION		DEFAULT
D1	Register update control	0 = Real-time update	1 = Update by R_{LOAD}	0
D2	R_{LOAD} polarity	0 = Update at rising edge of R_{LOAD}	1 = Update at falling edge of R_{LOAD} (1)	0
D3	CLPDM polarity	0 = Active low	1 = Active high	0
D4	CLPOB polarity	0 = Active low	1 = Active high	0
D5	SHP/SHD polarity	0 = Active low	1 = Active high	0

(1) When data bit D2 is set as '1', the register update timing is controlled by R_{LOAD} regardless if D1 is set as '0' or '1'.

AFE-Ctrl(1) Register Description (Address = 001h)

The AFE-Ctrl(1) register controls the standby settings, as shown in Table 4.

Table 4. Standby Setting

DATA BIT	NAME	DESCRIPTION		DEFAULT
D0	Standby	0 = Normal operation	1 = Standby	0
D1	DAC1 standby	0 = Operating	1 = Standby	1
D2	DAC2 standby	0 = Operating	1 = Standby	1
D3	Test enable	0 = Disabled	1 = Enabled	0

AFE-Ctrl(2) Register Description (Address = 002h)

The AFE-Ctrl(2) register controls the data output setting, as shown in Table 5.

Table 5. Data Output Setting

DATA BIT	NAME	DESCRIPTION		DEFAULT
D[1:0]	Data output delay	00 = 0 ns 01= 2 ns 10 = 4 ns 11 = 6 ns		00
D4	Output enabled	0 = Enabled	1 = Hi-Z	0

S-Delay Register Description (Address = 003h)

The S-delay register controls the SHD sampling start time from the rising edge of SHP. SHD sampling is shown in Table 6.

Table 6. SHD Sampling

DATA BIT	NAME	DESCRIPTION	DEFAULT
D[1:0]	Sampling delay for SHD	00 = 0 ns 01= 2 ns 10 = Do not use 11 = Do not use	00

PRODUCT PREVIEW

Clamp Register Description (Address = 004h)

The clamp levels for the VSP2560/62/66 are shown in Table 7.

Table 7. Clamp Levels

D4	D3	D2	D1	D0	CLAMP LEVEL (VSP2560)	CLAMP LEVEL (VSP2562)	CLAMP LEVEL (VSP2566)
0	0	0	0	0	16 (LSB)	64 (LSB)	1024 (LSB)
0	0	0	0	1	18 (LSB)	72 (LSB)	1152 (LSB)
—					—	—	—
0	0	1	1	1	30 (LSB)	120 (LSB)	1920 (LSB)
0	1	0	0	0	32 (LSB) (default)	128 (LSB) (default)	2048 (LSB) (default)
0	1	0	0	1	34 (LSB)	136 (LSB)	2176 (LSB)
—					—	—	—
1	1	1	1	0	76 (LSB)	304 (LSB)	4864 (LSB)
1	1	1	1	1	78 (LSB)	312 (LSB)	4992 (LSB)

Hot-Pixel Register Description (Address = 005h)

The hot-pixel register defines the threshold level for input signals from the saturated pixel (as shown in Table 8), which is mainly caused by a defective pixel during the OB term.

Table 8. Saturated Pixel Threshold Level

DATA BIT	NAME	DESCRIPTION		DEFAULT
D[4:0]	Hot pixel rejection level	The hot pixel rejection level is given as: For the VSP2560 (10-bit), R_L (LSB) = 16 × (d[4:0] + 1) For the VSP2562 (12-bit), R_L (LSB) = 64 × (d[4:0] + 1) For the VSP2566 (16-bit), R_L (LSB) = 1024 × (d[4:0] + 1) Where R_L is the difference in level from the OB level.		11111
D5	Hot pixel rejection disable	0 = Disabled	1 = Enabled	1

D-PGA Register Description (Address = 006h and 007h)

The D-PGA register defines the digital PGA gain, as shown in Table 9.

Table 9. DPGA Gain

D-PGA_U	D-PGA_L	ANALOG GAIN	DEFAULT
D[3:0]	D[5:0]	Digital PGA gain is given as: Gain (dB) = (D-PGA × 0.03125) – 6 Where D-PGA is the decimal value of 10-bit data that are combined D-PGA = 0 (decimal) = –6 dB D-PGA = 192 (decimal) = 0 (default) D-PGA = 1023 (decimal) = 26 dB	D-PGA = 00 1100 0000b = 0 dB

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A-PGA Register Description (Address = 008h)

The A-PGA register describes the CDS gain control, as shown in Table 10.

Table 10. CDS Gain Control

D2	D1	D0	ANALOG GAIN (dB)
0	0	0	0 (default)
0	0	1	6
0	1	0	12
0	1	1	18
1	1	1	–3

Power Register Description (Address = 009h)

The power register describes the power control settings, as shown in Table 11.

Table 11. Power Controls

DATA BIT	NAME	DESCRIPTION		DEFAULT
D[1:0]	OB loop IDAC output current	00 = x1, 01 = x2, 10 = x4, 11 = x8 DAC power control for OB loop time constant		00
D2	CDS power trim	0 = Normal CDS power	1 = Reduce CDS power	0
		CDS power control for settling time		
D3	ADC power trim	0 = Normal ADC power	1 = Reduce ADC power	0
		ADC power control		
D4	Ref power trim	0 = Normal Ref power	1 = Reduce Ref power	0
		REF bias power control		
D5	GBA power trim	0 = Normal GBA power	1 = Reduce GBA power	0
		CDS gain power control		

DAC A Register Description (Address = 00Ah and 00Bh)

The DAC B register describes the codes for DAC1, as shown in Table 12.

Table 12. DAC1

DAC1_U	DAC1_L	ANALOG GAIN	DEFAULT
D[1:0]	D[5:0]	General-purpose, 8-bit DAC1 input code. DAC1_U is the MSB side code.	00 000000

DAC B Register Description (Address = 00Ch and 00Dh)

The DAC B register describes the codes for DAC2, as shown in Table 13.

Table 13. DAC2

DAC2_U	DAC2_L	ANALOG GAIN	DEFAULT
D[1:0]	D[5:0]	General-purpose, 8-bit DAC2 input code. DAC1_U is MSB side code.	00 000000

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POWER SUPPLY, GROUNDING, AND DEVICE COUPLING RECOMMENDATIONS

The VSP2560/62/66 incorporate a high-precision, high-speed ADC and analog circuitry that are vulnerable to any extraneous noise from the rails or elsewhere. For this reason, the VSP2560/62/66 should be treated as an analog component. Furthermore, though these devices have several supply pins, all supply pins except for VDD should be powered by only the analog supply of the system. This design ensures the most consistent results because digital power lines often carry high levels of wideband noise that would otherwise be coupled into the device and degrade the achievable performance.

Proper grounding, short lead length, and the use of ground planes are also very important for high-frequency designs. Multilayer printed circuit boards (PCBs) are recommended to deliver the best performance because they offer distinct advantages such as minimizing ground impedance, separation of signal layers by ground layers, etc. It is highly recommended that the analog and digital ground pins of the VSP2560/62/66 be joined together at the IC and be connected only to the analog ground of the system. The driver stage of the digital outputs (B15, B11, and B[9:0]) is supplied through a dedicated supply pin (VDD) and should be separated from the other supply pins completely, or at least with a ferrite bead. It is also recommended to keep the capacitive loading on the output data lines as low as possible (typically less than 15 pF). Larger capacitive loads demand higher charging current as a result of surges that can feed back into the analog portion of the VSP2560/62/66 and affect performance.

If possible, external buffers or latches should be used. This configuration provides the added benefit of isolating the VSP2560/62/66 from any digital noise activities on the data lines. In addition, resistors in series with each data line may help in minimizing the surge current.

Because of the high operation speed, the converter also generates high-frequency current transients and noises that are fed back into the supply and reference lines. This condition requires the supply and reference pins to be sufficiently bypassed. In most cases, a 0.1-μF ceramic-chip capacitor is adequate to decouple the reference pins. Supply pins should be decoupled to the ground plane with a parallel combination of tantalum (1 μF to 22 μF) and ceramic (0.1 μF) capacitors. The effectiveness of the decoupling largely depends on the proximity to the individual pin. VDD should be decoupled to the proximity of DGND. Special attention must be paid to the bypassing of COB and BYPP because these capacitor values determine important analog performance of the device. Although the recommended value for COB is 0.1 μF and BYPP is 1000 pF, it is better to adjust the capacitor for BYPP in the case.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
VSP2560PTR	ACTIVE	LQFP	PT	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VSP2560	Samples
VSP2560PTRG4	ACTIVE	LQFP	PT	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VSP2560	Samples
VSP2562PT	ACTIVE	LQFP	PT	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	VSP2562	Samples
VSP2562PTG4	ACTIVE	LQFP	PT	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	VSP2562	Samples
VSP2566PT	ACTIVE	LQFP	PT	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	VSP2566	Samples
VSP2566PTG4	ACTIVE	LQFP	PT	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	VSP2566	Samples
VSP2566PTR	OBSOLETE	LQFP	PT	48		TBD	Call TI	Call TI	-25 to 85	VSP2566	
VSP2566PTRG4	OBSOLETE	LQFP	PT	48		TBD	Call TI	Call TI	-25 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

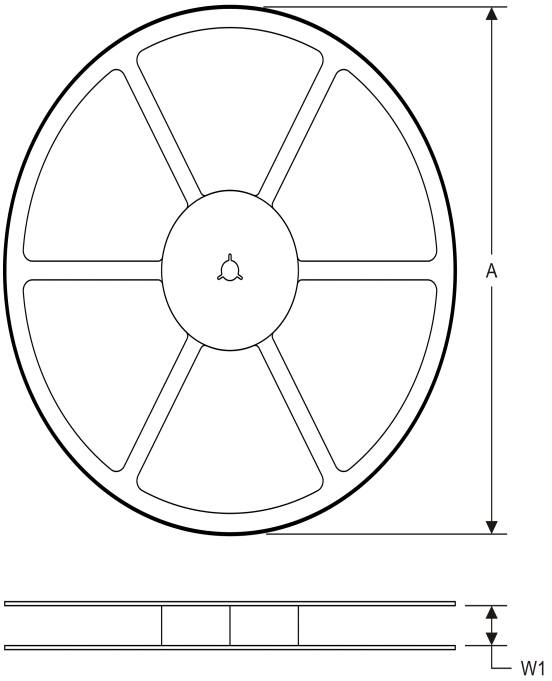
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

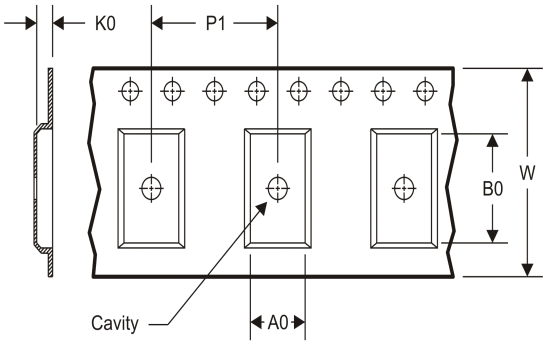
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



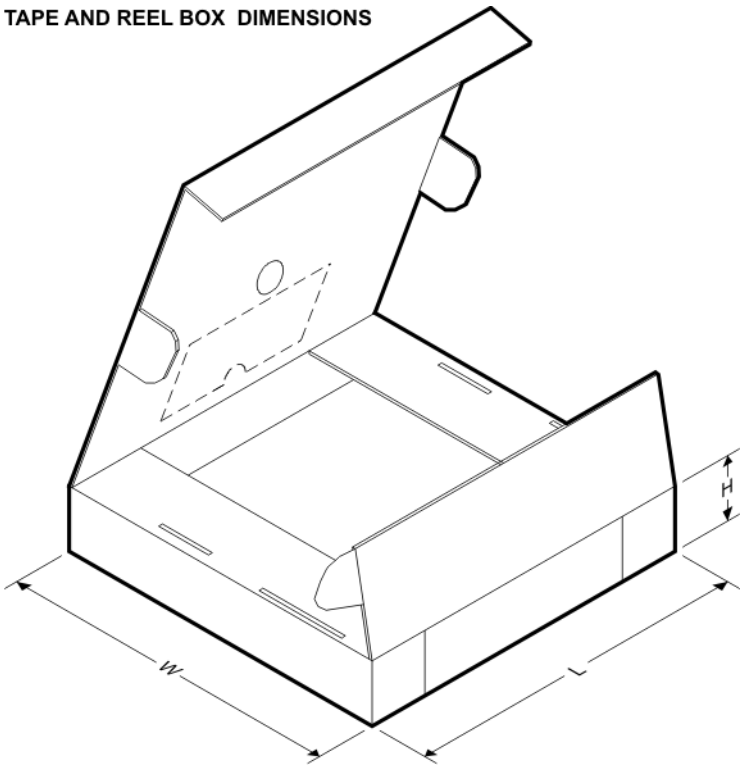
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
VSP2560PTR	LQFP	PT	48	1000	330.0	17.4	9.5	9.5	2.0	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
VSP2560PTR	LQFP	PT	48	1000	333.2	345.9	28.6

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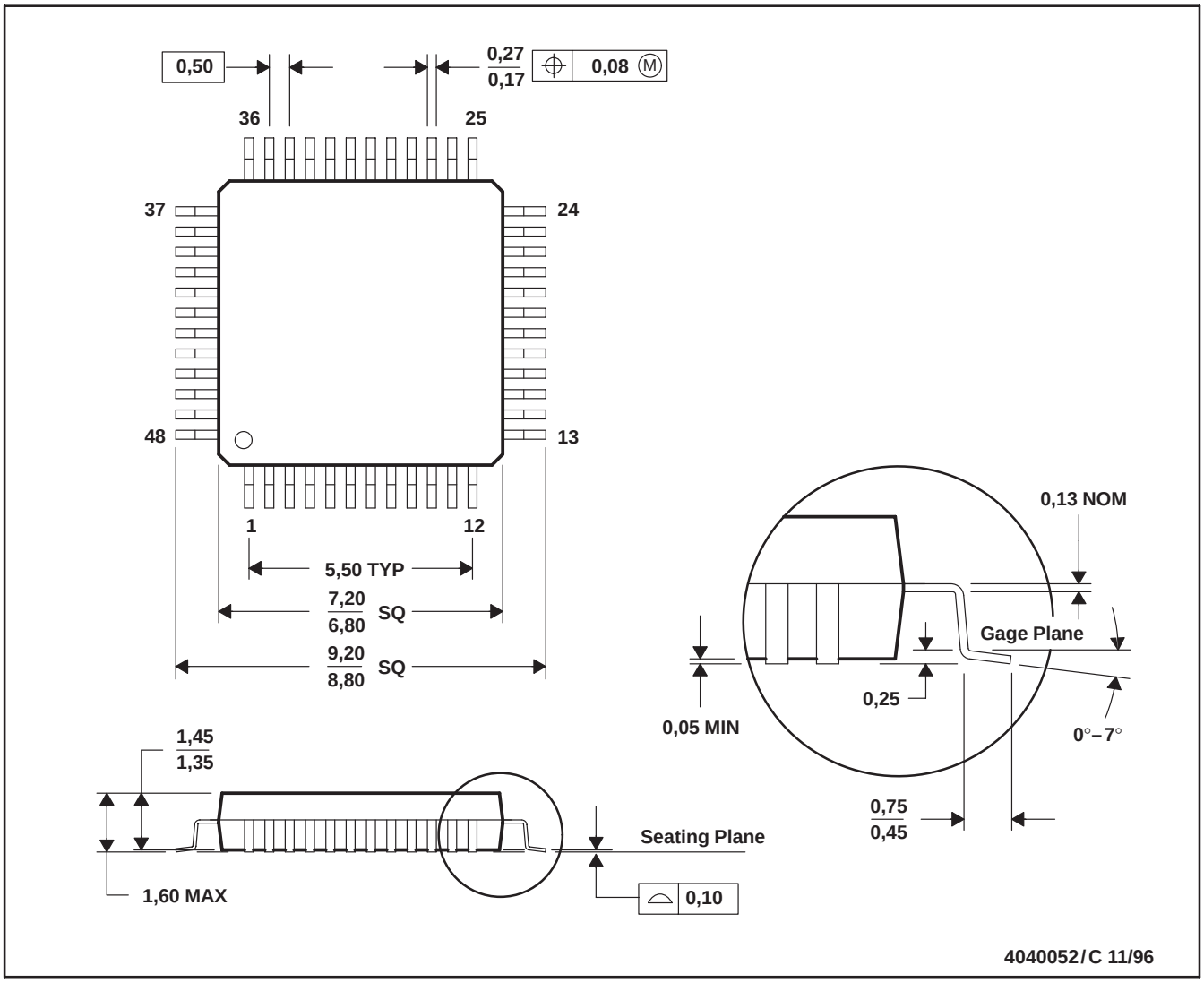
PT (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. This may also be a thermally enhanced plastic package with leads conected to the die pads.

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