# CCD Analog Front-End with Timing Generator for Digital Cameras

**Check for Samples: VSP8133**

## FEATURES

- **CCD Signal Processing:**
  - **Correlated Double Sampling (CDS)**
  - **16-Bit Analog-to-Digital Conversion:**
    - **Conversion Rate: 50 MHz**
    - **No Missing Codes Ensured**
- **Input-Referred SNR: 80 dB at 12-dB Gain**
- **Programmable and Fast Black-Level Clamping**
- **Programmable Gain Amplifier (PGA): 0 dB to +51.15 dB**
  - **Analog Gain: 0 dB to +18 dB**
  - **Digital Gain: 0 dB to + 33.15 dB**
  - **Additional CDS Gain: +3.5 dB**
- **Timing Generator:**
  - **Fully Programmable $V_{RATE}$ Timing with Serial I/O**
  - **Default Timing Supports Standard Operation**
  - **Flexible $V_{RATE}$ Pin Assignment**
  - **HD and VD Master or Slave Mode**
  - **Flexible Draft or Pixel Summing Operation**
  - **Supported Timing Range: 32767 Pixels × 8191 Lines**
  - **Frame Memory Depth: 32**
- **RG and $H_{DRIVER}$:**
  - **Programmable Drivability Control**
  - **Two-Phase $H_{MODE}$**
  - **Reset Gate Driver and HL Driver**
- **CCD Horizontal High-Speed Clock Phase Control:**
  - **Fine Step: 0.2 ns for 50 MHz**
  - **DLL Range (H1, H2, HL, RG, MCKOUT, SHP, SHD): Full Range of MCLK in 1/100th Steps**
- **Vertical CCD Driver:**
  - **16-Channel $V_{DRIVER}$ with Sub-Driver**
  - **Supports Motion and Still CCD Driving**
    - **Three Level Drivers ($V_{TRANSFER}$) × 10**
    - **Two Level Drivers ($V_{TRANSFER}$) × 2**
    - **Two Level Small Drivers ($V_{TRANSFER}$) × 4**
    - **Three Level Sub-Drivers ($E_{SHUTTER}$) × 1**
    - **6100 pF with 30 Ω (Except two level small drivers)**
- **Flexible Voltage Operation:**
  - **AVDD30: 2.7 V to 3.6 V**
  - **IOVDD30: 1.8 V to 3.0 V**
  - **RGVDD30: 2.7 V to 3.6 V**
  - **HVDD30: 2.7 V to 3.6 V**
  - **VL: –5.0 V to –8.0 V**
  - **VM: GND**
  - **VH: 11 V to 15 V**
- **Low Power Dissipation:**
  - **Operation: 100 mW at 2.7 V (40 MHz)**
  - **Standby Mode 1: 8 mW**
  - **Standby Mode 2: 2 mW**
- **QFN-64 Package**

## DESCRIPTION

The VSP8133 is a complete, mixed-signal device for charge-coupled device (CCD) signal processing with a built-in CCD timing generator and an analog-to-digital converter (ADC). The analog front-end (AFE) CCD channel has correlated double sampling to extract image information from the CCD output signal. Signal paths have gains ranging from 0 dB to +51.15 dB. The black-level clamping circuit enables accurate black reference level and rapid black-level recovery after gain changes. An input signal clamp is also available. The system synchronizes the master clock, horizontal driver (HD), and vertical driver (VD). The VSP8133 supports all signal terminals that the CCD requires. The RG driver and $H_{DRIVER}$ synchronize the ADC clock phase in order to achieve ideal performance.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION(1)

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR | SPECIFIED TEMPERATURE RANGE |
|---|---|---|---|
| VSP8133 | QFN-64 | RSK | 0°C to +85°C |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

## RELATED DOCUMENTS

| PRODUCT | LITERATURE NUMBER |
|---|---|
| VSP8133 User Reference Manual | SLEU107 |

## ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

| PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| Supply voltage | AVDD30, IOVDD30, HVDD30, RGVDD30 | –0.3 to +4.0 | V |
| | VL | GND to –10 | V |
| | VH | VL + 26 | V |
| Ground voltage differences | AVSS, IOVSS30, HVSS30, HLVSS, RGVSS30 | ±0.1 | V |
| Digital input voltage | | –0.3 to (IOVDD30 + 0.3) | V |
| Analog input voltage | | –0.3 to (AVDD30 + 0.3) | V |
| Input current (all pins except supplies) | | ±10 | mA |
| Ambient temperature under bias | | –25 to +85 | °C |
| Storage temperature | | –55 to +125 | °C |
| Junction temperature | | +150 | °C |
| Package temperature (IR reflow, peak) | | +250 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range, unless otherwise noted.

| PARAMETER | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Analog supply voltage | AVDD30 | | 2.7 | 3.0 | 3.6 | V |
| Digital supply voltage | IOVDD30 | | 1.5 | | 3.6 | V |
| Driver supply voltage | HVDD30, HLVDD30 | | 2.7 | 3.0 | 3.6 | V |
| | RGVDD30 | | 2.7 | 3.0 | 3.6 | V |
| | VMSUB | IOVDD30 – 1.7 V ≤ VL + 10 V | VL | | IOVDD30 – 1.7 | V |
| | | IOVDD30 – 1.7 V > VL + 10 V | VL | | VL + 10 | V |
| | VL | | –9.0 | | –5.0 | V |
| | VH | | 11.5 | | 15.5 | V |
| | VM | | | GND | | V |
| Digital input logic family | | | | CMOS | | V |
| Digital input clock frequency | MCK | | 9 | | 50 | MHz |
| | SCLK | | | | 20 | MHz |
| Operating free-air temperature | $T_A$ | | 0 | | +85 | °C |

## THERMAL INFORMATION

| THERMAL METRIC(1) | | VSP8133 RSK (QFN) 64 PINS | UNITS |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 27.3 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 13.8 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 5.9 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.2 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 5.9 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | 1.5 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## ELECTRICAL CHARACTERISTICS

All specifications are at $T_A$ = +25°C, AVDD30 = IOVDD30 = 3.0 V, and conversion rate = 40 MHz, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **RESOLUTION** | | | | | | |
| | Output resolution | | | 12 | | Bits |
| **CONVERSION AND CLOCK RATE** | | | | | | |
| | Conversion and clock rate | | 9 | 40 | 50 | MHz |
| **ANALOG INPUT (CCDIN)** | | | | | | |
| | Input signal level for full-scale out | Gain = 0 dB | | 1000 | | mV |
| | Input capacitance | | | 6 | | pF |
| **TRANSFER CHARACTERISTICS** | | | | | | |
| DNL | Differential nonlinearity | Gain = 0 dB | | ±0.5 | | LSB |
| INL | Integral nonlinearity | Gain = 0 dB, full-scale input | | ±3 | | LSB |
| | | Gain = 0 dB, 50-mV input | | ±0.5 | | LSB |
| | | Gain = 12 dB, 50-mV input | | ±1.0 | | LSB |
| | No missing codes | | | Ensured | | |
| | Step response settling time | Full-scale step, settle to 1% of step | | 1 | | Pixel |
| | Overload recovery time | 1.4-V step, settle to 1% of step | | 2 | | Pixels |
| | Data latency | | | 10 | | Clocks |
| | RTI signal-to-noise ratio (1) | Grounded input capacitor, gain = 12 dB, IOVDD = 1.8 V, OB pedestal = 248 | | 74.3 | | dB |
| | | Grounded input capacitor, gain = 0 dB | | 72.4 | | dB |
| | CCD offset correction range | | | ±150 | | mV |
| **INPUT CLAMP** | | | | | | |
| | Clamp on-resistance | | | 0.4 | | kΩ |
| | Input clamp voltage | | | 2.2 | | V |
| **PROGRAMMABLE GAIN (CDS)** | | | | | | |
| | Total programmable gain range | | | 51.15 | | dB |
| | Analog gain range | | | 18 | | dB |
| | Digital gain range | | | 33.15 | | dB |
| | Gain control error | | | 0.05 | | dB |
| | Gain step | | | 0.05 | | dB |
| | Additional CDS gain | | | +3.5 | | dB |
| **OPTICAL BLACK CLAMP LOOP** | | | | | | |
| | Optical black clamp level | Programmable range | 64 | | 319 | LSB |
| | | Program step | | 0.5 | | LSB |
| **DIGITAL INPUTS** | | | | | | |
| | Logic family | | | CMOS | | |
| $V_{T+}$ | Input voltage (Schmitt trigger), positive | Low-to-high threshold voltage at IOVDD30 = 3 V | | 1.2 | | V |
| $V_{T-}$ | Input voltage (Schmitt trigger), negative | High-to-low threshold voltage at IOVDD30 = 3 V | | 1.0 | | V |
| | Input capacitance | | | 5 | | pF |
| | Input leakage current high | Logic high | | | 50 | µA |
| | Input leakage current low | Logic low | | | 50 | µA |

(1) RTI (referred to input) SNR = 20 log (output full-scale/output code rms noise) + gain in dB.

## ELECTRICAL CHARACTERISTICS (continued)

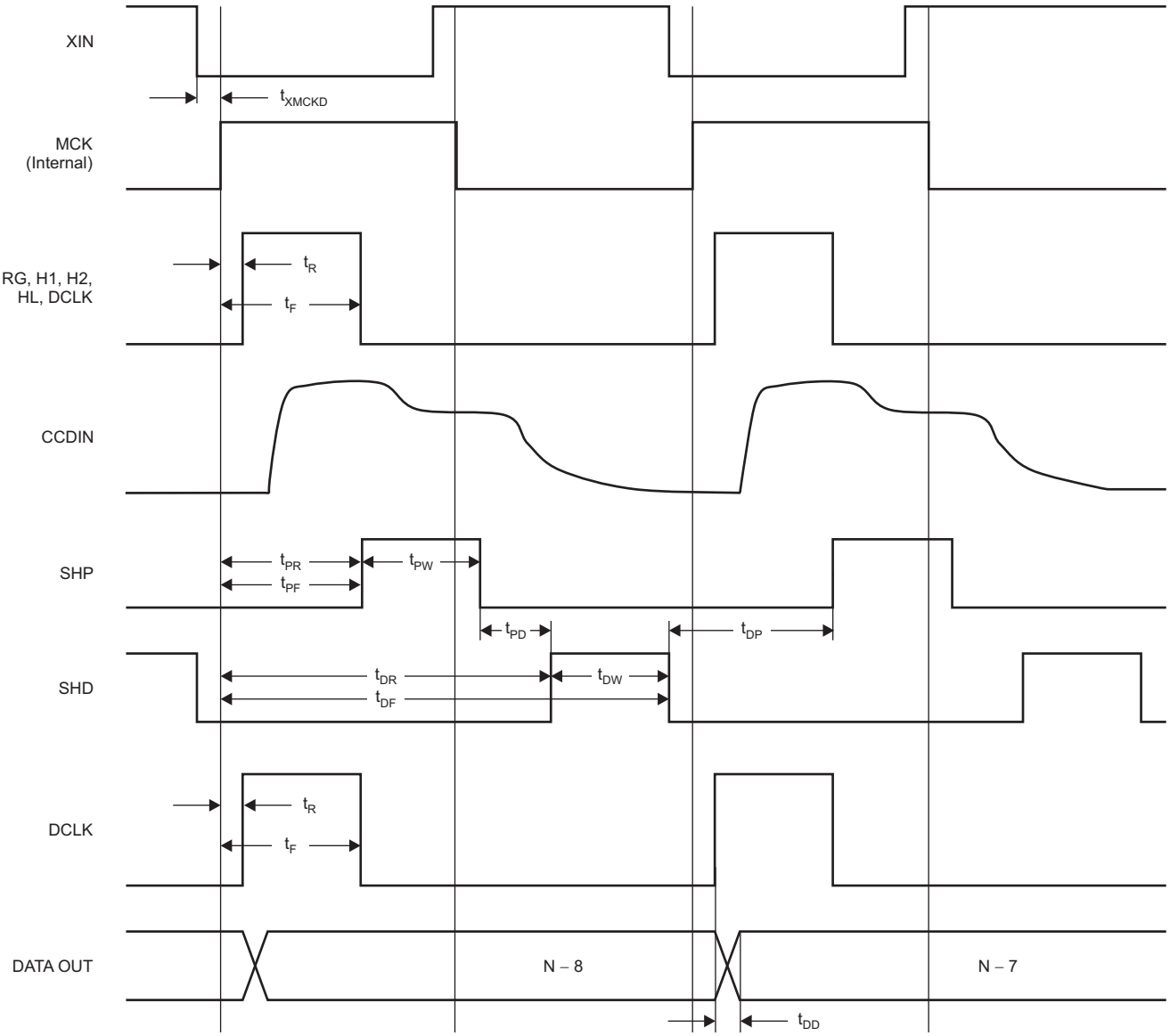
All specifications are at $T_A$ = +25°C, AVDD30 = IOVDD30 = 3.0 V, and conversion rate = 40 MHz, unless otherwise noted.

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **DIGITAL OUTPUTS** | | | | | | | |
| | Logic family | | | | CMOS | | |
| | Logic coding | | | | Straight binary | | |
| $V_{OH}$ | Output voltage, high | | Logic high | | | 2.4 | V |
| $V_{OL}$ | Output voltage, low | | Logic low | | | 0.4 | V |
| **$H_{DRIVER}$ OUTPUTS (OUTPUT VOLTAGE)** | | | | | | | |
| $V_{OH}$ | RG output voltage, high | | $I_{OH}$ = 5 mA | | (0.85)(RGVDD30) | | V |
| $V_{OL}$ | RG output voltage, low | | $I_{OL}$ = 5 mA | | (0.15)(RGVDD30) | | V |
| $V_{OH}$ | HL output voltage, high | | $I_{OH}$ = 5 mA | | (0.85)(HVDD30) | | V |
| $V_{OL}$ | HL output voltage, low | | $I_{OL}$ = 5 mA | | (0.15)(HVDD30) | | V |
| $V_{OH}$ | H1, H2 output voltage, high | | $I_{OH}$ = 30 mA | | (0.85)(HVDD30) | | V |
| $V_{OL}$ | H1, H2 output voltage, low | | $I_{OL}$ = 30 mA | | (0.15)(HVDD30) | | V |
| **TG OUTPUTS (OUTPUT VOLTAGE)** | | | | | | | |
| $V_{OH}$ | HD, VD output voltage, high | | $I_{OH}$ = 3 mA | | (0.85)(IOVDD30) | | V |
| $V_{OL}$ | HD, VD output voltage, low | | $I_{OL}$ = 3 mA | | (0.15)(IOVDD30) | | V |
| **$V_{DRIVER}$ (OUTPUT VOLTAGE)** | | | | | | | |
| $V_{OH}$ | $V_{NUMBER}$ output voltage, high | 3-state | $I_{OH}$ = 9 mA | | 14.5 | | V |
| $V_{OL}$ | $V_{NUMBER}$ output voltage, low | 3-state | $I_{OL}$ = –9 mA | | –7 | | V |
| | | 2-state large | $I_{OL}$ = –9 mA | | –7 | | V |
| | | 2-state small | $I_{OL}$ = –0.5 mA | | –7 | | V |
| $V_{CM}$ | $V_{NUMBER}$ common-mode voltage | 3-state | $I_{CM}$ = ±5 mA | | ±0.2 | | V |
| | | 2-state large | $I_{CM}$ = 5 mA | | –0.2 | | V |
| | | 2-state small | $I_{CM}$ = 0.5 mA | | –0.2 | | V |
| $V_{OH}$ | VSUB voltage output, high | 3-state | $I_{OH}$ = 9 mA | | 14.5 | | V |
| $V_{CM}$ | VSUB common-mode voltage | 3-state | $I_{CM}$ = ±5 mA | | ±0.2 | | V |
| $V_{OL}$ | VSUB voltage output, low | 3-state | $I_{OL}$ = –9 mA | | –7 | | V |
| **POWER SUPPLY** | | | | | | | |
| AFE, logic | Power dissipation | | Normal operation mode: without CCD load, AVDD30 = 2.7 V, IOVDD30 = 1.8 V | | 140 | | mW |
| IO | | | | | 5 | | mW |
| $H_{DRIVER}$ | | | | | 10 | | mW |
| $V_{DRIVER}$ | | | | | 10 | | mW |
| Total | | | | | 165 | | mW |
| Standby | | | Standby mode 1 | | 8 | | mW |
| | | | Standby mode 2 | | 2 | | mW |
| **TEMPERATURE RANGE** | | | | | | | |
| | Operating temperature | | | 0 | | +85 | °C |

# PARAMETER MEASUREMENT INFORMATION

## TIMING REQUIREMENTS

### High-Speed Pulse Timing Specification




NOTE: The SHP, SHD, CLPOB, and CLPDM signals are available as monitor signals. Refer to SLEU107 for enabling this mode and for polarity details.

**Figure 1. High-Speed Timing Diagram**

**Table 1. Timing Characteristics for Figure 1**

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{CKP}$ | MCK clock period | 22 | | 48 | ns |
| $t_{XMCKD}$ | XIN to MCK delay, XTALEN low | | 1 | | ns |
| $t_{XMCKD}$ | XIN to MCK delay, XTALEN high | | 1 | | ns |
| $t_{RGR}$ | MCK rising edge to RG rising edge(1) | $t_{CKP}$ / 100 | 0 | 99 $t_{CKP}$ / 100 | ns |
| $t_{H1R}$ | MCK rising edge to RG falling edge(1) | $t_{CKP}$ / 100 | 24 $t_{CKP}$ / 100 | 99 $t_{CKP}$ / 100 | ns |
| $t_{H2R}$ | MCK rising edge to H1 rising edge(1) | $t_{CKP}$ / 100 | 0 | 99 $t_{CKP}$ / 100 | ns |
| $t_{LHR}$ | MCK rising edge to H1 falling edge(1) | $t_{CKP}$ / 100 | 48 $t_{CKP}$ / 100 | 99 $t_{CKP}$ / 100 | ns |
| $t_{H1F}$ | MCK rising edge to H2 rising edge(1) | $t_{CKP}$ / 100 | 48 $t_{CKP}$ / 100 | 99 $t_{CKP}$ / 100 | ns |
| $t_{H2F}$ | MCK rising edge to H2 falling edge(1) | $t_{CKP}$ / 100 | 0 | 99 $t_{CKP}$ / 100 | ns |
| $t_{LHR}$ | MCK rising edge to HL rising edge(1) | $t_{CKP}$ / 100 | 0 | 99 $t_{CKP}$ / 100 | ns |
| $t_{LHF}$ | MCK rising edge to HL falling edge(1) | $t_{CKP}$ / 100 | 48 $t_{CKP}$ / 100 | 99 $t_{CKP}$ / 100 | ns |
| $t_{PF}$ | MCK rising edge to SHP falling edge(1) | $t_{CKP}$ / 100 | 48 $t_{CKP}$ / 100 | 99 $t_{CKP}$ / 100 | ns |
| $t_{PR}$ | MCK rising edge to SHP rising edge(1) | $t_{CKP}$ / 100 | 24 $t_{CKP}$ / 100 | 99 $t_{CKP}$ / 100 | ns |
| $t_{DF}$ | MCK rising edge to SHD falling edge(1) | $t_{CKP}$ / 100 | 0 | 99 $t_{CKP}$ / 100 | ns |
| $t_{DR}$ | MCK rising edge to SHD rising edge(1) | $t_{CKP}$ / 100 | 76 $t_{CKP}$ / 100 | 99 $t_{CKP}$ / 100 | ns |
| $t_{PD}$ | SHP to SHD spacing | | $t_{CKP}$ / 4 | | ns |
| $t_{DP}$ | SHD to SHP spacing | | $t_{CKP}$ / 4 | | ns |
| $t_{PW}$ | SHP width | 0 | | 99 | ns |
| $t_{DW}$ | SHD width | 0 | | 99 | % |
| $t_{PMDLY}$ | SHP sampling point to monitoring point | –0.7 | 0 | 0.7 | ns |
| $t_{DMDLY}$ | SHD sampling point to monitoring point | –0.7 | 0 | 0.7 | ns |
| DL | Data latency | | 8 | | $t_{CKP}$ cycles |

(1) Pulse phase can be programmed through the serial interface. Refer to SLEU107 for details.

### Serial Interface Timing Specification

The serial interface has two writing modes: standard and continuous write. These modes are shown in Figure 2 and Figure 3, respectively.

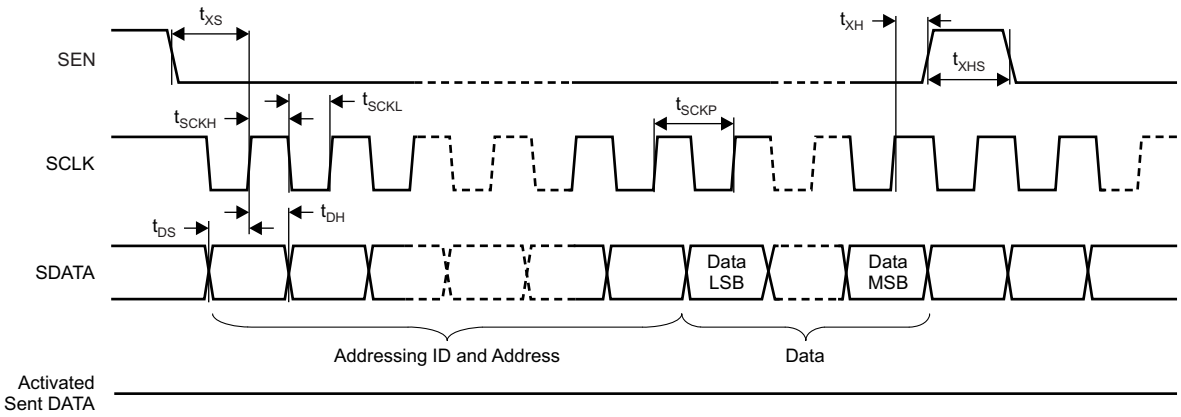



**Figure 2. Standard Mode Timing**

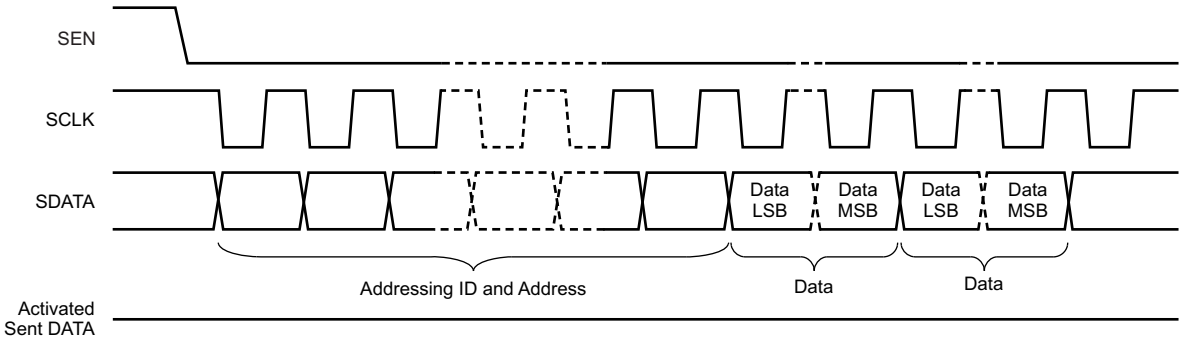



**Figure 3. Continuous Write Mode Timing**

**Table 2. Timing Characteristics for Figure 2 and Figure 3**

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{SCKP}$ | Clock period | 50 | | | ns |
| $t_{SCKH}$ | Clock high pulse width | 25 | | | ns |
| $t_{SCKL}$ | Clock low pulse width | 25 | | | ns |
| $t_{DS}$ | Data setup time | 15 | | | ns |
| $t_{DH}$ | Data hold time | 15 | | | ns |
| $t_{XS}$ | $\overline{CS}$ to SCLK setup time | 20 | | | ns |
| $t_{XH}$ | SCLK to $\overline{CS}$ hold time | 20 | | | ns |
| $t_{XHS}$ | $\overline{CS}$ width | 20 | | | ns |

The data shift operation latches data at the SCLK rising edges while $\overline{CS}$ is low. Parallel latch timing for each mode is the end of MSB data.

In addition to the parallel latch, there are several registers dedicated to the specific features of the devices; these registers are synchronized with MCK. Fewer than 10 clock cycles are required for the data in the parallel latch to be written to these registers. Therefore, to complete data updates, less than 10 clock cycles are required after parallel latching.

### Slave Mode: VD, HD Timing Relationship

The VD and HD phase slave mode timing relationship is specified in Figure 4.

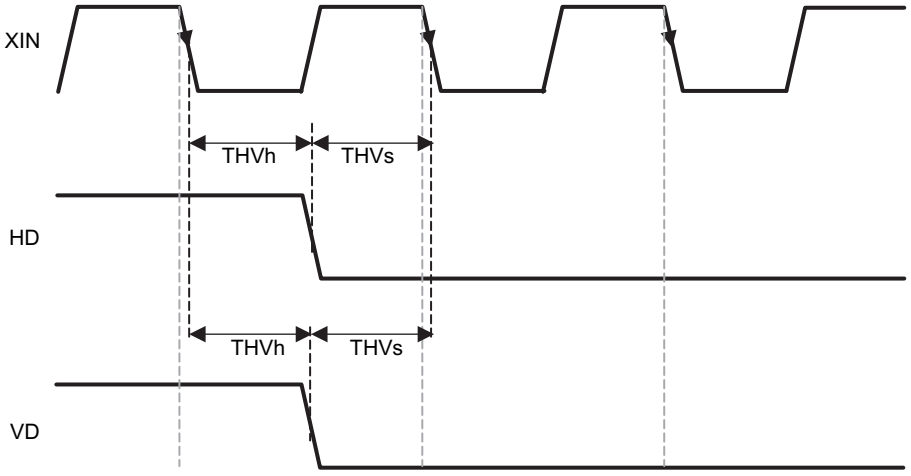



**Figure 4. VD, HD Slave Mode Timing Relationship Diagram**

**Table 3. Timing Characteristics for Figure 4(1)**

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| | XIN to DCLK delay | | 6 | | ns |
| $THV_S$ | VD, HD setup time | 0 | | | ns |
| $THV_H$ | VD, HD hold time | 6 | | | ns |
| | VD, HD to pixel counter reset | | 17 | | τ (MCK cycles) |

(1) These specifications are valid when MCKPOL (register 80h, bit 8) = 0.

### Master Mode: VD, HD Timing Relationship

The VD and HD phase master mode timing relationship is specified in Figure 5.

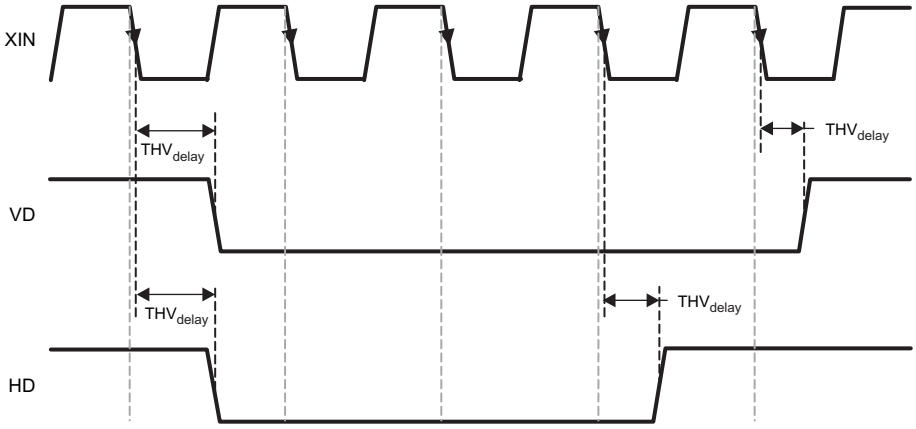



**Figure 5. VD, HD Master Mode Timing Relationship Diagram**

**Table 4. Timing Characteristics for Figure 5 (1)**

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| | XIN to DCLK delay | | 6 | | ns |
| $THV_{DELAY}$ | XIN to VD, HD delay | 3.40 | | 14.66 | ns |
| | VD, HD to pixel counter reset | | 17 | | τ (MCK cycles) |

(1) These specifications are valid when MCKPOL (register 80h, bit 8) = 0.

## EQUIVALENT CIRCUITS

### $H_{DRIVER}$ Load Model

Figure 6 shows the H1 and H2 high-speed driver and load model.

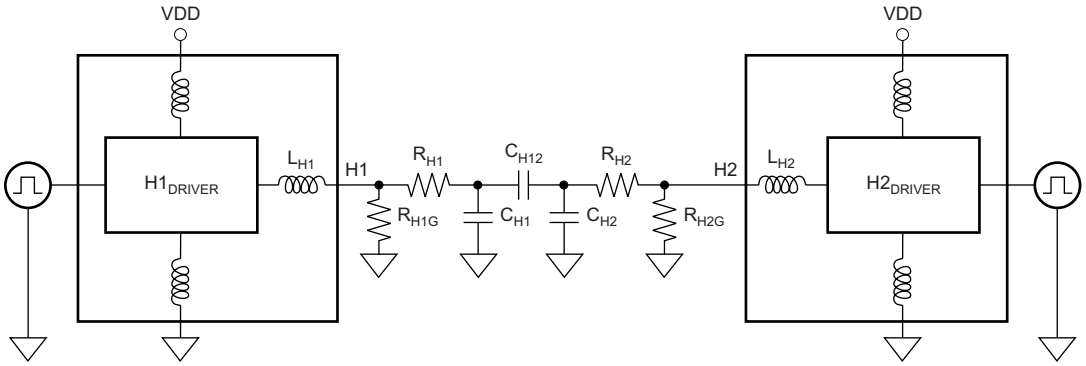



**Figure 6. $H_{DRIVER}$ and Load Model**

### $RG_{DRIVER}$ Load Model

Figure 7 shows the RG high-speed driver and load model.

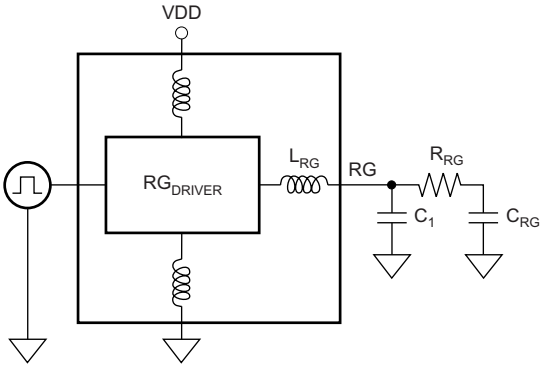



**Figure 7. $RG_{DRIVER}$ and Load Model**

### $HL_{DRIVER}$ Load Model

Figure 8 shows the HL high-speed driver and load model.

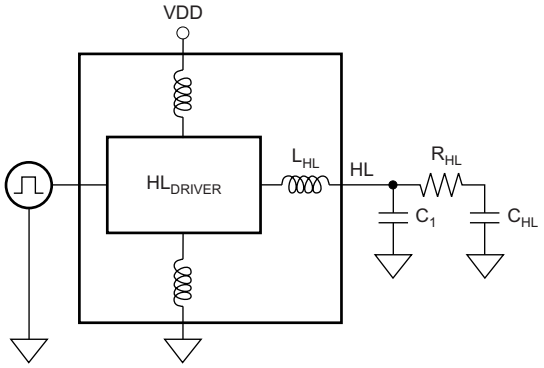



**Figure 8. $HL_{DRIVER}$ and Load Model**

## $RD_{DRIVER}$, $HL_{DRIVER}$, AND $H_{DRIVER}$ DRIVING CURRENT SPECIFICATION

Table 5 lists the $RD_{DRIVER}$, $HL_{DRIVER}$, and $H_{DRIVER}$ driving current specifications.

**Table 5. Driving Current Specification**

| STRENGTH REGISTER | RG, HL (Each in mA at 3.3 V) | H1, H2 (Each in mA at 3.3 V) |
|---|---|---|
| Hi-Z | 0 | 0 |
| 1x | 2 | 8 |
| 2x | 4 | 16 |
| 3x | 6 | 24 |
| 4x | 8 | 32 |
| 5x | 10 | 40 |
| 6x | 12 | 48 |
| 7x | 14 | 56 |

## POWER-ON, POWER-OFF SEQUENCE

If any of the power sources are not supplied, the device may not function properly. The power-on and power-off sequences must be as shown in Figure 9 and Figure 10. Otherwise, the device may malfunction or even be irreversibly damaged.

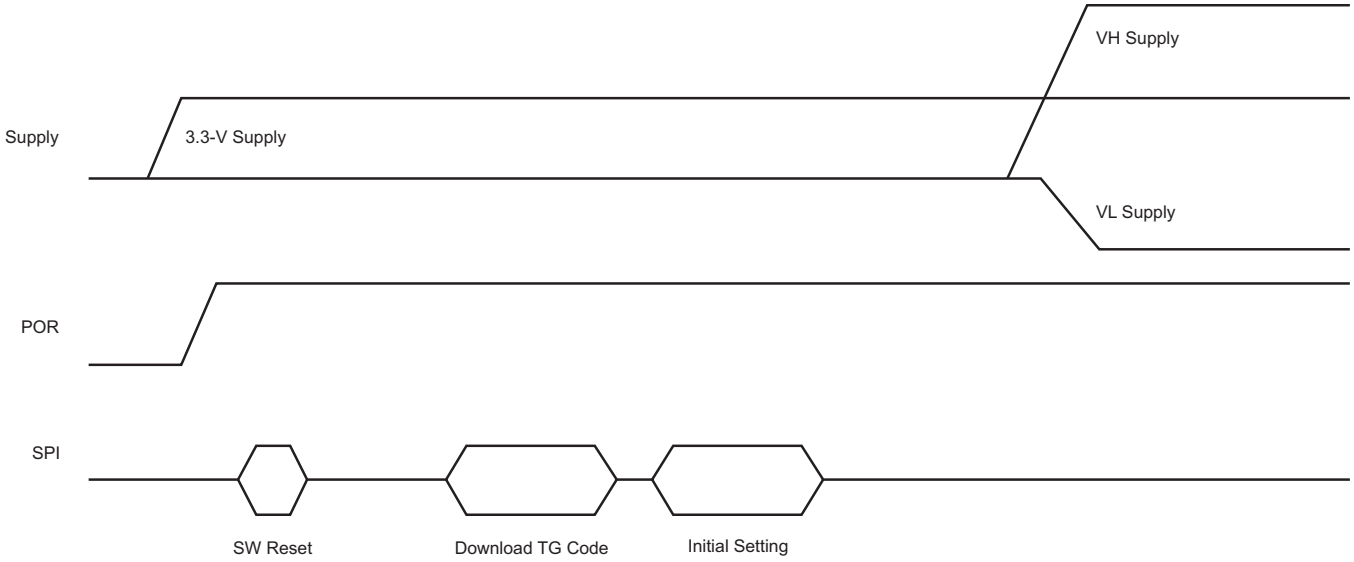



**Figure 9. Power-On Sequence Example**

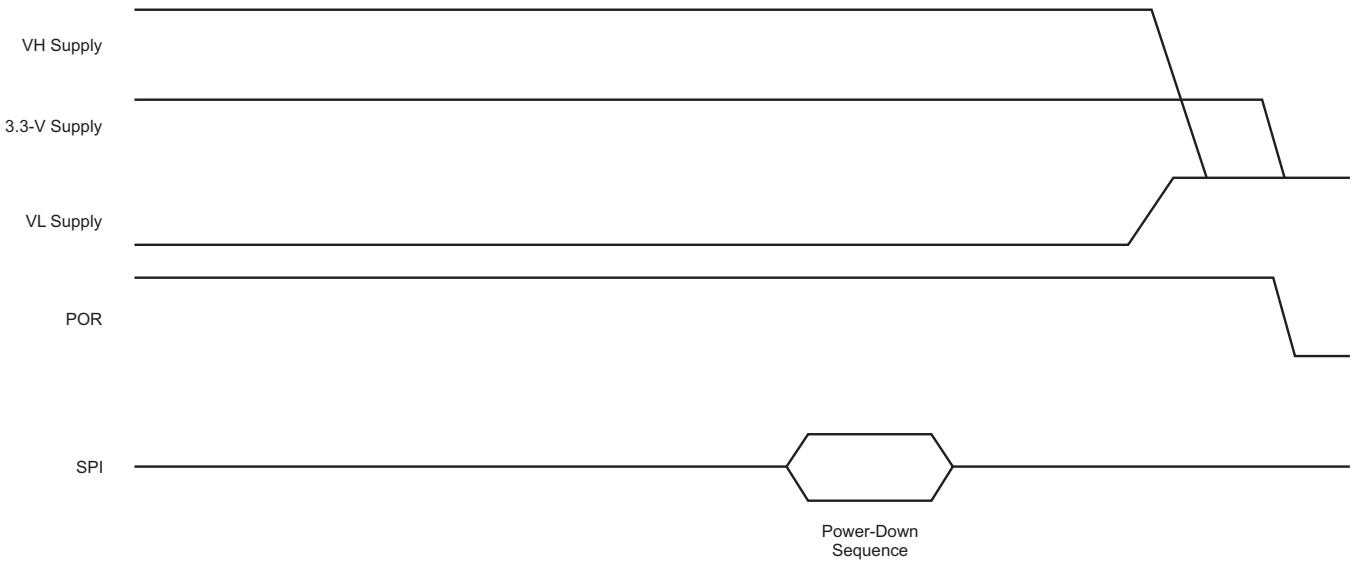
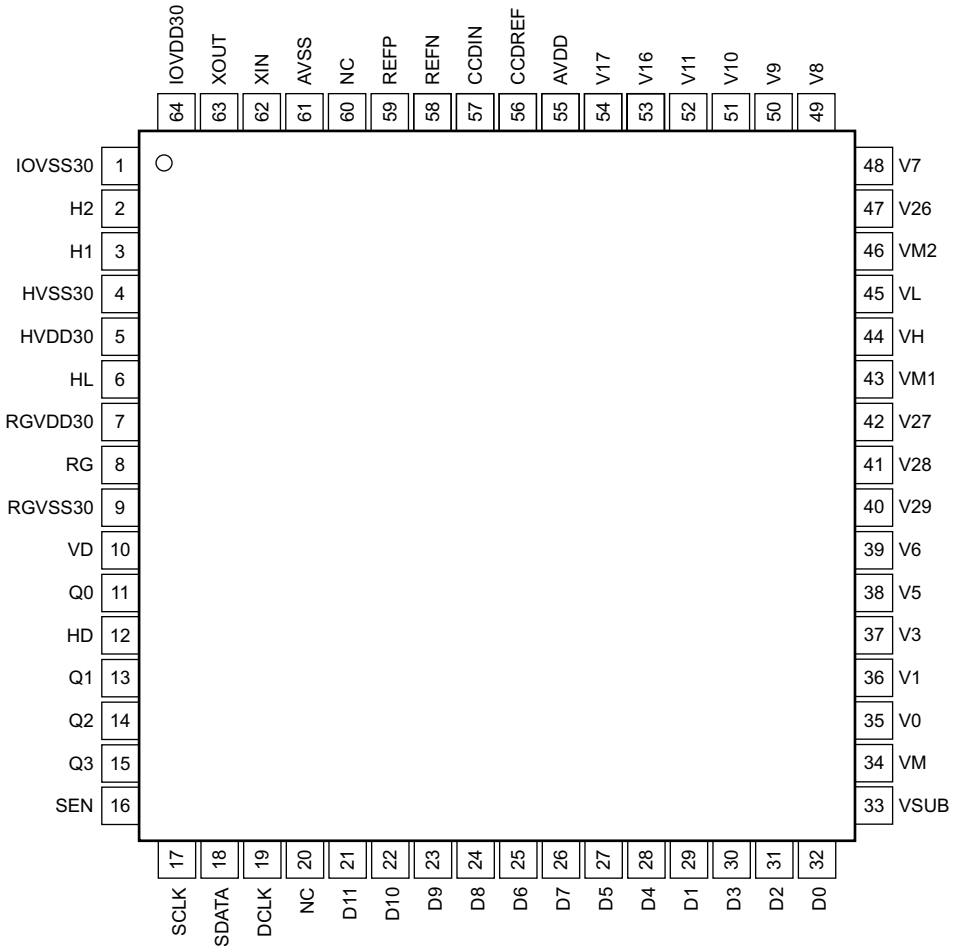



**Figure 10. Power-Off Sequence Example**

## PIN CONFIGURATION

**RSK PACKAGE**
**QFN-64**
**(TOP VIEW)**




NOTE: NC = no connection.

**Table 6. PIN DESCRIPTIONS**

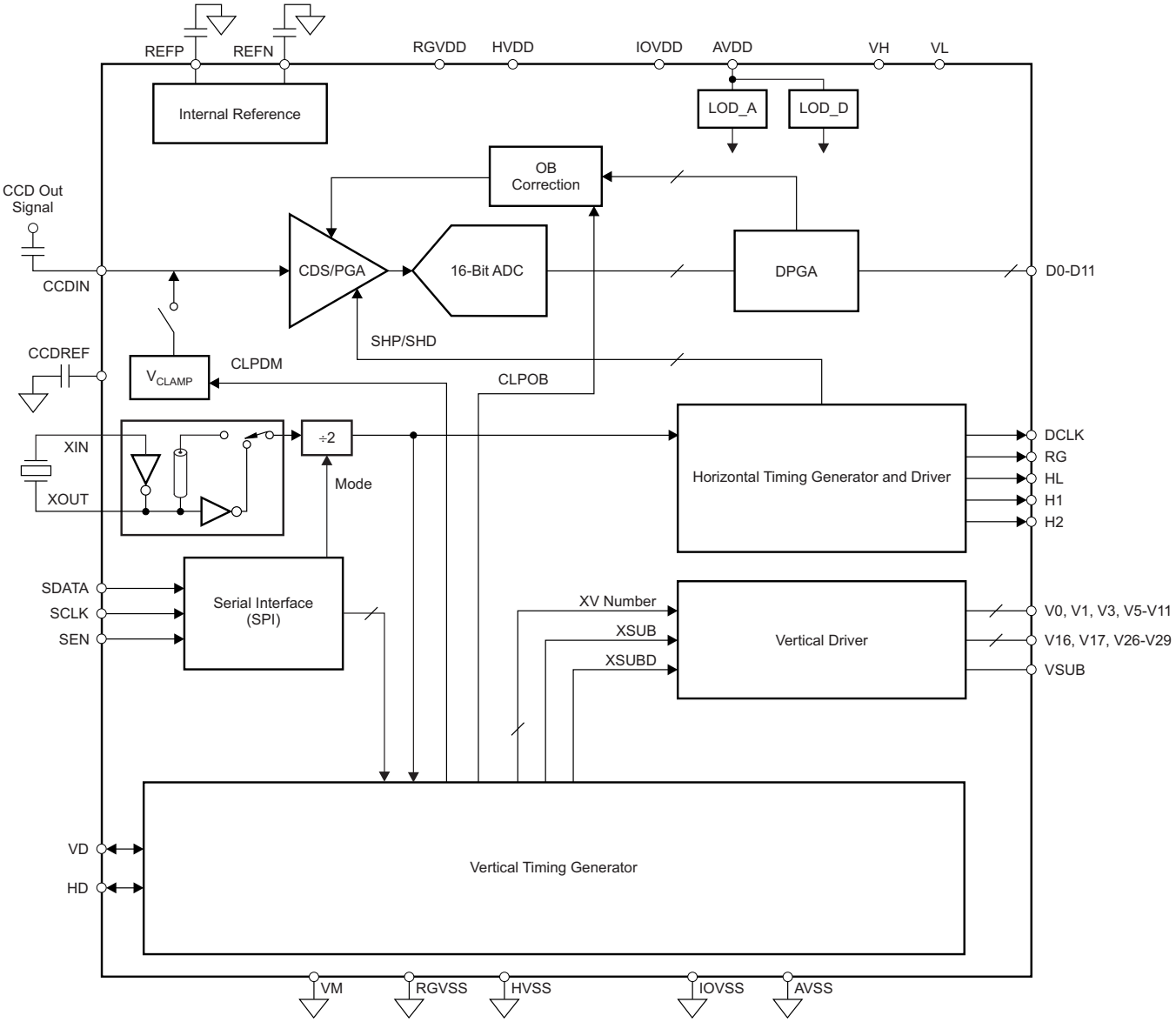
| PIN NUMBER | PIN NAME | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| 1 | IOVSS30 | G | Ground |
| 2 | H2 | HDO | Horizontal drive output |
| 3 | H1 | HDO | Horizontal drive output |
| 4 | HVSS30 | G | Ground |
| 5 | HVDD30 | P | Supply for H1 and H2 drivers |
| 6 | HL | DO | HL horizontal drive output |
| 7 | RGVDD30 | P | Supply for RG and HL driver |
| 8 | RG | DO | Reset gate drive output |
| 9 | RGVSS30 | G | Ground |
| 10 | VD | DIO | Frame synchronization pulse<br>Input = slave mode (default mode = pull-down)<br>Output = master mode |
| 11 | Q0 | DIO | Connect to test pad |
| 12 | HD | DIO | Line synchronization pulse<br>Input = slave mode (default mode = pull-down)<br>Output = master mode |
| 13 | Q1 | DIO | Connect to test pad |
| 14 | Q2 | DIO | Connect to test pad |
| 15 | Q3 | DIO | Connect to test pad |
| 16 | SEN | DI | Serial port interface enable (active low) |
| 17 | SCLK | DI | Serial port interface clock |
| 18 | SDATA | DI | Serial port interface data |
| 19 | DCLK | DO | Data clock output for latching data |
| 20 | NC | — | No connection |
| 21 | D11 | DO | Data output bit 11 |
| 22 | D10 | DO | Data output bit 10 |
| 23 | D9 | DO | Data output bit 9 |
| 24 | D8 | DO | Data output bit 8 |
| 25 | D6 | DO | Data output bit 6 |
| 26 | D7 | DO | Data output bit 7 |
| 27 | D5 | DO | Data output bit 5 |
| 28 | D4 | DO | Data output bit 4 |
| 29 | D1 | DO | Data output bit 1 |
| 30 | D3 | DO | Data output bit 3 |
| 31 | D2 | DO | Data output bit 2 |
| 32 | D0 | DO | Data output bit 0 |
| 33 | VSUB | VDO | $V_{DRIVER}$ SUB output |
| 34 | VM | P | Supply for VSUB middle level |
| 35 | V0 | VDO | $V_{DRIVER}$ output (three level) |
| 36 | V1 | VDO | $V_{DRIVER}$ output (three level) |
| 37 | V3 | VDO | $V_{DRIVER}$ output (three level) |
| 38 | V5 | VDO | $V_{DRIVER}$ output (three level) |
| 39 | V6 | VDO | $V_{DRIVER}$ output (three level) |
| 40 | V29 | VDO | $V_{DRIVER}$ output (two level, small) |
| 41 | V28 | VDO | $V_{DRIVER}$ output (two level, small) |
| 42 | V27 | VDO | $V_{DRIVER}$ output (two level, small) |

(1) Designators by type: AI = analog input; AO = analog output; DI = digital input; DO = digital output; G = ground; HDO = $H_{DRIVER}$ output; P = power supply; and VDO = $V_{DRIVER}$ output.

**Table 6. PIN DESCRIPTIONS (continued)**

| PIN NUMBER | PIN NAME | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| 43 | VM1 | P | Supply for $V_{DRIVER}$ output, middle level |
| 44 | VH | P | Supply for $V_{DRIVER}$, high level |
| 45 | VL | P | Supply for $V_{DRIVER}$ output, low level |
| 46 | VM2 | P | Supply for $V_{DRIVER}$ output, middle level |
| 47 | V26 | VDO | $V_{DRIVER}$ output (two level, small) |
| 48 | V7 | VDO | $V_{DRIVER}$ output (three level) |
| 49 | V8 | VDO | $V_{DRIVER}$ output (three level) |
| 50 | V9 | VDO | $V_{DRIVER}$ output (three level) |
| 51 | V10 | VDO | $V_{DRIVER}$ output (three level) |
| 52 | V11 | VDO | $V_{DRIVER}$ output (three level) |
| 53 | V16 | VDO | $V_{DRIVER}$ output (two level, small) |
| 54 | V17 | VDO | $V_{DRIVER}$ output (two level, small) |
| 55 | AVDD | P | Analog supply |
| 56 | CCDREF | AI | CCD ground reference; decouple to ground with a 0.1-µF capacitor close to the device |
| 57 | CCDIN | AI | CCD signal input; couple with a 0.1-µF capacitor |
| 58 | REFN | AO | ADC low reference voltage; decouple to ground with a 0.1-µF capacitor close to the device |
| 59 | REFP | AO | ADC high reference voltage; decouple to ground with a 0.1-µF capacitor close to the device |
| 60 | NC | — | No connection |
| 61 | AVSS | G | Ground |
| 62 | XIN | AI, DI | Crystal oscillator and external clock input |
| 63 | XOUT | AO | Crystal oscillator inverter output |
| 64 | IOVDD30 | P | I/O supply |

## FUNCTIONAL BLOCK DIAGRAM



## COMMON SECTION

The device includes an analog front-end (AFE) section, timing generator (TG) section, and $V_{DRIVER}$, which are each explained later in this document. The primary functionality of this device is:

- Serial interface ( SPI™) for programming,
- Control of register update timing,
- System reset via function pin or software,
- Crystal input support, and
- 8-bit general-purpose digital-to-analog converter (GP DAC).

Each setting of the AFE and timing generator (TG) is programmed with a serial interface (SPI). Some register settings are stored in the buffer through the SPI. This configuration is activated by a defined timing. For example, some areas of the register are activated at the VD active edge. A system reset function is supported by a function pin or register. For MCK, both external MCK and crystal input methods are supported. The GP DAC can be used as an external circuit. Figure 11 shows a block diagram of the Common section.

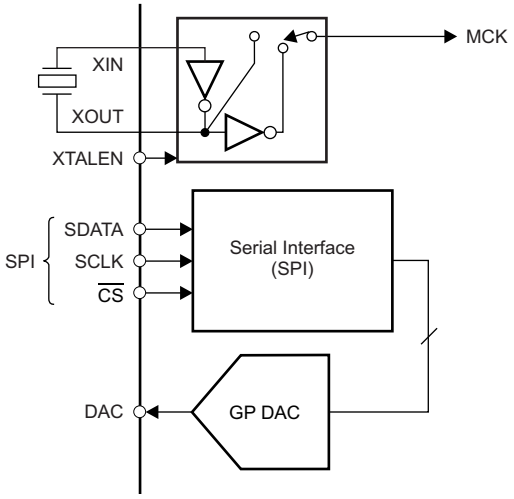



**Figure 11. Common Section Block Diagram**

## SERIAL INTERFACE (SPI) FOR PROGRAMMING

The functions and timings are controlled through the serial interface, which consists of three signals: SDATA, SCLK, and $\overline{CS}$ for writing and a fourth signal (SOUT) for reading. SDATA data are sequentially stored to the shift register at the SCLK rising edge. Before a write operation, $\overline{CS}$ must go low and remain low during writing. Refer to the *Serial Interface Timing Specification* for further details.

The serial interface command is composed of an 8-bit addressing ID, a 16-bit address, and 24-bit data. Reserved registers cannot be written to. Most importantly, addresses FEh and FFh are reserved to prevent confusion in the addressing ID. The SPI has two sequence modes: standard mode and continuous mode. Table 7 shows the SPI mode matrix.

**Table 7. SPI Mode For Accessible Areas**

| READ/WRITE | ADDRESSING ID (8-Bit) | SEQUENCE MODE | ACCESS AREA |
|---|---|---|---|
| Write | FEh | Standard | Register and memory |
| | | Continuous | |
| Read | FFh | Standard | |
| | | Continuous | |

### Standard Write Mode

Normally, one serial interface command is sent by one addressing ID, address, and data combination. The 16-bit address should be sent LSB first; the following 24-bit data should also sent LSB first. Data are stored in the respective register by the address. If data do not equal 24 bits at the end of the data stream, any empty data bits are discarded. The addressing ID value is fixed as FEh. Figure 12 shows the SPI standard write mode timing.

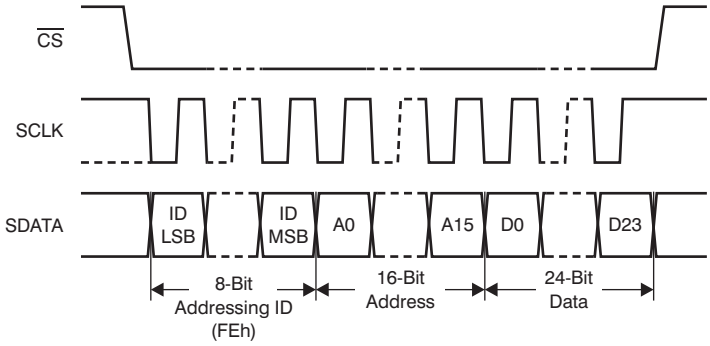



**Figure 12. SPI Standard Write Mode for Register and Memory**

### Continuous Write Mode

This device also supports a continuous write mode, as shown in Figure 13. When the input serial data are longer than one set of instructions, the following data stream is automatically recognized as the data of the next address.

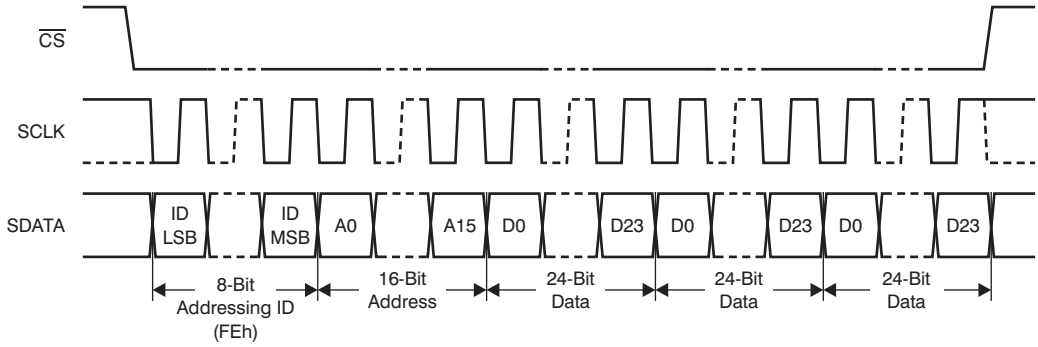



**Figure 13. SPI Continuous Write Mode for Register and Memory**

## AFE (ANALOG FRONT-END) SECTION

The VSP8133 is a complete mixed-signal device that contains all key features associated with the processing of the CCD imager output signal in a video camera, digital still camera, security camera, or other similar applications. A simplified block diagram of the AFE section is shown in Figure 14. The AFE section includes:

- Correlated double sampler (CDS),
- Programmable gain amplifier (PGA),
- Input clamp,
- Analog-to-digital converter (ADC),
- Optical black (OB) level clamp loop,
- Timing control,
- Internal reference voltage generator, and
- Hot pixel rejection.

An off-chip emitter follower buffer is recommended to be placed between the CCD output and the VSP8133 CCDIN input. The serial interface controls PGA gain, clock polarity setting, and operating mode.

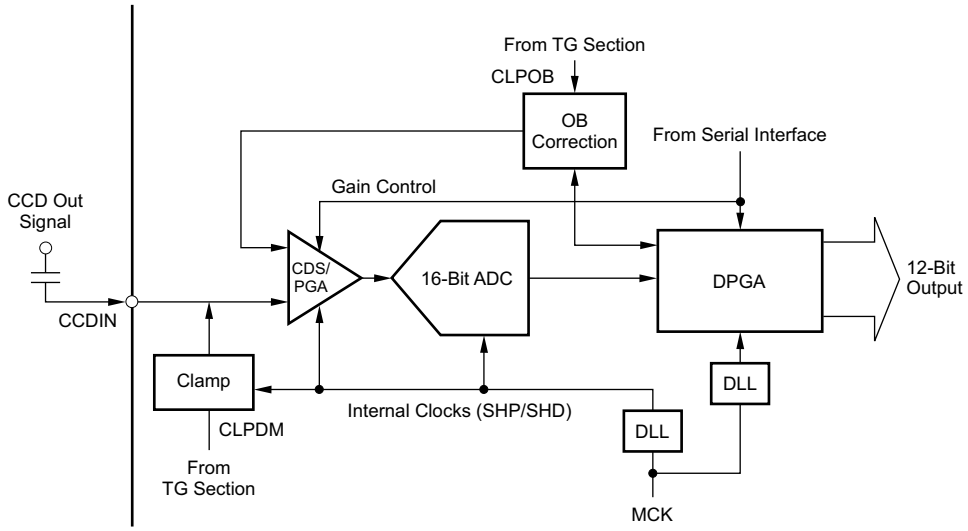



**Figure 14. AFE Section Block Diagram**

## TIMING GENERATOR (TG) SECTION

This device supports variable CCD timing. For horizontal and vertical sequences, full programming is available. The TG section has the following major functionality:

- Programmable horizontal pattern,
- Programmable vertical pattern,
- Programmable $V_{CCD}$ high-speed transfer pattern,
- Electrical zoom function,
- Sync signal selectable (master or slave),
- Programmable electrical shutter,
- Frame mode control via trigger,
- Waiting mode via trigger,
- Pixel summing operation,
- Adjustable high-speed pulse ($H_{DRIVER}$ and AFE control),
- Selectable $H_{DRIVER}$ power,
- Auto frame change mode, and
- Monitor out for internal signal.

VA, which is a programmable vertical sequence, supports a 32-frame mode. HA, which is a programmable horizontal sequence, has enough memory area for motion picture mode. HS, which is a programmable vertical high-speed transfer, can be used for electrical zooming or as a vibration canceller. The high-speed signal generator that controls the $H_{DRIVER}$ signals can be adjusted in 100 fine steps for falling and rising signal timing. Similarly, AFE sampling signals can be adjusted in 100 fine steps for falling and rising signal timing. A simplified block diagram is shown in Figure 15.

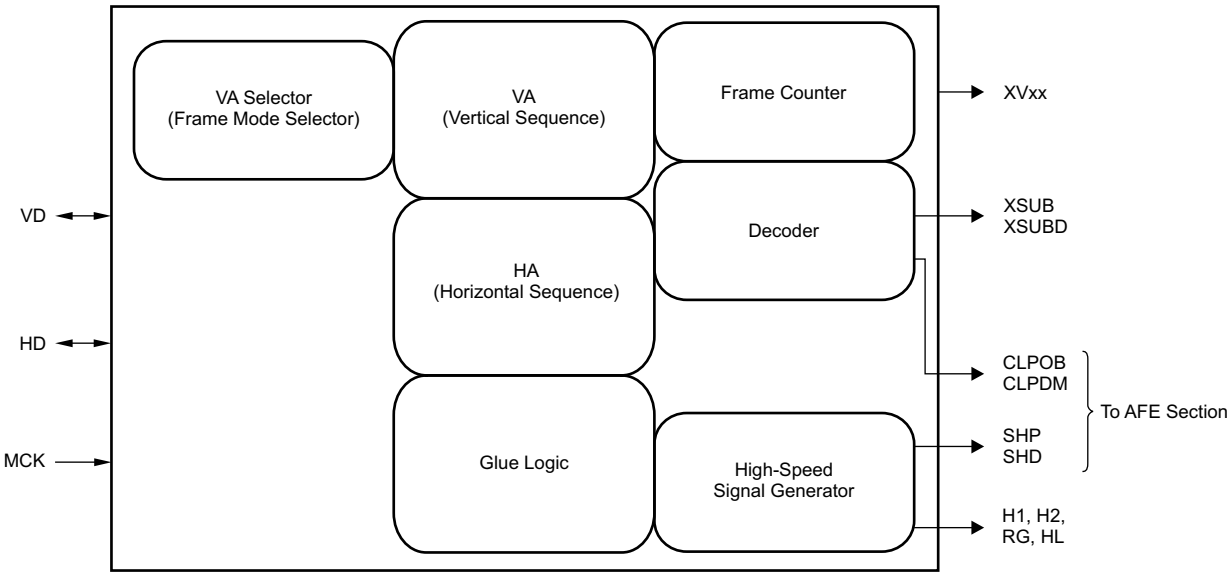



**Figure 15. TG Section Block Diagram**

## $V_{DRIVER}$ SECTION

### VSUB 3-Level Output

Table 8 describes the 3-level output of VSUB.

**Table 8. VSUB 3-Level Output**

| INPUT (TG OUTPUT) | | OUTPUT (DEVICE PIN OUTPUT) | |
|---|---|---|---|
| SIGNAL NAME | | SIGNAL NAME | DRIVE CAPABILITY |
| XSUB | XSUBD | VSUB | 1000 pF through 30 Ω |
| TRUTH TABLE | | LEVEL(1) | |
| XSUB | XSUBD | | |
| Low | Low | VH | |
| | High | Hi-Z | |
| High | Low | VL | |
| | High | VM | |

(1) VH = high level; Hi-Z = high impedance; VL = low level; and VM = middle level.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| VSP8133RSKR | ACTIVE | QFN | RSK | 64 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | 0 to 85 | VSP8133 | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

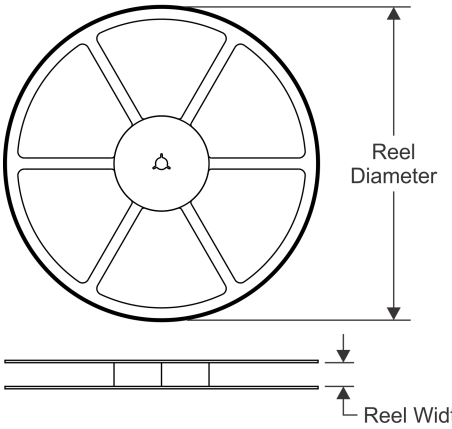
**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

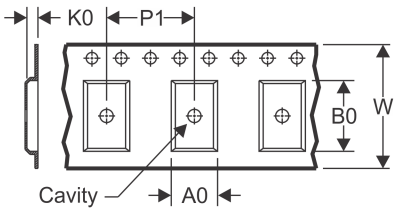
**(4)** Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

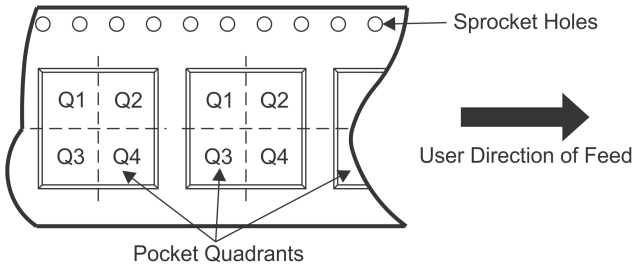



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

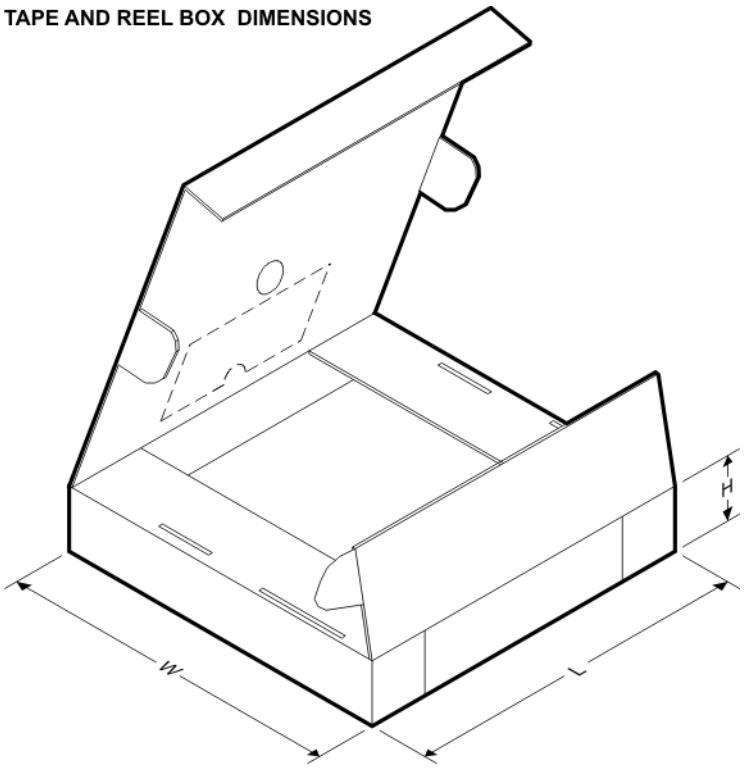
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VSP8133RSKR | QFN | RSK | 64 | 2000 | 330.0 | 16.4 | 8.3 | 8.3 | 2.25 | 12.0 | 16.0 | Q2 |

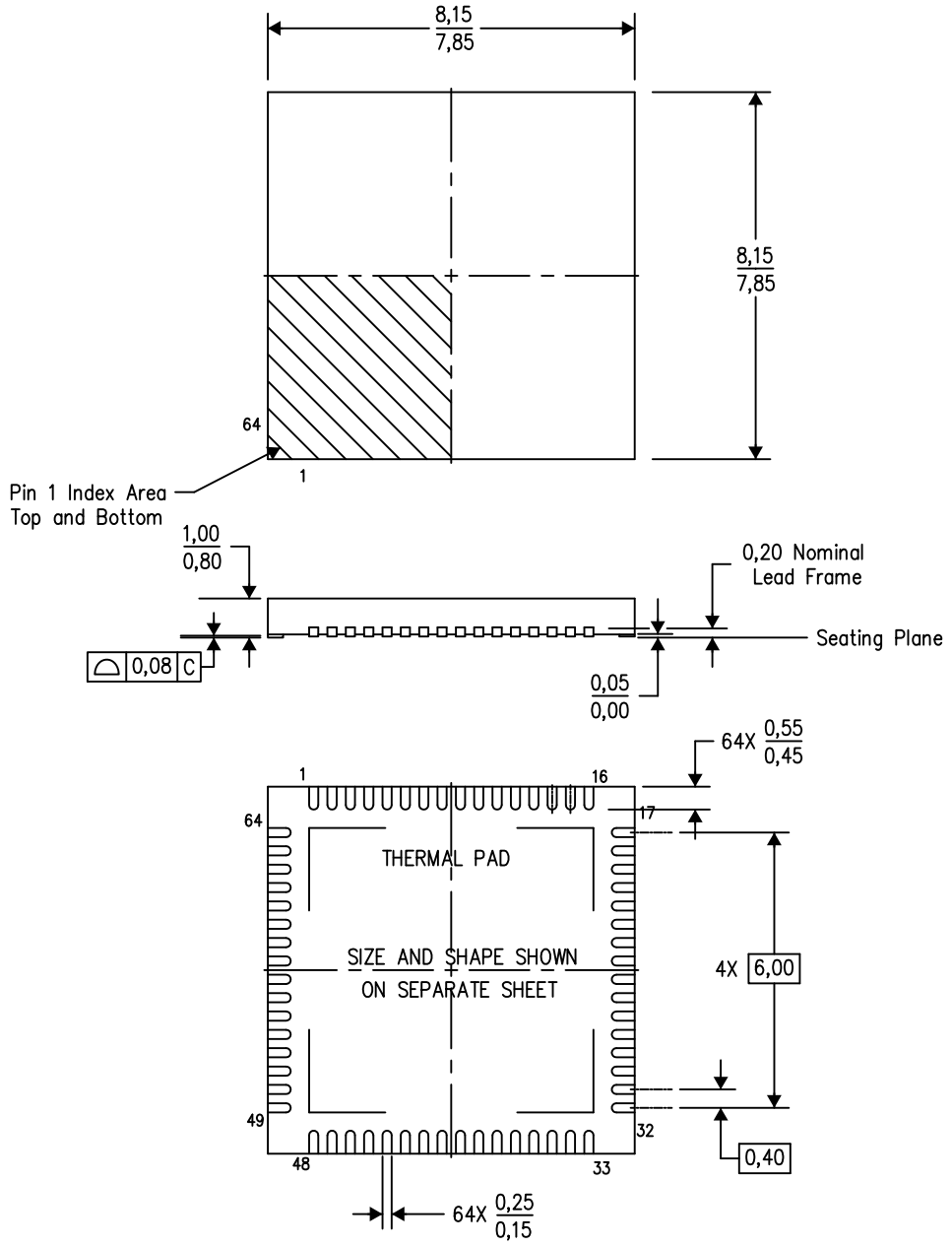
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| VSP8133RSKR | QFN | RSK | 64 | 2000 | 367.0 | 367.0 | 38.0 |

RSK (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD




Bottom View

4207547/C 04/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

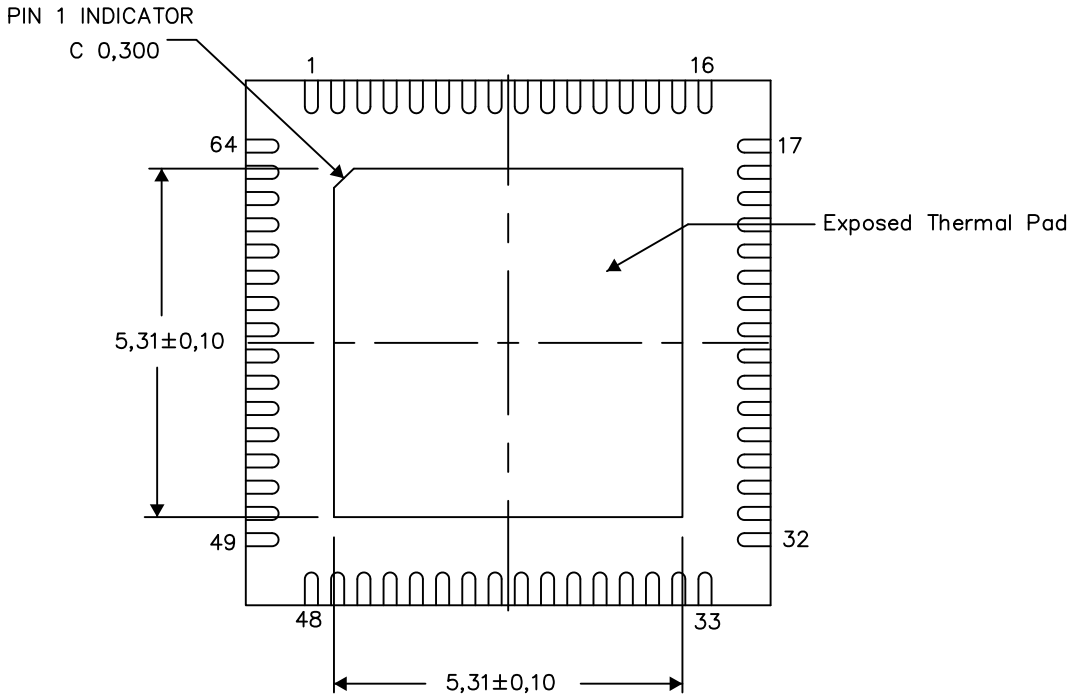
RSK (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



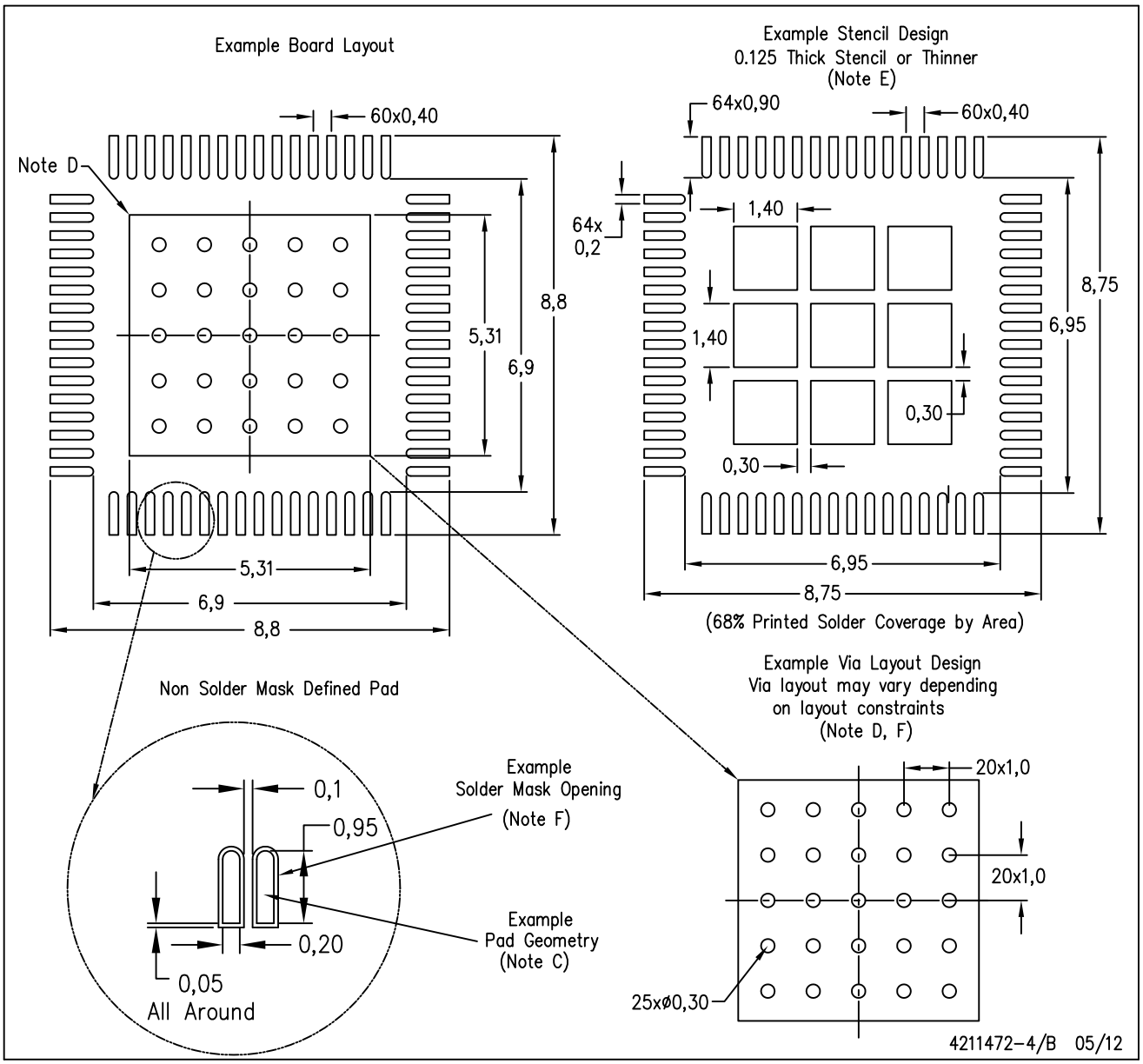

Bottom View

Exposed Thermal Pad Dimensions

4208001–4/F 05/12

NOTE: A. All linear dimensions are in millimeters

# RSK (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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