

ISO175

## Precision, Isolated INSTRUMENTATION AMPLIFIER

### FEATURES

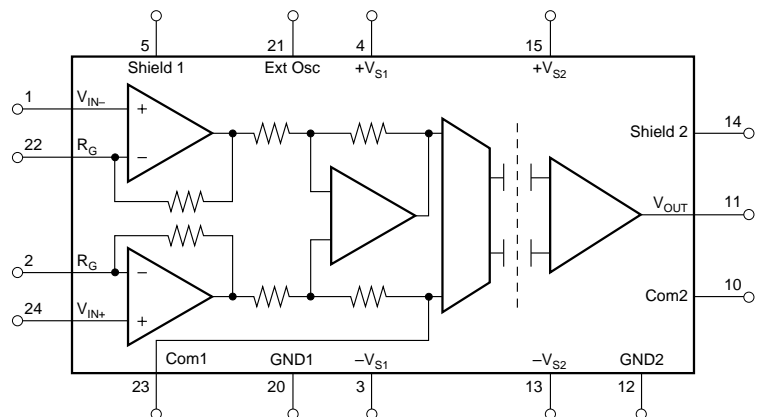
- **RATED**  
1500Vrms Continuous  
2500Vrms for One Minute  
100% TESTED FOR PARTIAL DISCHARGE
- **HIGH IMR: 115dB at 50Hz**
- **LOW NONLINEARITY:  $\pm 0.01\%$**
- **LOW INPUT BIAS CURRENT: 10nA max**
- **LOW INPUT OFFSET VOLTAGE: 101mV max**
- **INPUTS PROTECTED TO  $\pm 40V$**
- **BIPOLAR OPERATION:  $V_O = \pm 10V$**
- **SYNCHRONIZATION CAPABILITY**
- **24-PIN PLASTIC DIP: 0.3" Wide**

### DESCRIPTION

ISO175 is a precision isolated instrumentation amplifier incorporating a novel duty cycle modulation-demodulation technique and excellent accuracy. A single external resistor sets the gain. Internal input protection can withstand up to  $\pm 40V$  without damage. The signal is transmitted digitally across a differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity. This results in excellent reliability and good high frequency transient immunity across the barrier. Both the amplifier and barrier capacitors are housed in a plastic DIP. ISO175 is easy to use. A power supply range of  $\pm 4.5V$  to  $\pm 18V$  makes this amplifier ideal for a wide range of applications.

### APPLICATIONS

- **INDUSTRIAL PROCESS CONTROL**  
Transducer Isolator, Thermocouple Isolator, RTD Isolator, Pressure Bridge Isolator, Flow Meter Isolator
- **POWER MONITORING**
- **MEDICAL INSTRUMENTATION**
- **ANALYTICAL MEASUREMENTS**
- **BIOMEDICAL MEASUREMENTS**
- **DATA ACQUISITION**
- **TEST EQUIPMENT**
- **POWER MONITORING**
- **GROUND LOOP ELIMINATION**



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111  
Internet: <http://www.burr-brown.com/> • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

# SPECIFICATIONS

At  $T_A = +25^\circ\text{C}$ ,  $V_{S1} = V_{S2} = \pm 15\text{V}$ , and  $R_L = 2\text{k}\Omega$  unless otherwise noted.

PARAMETER	CONDITIONS	ISO175P			UNITS
		MIN	TYP	MAX	
<b>ISOLATION<sup>(1)</sup></b> Voltage Rated Continuous: AC DC 100% Test (AC, 50Hz) Isolation-Mode Rejection AC 50Hz DC Barrier Impedance Leakage Current	$T_{\text{MIN}}$ to $T_{\text{MAX}}$ $T_{\text{MIN}}$ to $T_{\text{MAX}}$ 1s; Partial Discharge $\leq 5\text{pC}$  1500Vrms  VISO = 240Vrms, 50Hz	1500 2121 2500	   115 160 $10^{14} \parallel 6$ 0.8	     1	Vrms VDC Vrms  dB dB $\Omega \parallel \text{pF}$ $\mu\text{Arms}$
<b>GAIN</b>  Gain Error  Gain vs Temperature Nonlinearity	  G = 1 G = 10 G = 100  G = 1 G = 1 G = 10 G = 100	        	$1 + \left( \frac{50\text{k}}{R_G} \right)$  $\pm 0.07$  $\pm 11$  $\pm 0.04$	  $\pm 0.35$ $\pm 0.95$  $\pm 0.102$ $\pm 0.104$	V/V  % % % ppm/ $^\circ\text{C}$ % % %
<b>INPUT OFFSET VOLTAGE</b> Initial Offset  vs Temperature  vs Supply	G = 1, 100   G = 1	   	  $\pm \left( 1 + \frac{520}{G} \right)$ $\pm 2$	$\pm \left( 0.125 + \frac{101}{G} \right)$	mV  $\mu\text{V}/^\circ\text{C}$  mV/V
<b>INPUT</b> Voltage Range Bias Current vs Temperature Offset Current vs Temperature		$\pm 10$	  $\pm 40$  $\pm 40$	  $\pm 10$  $\pm 10$	V nA $\text{pA}/^\circ\text{C}$ nA $\text{pA}/^\circ\text{C}$
<b>OUTPUT</b> Voltage Range Current Drive Capacitive Load Drive Ripple Voltage		$\pm 10$ $\pm 5$	  0.1 10	   	V mA $\mu\text{F}$ mVp-p
<b>FREQUENCY RESPONSE</b> Small Signal Bandwidth  Slew Rate	G = 1 G = 10 G = 100 $V_O = \pm 10\text{V}, G = 10$	   	60 60 50 0.9	   	kHz kHz kHz V/ $\mu\text{s}$
<b>POWER SUPPLIES</b> Rated Voltage Voltage Range Quiescent Current $V_{S1}$ $V_{S2}$		$\pm 4.5$	15	$\pm 18$  $\pm 7.4$ $\pm 7.5$	V V  mA mA
<b>TEMPERATURE RANGE</b> Operating Storage		$-40$ $-40$		85 125	$^\circ\text{C}$ $^\circ\text{C}$

NOTE: (1) All devices receive a 1s test. Failure criterion is  $\geq 5$  pulses of  $\geq 5\text{pC}$ .

## ABSOLUTE MAXIMUM RATINGS

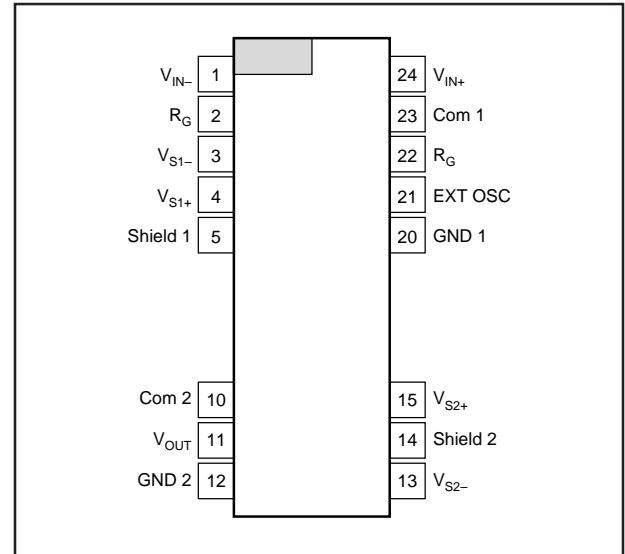
Supply Voltage .....	±18V
Analog Input Voltage Range .....	±40V
External Oscillator Input .....	±25V
Com 1 to GND1 .....	±1V
Com 2 to GND2 .....	±1V
Continuous Isolation Voltage: .....	1500Vrms
IMV, dv/dt .....	20kV/μs
Junction Temperature .....	150°C
Storage Temperature .....	-40°C to +125°C
Lead Temperature (soldering, 10s) .....	+300°C
Output Short Duration .....	Continuous to Common

## ELECTROSTATIC DISCHARGE SENSITIVITY

Any integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PIN CONFIGURATION



## PACKAGE/ORDERING INFORMATION

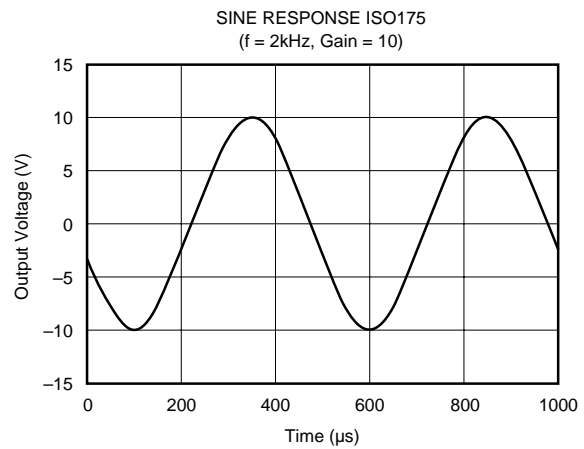
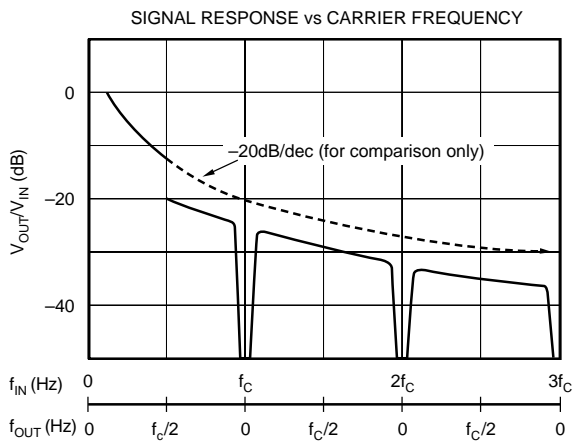
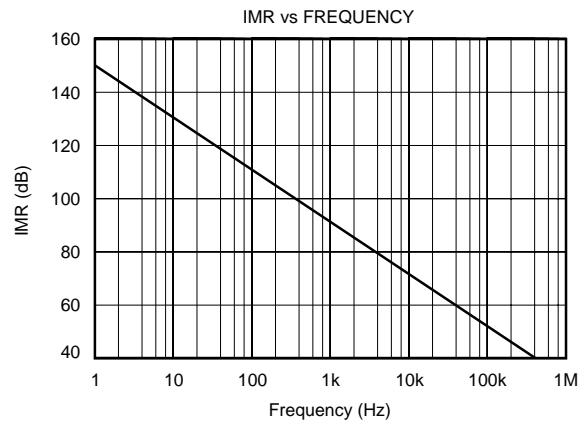
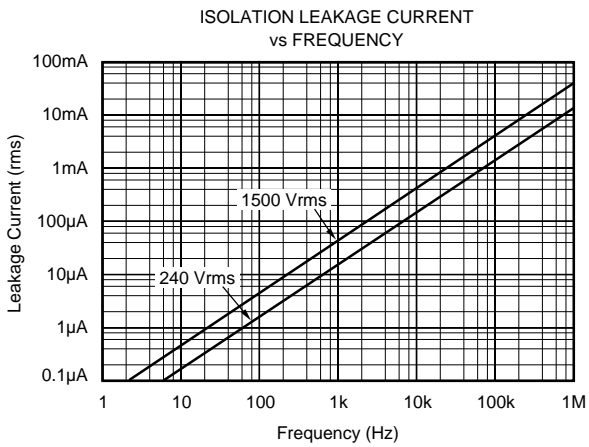
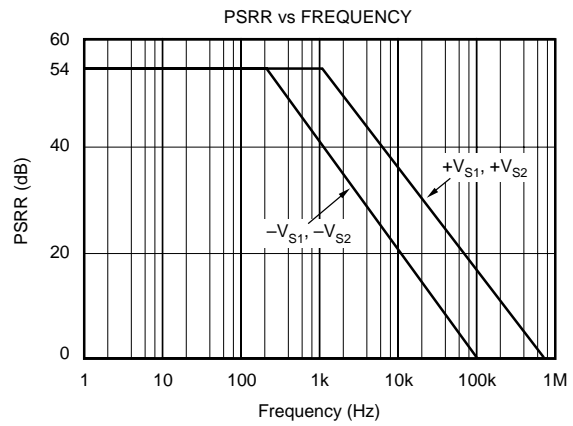
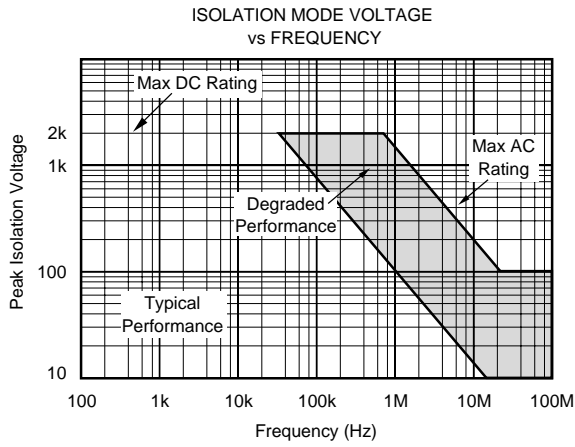
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER <sup>(1)</sup>	BANDWIDTH
ISO175P	24-Pin Plastic DIP	243-2	60kHz

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

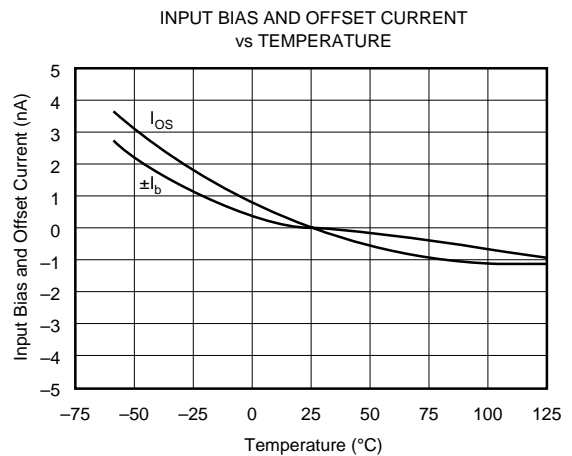
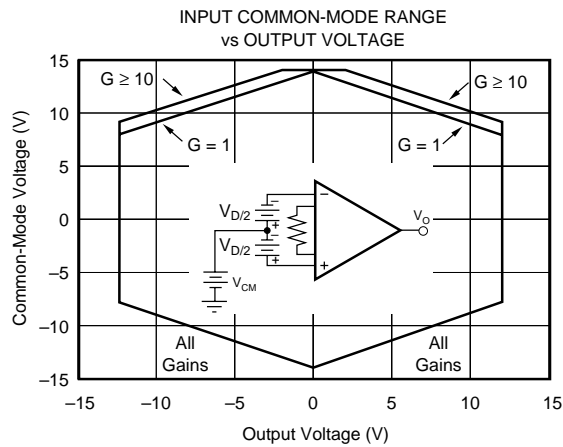
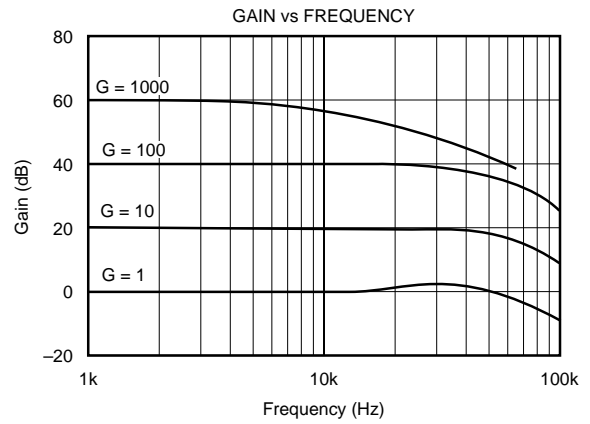
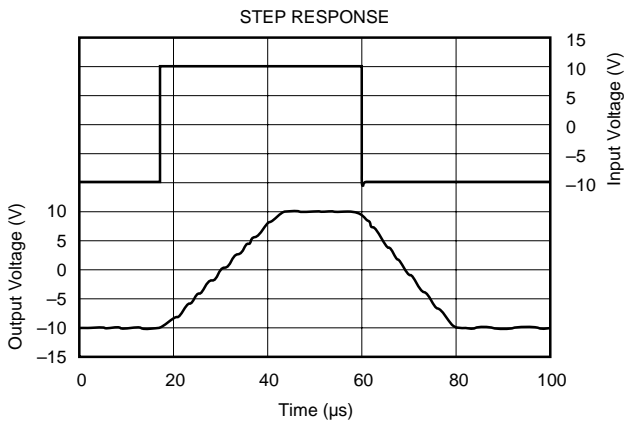
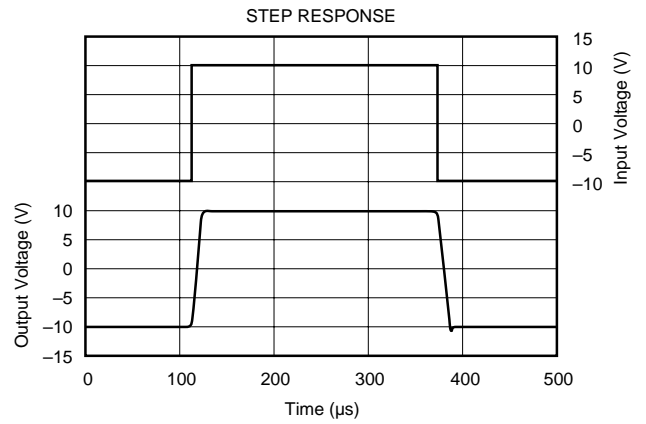
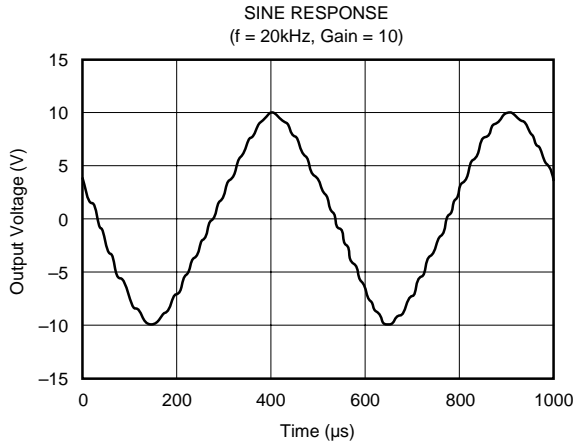
# TYPICAL PERFORMANCE CURVES

At  $T_A = +25^\circ\text{C}$ ,  $V_{S1} = V_{S2} = \pm 15\text{V}$ , and  $R_L = 2\text{k}\Omega$ , unless otherwise noted.



# TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$ ,  $V_{S1} = V_{S2} = \pm 15\text{V}$ , and  $R_L = 2\text{k}\Omega$ , unless otherwise noted.



# BASIC OPERATION

ISO175 instrumentation input isolation amplifier comprises of a precision instrumentation amplifier followed by an isolation amplifier. The input and output isolation sections are galvanically isolated and EMI shielded by matched capacitors.

## Signal and Power Connections

Figure 1 shows power and signal connections. Each power supply pin should be bypassed with a 1µF tantalum capacitor located as close to the amplifier as possible. All ground connections should be run independently to a common point if possible. Signal Common on both input and output sections provide a high-impedance point for sensing signal ground in noisy applications. Com 1 and Com 2 must have a path to ground for bias current return and should be maintained within ±1V of GND1 and GND2, respectively.

## SETTING THE GAIN

Gain of the ISO175 is set by connecting a single external resistor R<sub>G</sub>, connected between pins 2 and 22.

$$G = 1 + \frac{50k\Omega}{R_G} \quad (1)$$

Commonly used gains and resistor values are shown in Figure 1.

The 50kΩ term in equation (1) comes from the sum of the two internal feedback resistors. These on-chip metal film resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of this resistor are included in the gain accuracy and drift specifications of the ISO175.

The stability and temperature drift of the external gain setting resistor R<sub>G</sub>, also affects gain. R<sub>G</sub>'s contribution to gain accuracy and drift can be directly inferred from the

gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

## INPUT COMMON-MODE RANGE

The linear voltage range of the input circuitry of the ISO175 is from approximately 2.5V below the positive supply voltage to 2.5V above the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range will be limited by the output voltage swing of the internal amplifiers. Thus, the linear common-mode input range is related to the output voltage of the complete input amplifier.

This behavior also depends on the supply voltage—see performance curves “Input Common-Mode Range vs Output Voltage.”

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of the ISO175 will be near 0V even though both inputs are overloaded.

## INPUT PROTECTION

The input of the ISO175 is individually protected for voltages up to ±40V referenced to GND1. For example, a condition of -40V on one input and +40V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded,

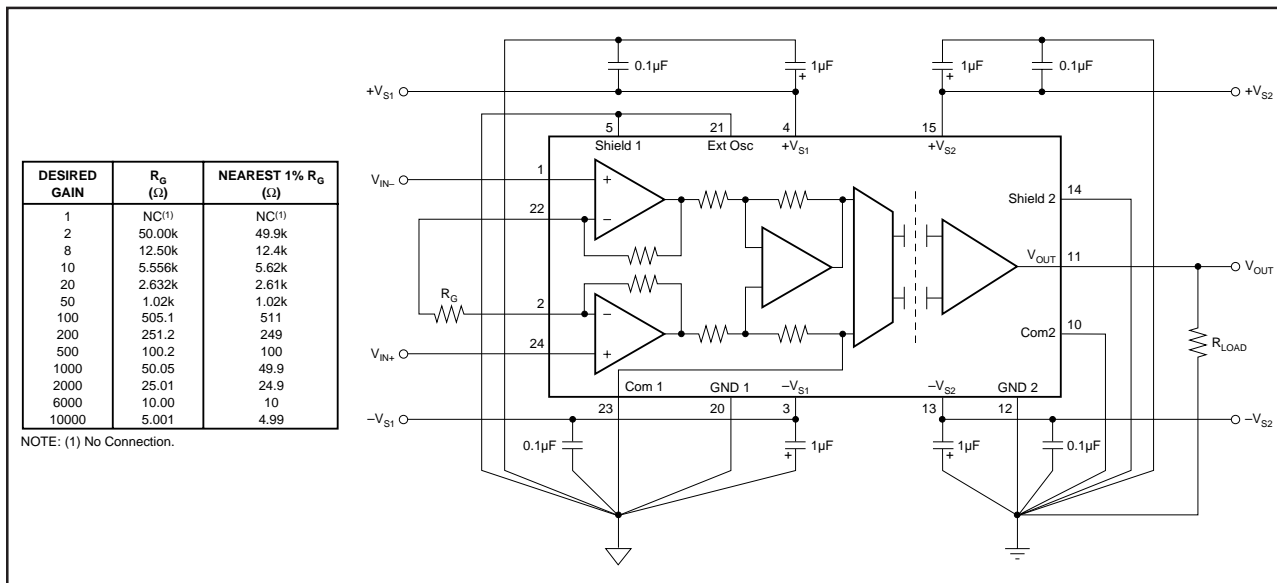


FIGURE 1. Basic Connections.

the protection circuitry limits the input current to a safe value of approximately 1.5 to 5mA. The inputs are protected even if the power supplies are disconnected or turned off.

### SYNCHRONIZED OPERATION

ISO175 can be synchronized to an external signal source. This capability is useful in eliminating troublesome beat frequencies in multichannel systems and in rejecting AC signals and their harmonics. To use this feature, an external signal must be applied to the Ext Osc pin. ISO175 can be synchronized over the 400kHz to 700kHz range.

The ideal external clock signal for the ISO175 is a  $\pm 4V$  sine wave or  $\pm 4V$ , 50% duty-cycle triangle wave. The Ext Osc pin of the ISO175 can be driven directly with a  $\pm 3V$  to  $\pm 5V$  sine or 25% to 75% duty-cycle triangle wave and the ISO amp's internal modulator/demodulator circuitry will synchronize to the signal.

ISO175 can also be synchronized to a 400kHz to 700kHz Square-Wave External Clock since an internal clamp and filter provide signal conditioning. A square-wave signal of 25% to 75% duty cycle, and  $\pm 3V$  to  $\pm 20V$  level can be used to directly drive the ISO175.

With the addition of the signal conditioning circuit shown in Figure 2, any 10% to 90% duty-cycle square-wave signal can be used to drive the ISO175 Ext Osc pin. With the values shown, the circuit can be driven by a 4Vp-p TTL signal. For a higher or lower voltage input, increase or decrease the 1k $\Omega$  resistor,  $R_X$ , proportionally, e.g. for a  $\pm 4V$  square-wave (8Vp-p)  $R_X$  should be increased to 2k $\Omega$ . The value of  $C_X$  used in the Figure 2 circuit depends on the frequency of the external clock signal.  $C_X$  should be 30pF for ISO175.

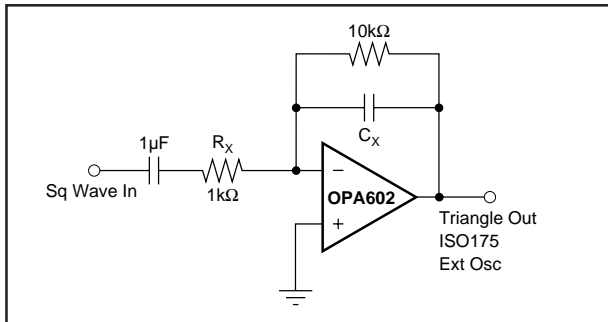


FIGURE 2. Square-Wave to Triangle Wave Signal Conditioner for Driving ISO175 Ext Osc Pin.

### CARRIER FREQUENCY CONSIDERATIONS

ISO175 amplifier transmit the signal across the ISO-barrier by a duty-cycle modulation technique. This system works like any linear amplifier for input signals having frequencies below one half the carrier frequency,  $f_C$ . For signal frequencies above  $f_C/2$ , the behavior becomes more complex. The “Signal Response vs Carrier Frequency” performance curve describes this behavior graphically. The upper curve illustrates the response for input signals varying from DC to  $f_C/2$ . At input frequencies at or above  $f_C/2$ , the device

generates an output signal component that varies in both amplitude and frequency, as shown by the lower curve. The lower horizontal scale shows the periodic variation in the frequency of the output component. Note that at the carrier frequency and its harmonics, both the frequency and amplitude of the response go to zero. These characteristics can be exploited in certain applications.

It should be noted that for the ISO175, the carrier frequency is nominally 500kHz and the  $-3dB$  point of the amplifier is 60kHz. Spurious signals at the output are not significant under these circumstances unless the input signal contains significant components above 250kHz.

When periodic noise from external sources such as system clocks and DC/DC converters are a problem, ISO175 can be used to reject this noise. The amplifier can be synchronized to an external frequency source,  $f_{EXT}$ , placing the amplifier response curve at one of the frequency and amplitude nulls indicated in the “Signal Response vs Carrier Frequency” performance curve. Figure 3 shows circuitry with opto-isolation suitable for driving the Ext Osc input from TTL levels.

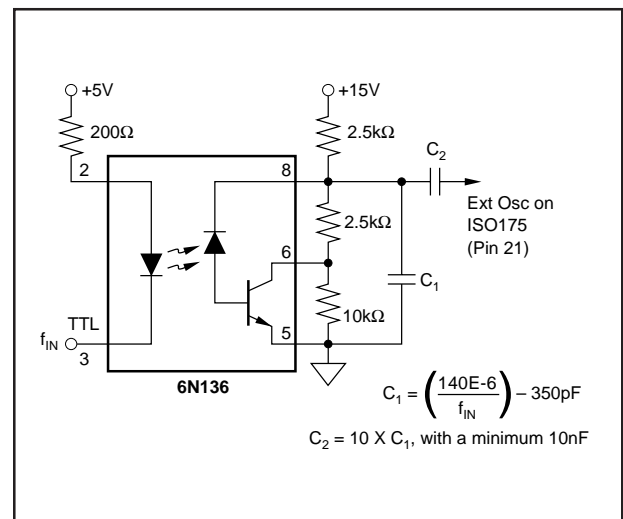


FIGURE 3. Synchronization with Isolated Drive Circuit for Ext Osc Pin.

### ISOLATION MODE VOLTAGE

Isolation Mode Voltage (IMV) is the voltage appearing between isolated grounds GND1 and GND2. The IMV can induce errors at the output as indicated by the plots of IMV versus Frequency. It should be noted that if the IMV frequency exceeds  $f_C/2$ , the output will display spurious outputs in a manner similar to that described above, and the amplifier response will be identical to that shown in the “Signal Response vs Carrier Frequency” performance curve. This occurs because IMV-induced errors behave like input-referred error signals. To predict the total IMR, divide the isolation voltage by the IMR shown in “IMR vs Frequency” performance curve and compute the amplifier response to this input-referred error signal from the data given in the “Signal Response vs Carrier Frequency” performance curve.

Due to effects of very high-frequency signals, typical IMV performance can be achieved only when  $dV/dT$  of the isolation mode voltage falls below  $1000V/\mu s$ . For convenience, this is plotted in the typical performance curve for the ISO175 as a function of voltage and frequency for sinusoidal voltages. When  $dV/dT$  exceeds  $1000V/\mu s$  but falls below  $20kV/\mu s$ , performance may be degraded. At rates of change above  $20kV/\mu s$ , the amplifier may be damaged, but the barrier retains its full integrity. Lowering the power supply voltages below  $\pm 15V$  may decrease the  $dV/dT$  to  $500V/\mu s$  for typical performance, but the maximum  $dV/dT$  of  $20kV/\mu s$  remains unchanged.

Leakage current is determined solely by the impedance of the barrier capacitance and is plotted in the "Isolation Leakage Current vs Frequency" curve.

### ISOLATION VOLTAGE RATINGS

Because a long-term test is impractical in a manufacturing situation, the generally accepted practice is to perform a production test at a higher voltage for some shorter time. The relationship between actual test voltage and the continuous derated maximum specification is an important one.

Historically, Burr-Brown has chosen a deliberately conservative one:  $V_{TEST} = (2 \times AC_{rms} \text{ continuous rating}) + 1000V$  for 10 seconds, followed by a test at rated AC<sub>rms</sub> voltage for one minute. This choice was appropriate for conditions where system transients are not well defined.

Recent improvements in high-voltage stress testing have produced a more meaningful test for determining maximum permissible voltage ratings, and Burr-Brown has chosen to apply this new technology in the manufacture and testing of the ISO175.

### PARTIAL DISCHARGE

When an insulation defect such as a void occurs within an insulation system, the defect will display localized corona or ionization during exposure to high-voltage stress. This ionization requires a higher applied voltage to start the discharge and lower voltage to maintain it or extinguish it once started. The higher start voltage is known as the inception voltage, while the extinction voltage is that level of voltage stress at which the discharge ceases. Just as the total insulation system has an inception voltage, so do the individual voids. A voltage will build up across a void until its inception voltage is reached, at which point the void will ionize, effectively shorting itself out. This action redistributes electrical charge within the dielectric and is known as partial discharge. If, as is the case with AC, the applied voltage gradient across the device continues to rise, another partial discharge cycle begins. The importance of this phenomenon is that, if the discharge does not occur, the insulation system retains its integrity. If the discharge

begins, and is allowed to continue, the action of the ions and electrons within the defect will eventually degrade any organic insulation system in which they occur. The measurement of partial discharge is still useful in rating the devices and providing quality control of the manufacturing process. The inception voltage for these voids tends to be constant, so that the measurement of total charge being redistributed within the dielectric is a very good indicator of the size of the voids and their likelihood of becoming an incipient failure. The bulk inception voltage, on the other hand, varies with the insulation system, and the number of ionization defects and directly establishes the absolute maximum voltage (transient) that can be applied across the test device before destructive partial discharge can begin. Measuring the bulk extinction voltage provides a lower, more conservative voltage from which to derive a safe continuous rating. In production, measuring at a level somewhat below the expected inception voltage and then derating by a factor related to expectations about system transients is an accepted practice.

### PARTIAL DISCHARGE TESTING

Not only does this test method provide far more qualitative information about stress-withstand levels than did previous stress tests, but it provides quantitative measurements from which quality assurance and control measures can be based. Tests similar to this test have been used by some manufacturers, such as those of high-voltage power distribution equipment, for some time, but they employed a simple measurement of RF noise to detect ionization. This method was not quantitative with regard to energy of the discharge, and was not sensitive enough for small components such as isolation amplifiers. Now, however, manufacturers of HV test equipment have developed means to quantify partial discharge. VDE in Germany, an acknowledged leader in high-voltage test standards, has developed a standard test method to apply this powerful technique. Use of partial discharge testing is an improved method for measuring the integrity of an isolation barrier.

To accommodate poorly-defined transients, the part under test is exposed to voltage that is 1.6 times the continuous-rated voltage and must display less than or equal to 5pC partial discharge level in a 100% production test.

### APPLICATIONS

The ISO175 isolation amplifier is used in three categories of applications:

- Accurate isolation of signals from high voltage ground potentials,
- Accurate isolation of signals from severe ground noise and,
- Fault protection from high voltages in analog measurements.



## **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.