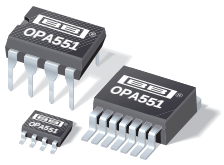


SBOS100A – JULY 1999 – REVISED OCTOBER 2003

High-Voltage, High-Current OPERATIONAL AMPLIFIERS

FEATURES

- WIDE SUPPLY RANGE: ±4V to ±30V
- HIGH OUTPUT CURRENT: 200mA Continuous
- LOW NOISE: 14nV/√Hz
- FULLY PROTECTED:
  Thermal Shutdown
  Output Current-Limited
- THERMAL SHUTDOWN INDICATOR
- WIDE OUTPUT SWING: 2V From Rail
- FAST SLEW RATE:
  OPA551: 15V/µs
  OPA552: 24V/µs
- WIDE BANDWIDTH:
  OPA551: 3MHz
  OPA552: 12MHz
- PACKAGES: DIP-8, SO-8, or DDPAK-7

APPLICATIONS

- TELEPHONY
- TEST EQUIPMENT
- AUDIO AMPLIFIERS
- TRANSDUCER EXCITATION
- SERVO DRIVERS

DESCRIPTION

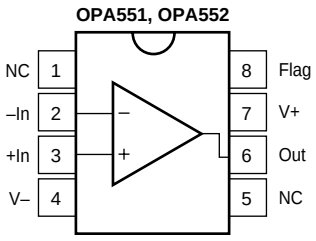
The OPA551 and OPA552 are low cost op amps with high-voltage (60V) and high-current (200mA) capability.

The OPA551 is unity-gain stable and features high slew rate (15V/µs) and wide bandwidth (3MHz). The OPA552 is optimized for gains of 5 or greater, and offers higher speed with a slew rate of 24V/µs and a bandwidth of 12MHz. Both are suitable for telephony, audio, servo, and test applications.

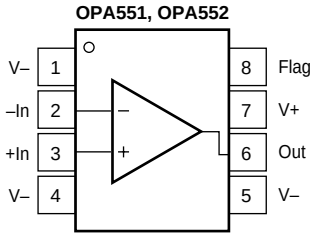
These laser-trimmed, monolithic integrated circuits provide excellent low-level accuracy along with high output swing. High performance is maintained as the amplifier swings to its specified limits.

The OPA551 and OPA552 are internally protected against over-temperature conditions and current overloads. The thermal shutdown indicator "flag" provides a current output to alert the user when thermal shutdown has occurred.

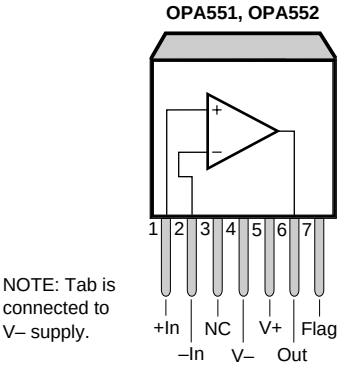
The OPA551 and OPA552 are available in DIP-8 and SO-8 packages, as well as a DDPAK-7 surface-mount plastic power package. They are specified for operation over the extended industrial temperature range, –40°C to +125°C.



DIP-8 (P)



SO-8 (U)



NOTE: Tab is connected to V– supply.

DDPAK-7 Surface-Mount (F)

SPECIFICATIONS: $V_S = \pm 30V$

OPA551

At T_J = +25°C[1], R_L = 3kΩ connected to ground and V_{OUT} = 0V, unless otherwise noted.
Boldface limits apply over the specified junction temperature range, T_J = –40°C to +125°C.

PARAMETER		CONDITION	OPA551UA, PA, FA MIN	TYP	MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_{CM} = 0V, I_O = 0		±1	±3	mV
T_J = –40°C to +125°C					**±5**	mV
vs Temperature	**dV_{OS}/dT**			**±7**		µV/°C
vs Power Supply	PSRR	V_S = ±4V to ±30V, V_{CM} = 0V		10	30	µV/V
INPUT BIAS CURRENT						
Input Bias Current	I_B			±20	±100	pA
Input Offset Current	I_{OS}			±3	±100	pA
NOISE						
Input Voltage Noise Density, f = 1kHz	e_n			14		$nV/\sqrt{Hz}$
Current Noise Density, f = 1kHz	i_n			3.5		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V–) + 2.5		(V+) – 2.5	V
Common-Mode Rejection Ratio	CMRR	–27.5V < V_{CM} < +27.5V	92	102		dB
INPUT IMPEDANCE						
Differential				10^{13} || 2		Ω || pF
Common-Mode				10^{13} || 6		Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	R_L = 3kΩ, –28V < V_O < +28V	110	126		dB
T_J = –40°C to +125°C		**R_L = 3kΩ, –28V < V_O < +28V**	**100**			dB
		R_L = 300Ω, –27V < V_O < +27V		120		dB
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW			3		MHz
Slew Rate	SR	G = 1		±15		V/µs
Settling Time: 0.1%		G = 1, C_L = 100pF, 10V Step		1.3		µs
0.01%		G = 1, C_L = 100pF, 10V Step		2		µs
Total Harmonic Distortion + Noise, f = 1kHz	THD+N	V_O = 15Vrms, R_L = 3kΩ, G = 3		0.0005		%
		V_O = 15Vrms, R_L = 300Ω, G = 3		0.0005		%
Overload Recovery Time		V_{IN} • Gain = V_S		1		µs
OUTPUT						
Voltage Output	V_{OUT}	I_O = 200mA	(V–) + 3.0		(V+) – 3.0	V
T_J = –40°C to +125°C		**I_O = 200mA**	**(V–) + 3.5**		**(V+) – 3.5**	V
		I_O = 10mA	(V–) + 2.0		(V+) – 2.0	V
T_J = –40°C to +125°C		**I_O = 10mA**	**(V–) + 2.5**		**(V+) – 2.7**	V
Maximum Continuous Current Output: dc	I_O	Package Dependent—See Text	±200			mA
Short-Circuit Current	I_{SC}			±380		mA
Capacitive Load Drive	C_{LOAD}	Stable Operation		See Typical Curve		
SHUTDOWN FLAG						
Thermal Shutdown Status Output						
Normal Operation		Sourcing		0.05	1	µA
Thermally Shutdown		Sourcing	80	120	160	µA
Voltage Compliance Range			V–		(V+) – 1.5	V
Junction Temperature						
Shutdown				160		°C
Reset from Shutdown				140		°C
POWER SUPPLY						
Specified Voltage	V_S			±30		V
Operating Voltage Range			±4		±30	V
Quiescent Current	I_Q	I_O = 0		±7	±8.5	mA
T_J = –40°C to +125°C					**±10**	mA
TEMPERATURE RANGE						
Specified Range	T_J		–40		+125	°C
Operating Range	T_J		–55		+125	°C
Storage Range	T_A		–65		+150	°C
Thermal Resistance						
SO-8 Surface Mount	θ_{JA}			90		°C/W
DIP-8	θ_{JA}			100		°C/W
DDPak-7	θ_{JA}			65		°C/W
DDPak-7	θ_{JC}			3		°C/W

NOTES: (1) All tests are high-speed tested at +25°C ambient temperature. Effective junction temperature is +25°C unless otherwise noted.

SPECIFICATIONS: $V_S = \pm 30V$

OPA552

At T_J = +25°C[1], R_L = 3kΩ connected to Ground and V_{OUT} = 0V, unless otherwise noted.
Boldface limits apply over the specified junciton temperature range, T_J = –40°C to +125°C.

PARAMETER		CONDITION	OPA552UA, PA, FA			UNITS
			MIN	TYP	MAX	
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_{CM} = 0V, I_O = 0		±1	±3	mV
T_J = –40°C to +125°C					**±5**	mV
vs Temperature	**dV_{OS}/dT**			**±7**		µV/°C
vs Power Supply	PSRR	V_S = ±4V to ±30V, V_{CM} = 0V		10	30	µV/V
INPUT BIAS CURRENT						
Input Bias Current	I_B			±20	±100	pA
Input Offset Current	I_{OS}			±3	±100	pA
NOISE						
Input Voltage Noise Density, f = 1kHz	e_n			14		nV/√Hz
Current Noise Density, f = 1kHz	i_n			3.5		fA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V–) + 2.5		(V+) – 2.5	V
Common-Mode Rejection Ratio	CMRR	–27.5V < V_{CM} < +27.5V	92	102		dB
INPUT IMPEDANCE						
Differential				10^{13} || 2		Ω || pF
Common-Mode				10^{13} || 6		Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	R_L = 3kΩ, –28V < V_O < +28V	110	126		dB
T_J = –40°C to +125°C		**R_L = 3kΩ, –28V < V_O < +28V**	**100**			dB
		R_L = 300Ω, –27V < V_O < +27V		120		dB
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW			12		MHz
Slew Rate	SR	G = 5		±24		V/µs
Settling Time: 0.1%		G = 5, C_L = 100pF, 10V Step		2.2		µs
0.01%		G = 5, C_L = 100pF, 10V Step		3		µs
Total Harmonic Distortion + Noise, f = 1kHz	THD+N	V_O = 15Vrms, R_L = 3kΩ, G = 5		0.0005		%
		V_O = 15Vrms, R_L = 300Ω, G = 5		0.0005		%
Overload Recovery Time		V_{IN} • Gain = V_S		1		µs
OUTPUT						
Voltage Output	V_{OUT}	I_O = 200mA	(V–) + 3.0		(V+) – 3.0	V
T_J = –40°C to +125°C		**I_O = 200mA**	**(V–) + 3.5**		**(V+) – 3.5**	V
		I_O = 10mA	(V–) + 2.0		(V+) – 2.0	V
T_J = –40°C to +125°C		**I_O = 10mA**	**(V–) + 2.5**		**(V+) – 2.7**	V
Maximum Continuous Current Output: dc	I_O	Package Dependent—See Text	±200			mA
Short-Circuit Current	I_{SC}			±380		mA
Capacitive Load Drive	C_{LOAD}	Stable Operation	See Typical Curve			
SHUTDOWN FLAG						
Thermal Shutdown Status Output						
Normal Operation		Sourcing		0.05	1	µA
Thermally Shutdown		Sourcing	80	120	160	µA
Voltage Compliance Range			V–		(V+) – 1.5	V
Junction Temperature						
Shutdown				160		°C
Reset from Shutdown				140		°C
POWER SUPPLY						
Specified Voltage	V_S			±30		V
Operating Voltage Range			±4		±30	V
Quiescent Current	I_Q	I_O = 0		±7	±8.5	mA
T_J = –40°C to +125°C					**±10**	mA
TEMPERATURE RANGE						
Specified Range	T_J		–40		+125	°C
Operating Range	T_J		–55		+125	°C
Storage Range	T_A		–65		+150	°C
Thermal Resistance						
SO-8 Surface Mount	θ_{JA}			90		°C/W
DIP-8	θ_{JA}			100		°C/W
DDPak-7	θ_{JA}			65		°C/W
DDPak-7	θ_{JC}			3		°C/W

NOTES: (1) All tests are high-speed tested at +25°C ambient temperature. Effective junction temperature is +25°C unless otherwise noted.

ABSOLUTE MAXIMUM RATINGS[1]

Output Current	See SOA Curve
Supply Voltage, V+ to V–	60V
Input Voltage Range	(V–) – 0.5V to (V+) + 0.5V
Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering 10s, DIP-8)	300°C
(soldering 3s, SO-8 and DDPAK)	240°C
ESD Capability (Human Body Model)	3000V

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

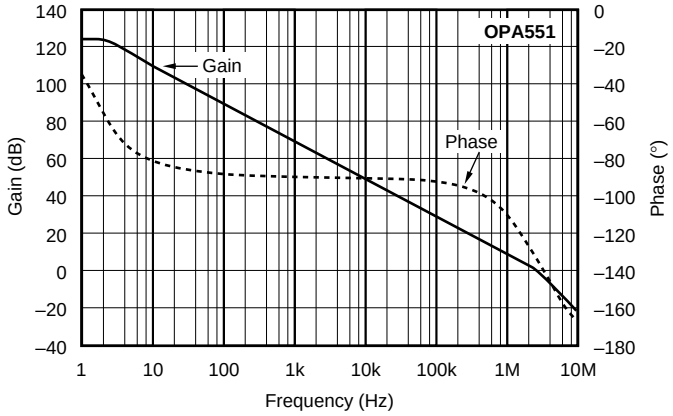
For the most current package and ordering information, see the Package Ordering Addendum at the end of this data sheet.

TYPICAL PERFORMANCE CURVES

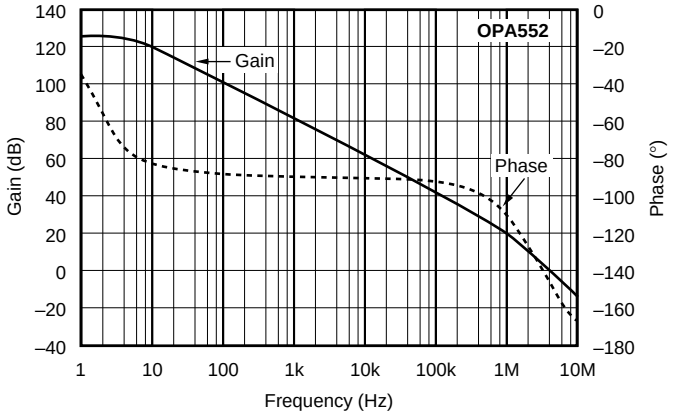
At T_J = +25°C, V_S = ±30V and R_L = 3kΩ, unless otherwise noted.

All temperatures are junction temperatures unless otherwise noted. Refer to the Applications Information section to calculate junction temperatures from ambient temperatures for a specific configuration.

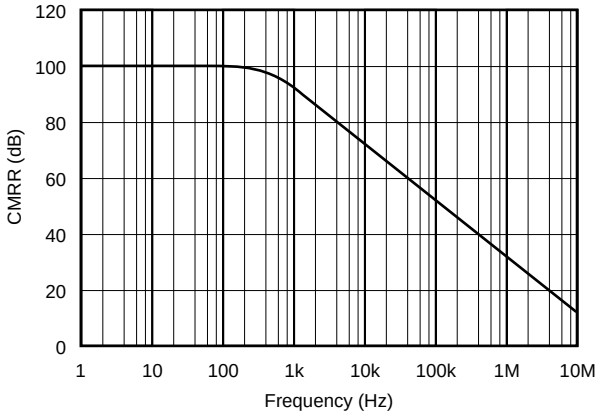
OPEN-LOOP GAIN AND PHASE vs FREQUENCY
OPA551



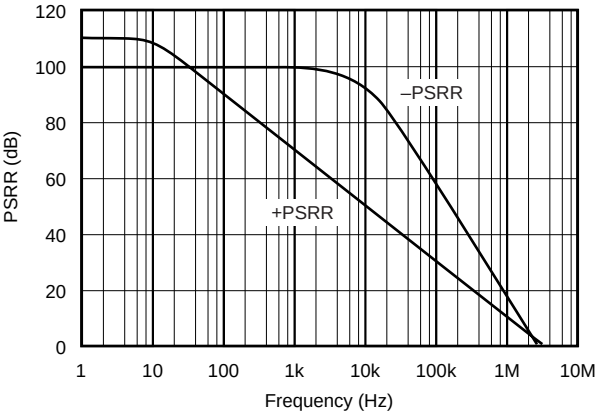
OPEN-LOOP GAIN AND PHASE vs FREQUENCY
OPA552



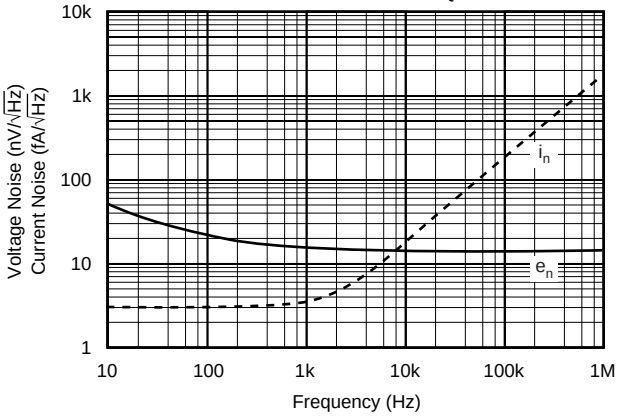
COMMON-MODE REJECTION RATIO vs FREQUENCY



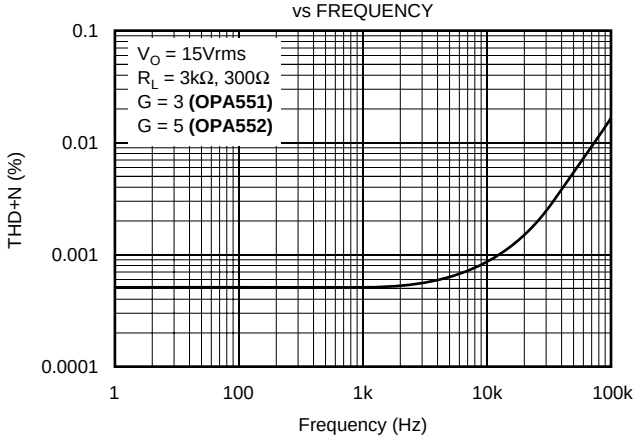
POWER SUPPLY REJECTION RATIO vs FREQUENCY



INPUT VOLTAGE AND CURRENT NOISE
SPECTRAL DENSITY vs FREQUENCY



TOTAL HARMONIC DISTORTION + NOISE
vs FREQUENCY

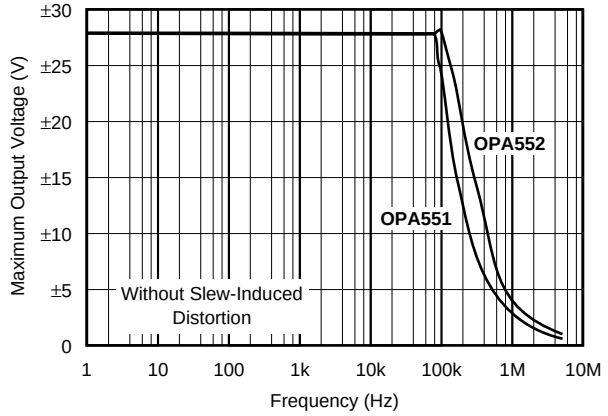


TYPICAL PERFORMANCE CURVES (Cont.)

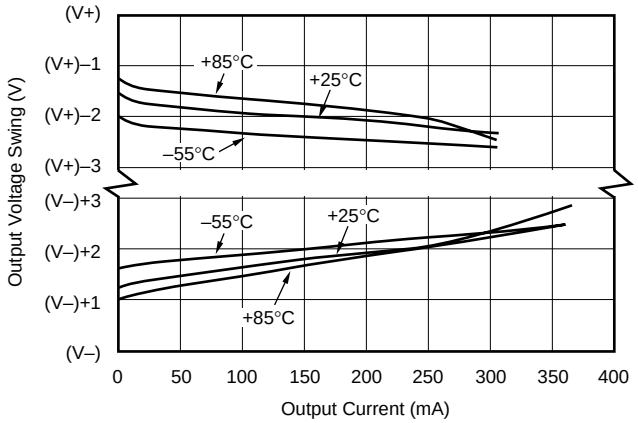
At T_J = +25°C, V_S = ±30V and R_L = 3kΩ, unless otherwise noted.

All temperatures are junction temperatures unless otherwise noted. Refer to the Applications Information section to calculate junction temperatures from ambient temperatures for a specific configuration.

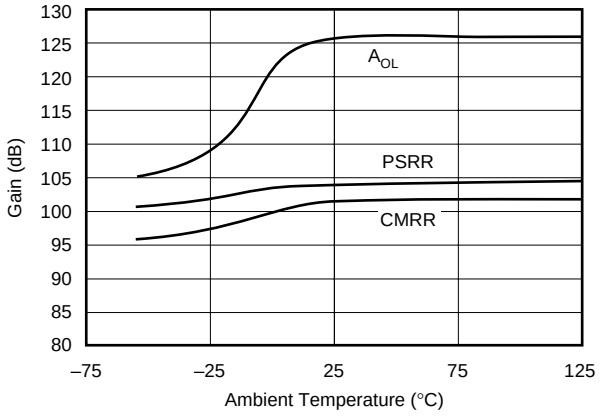
MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY



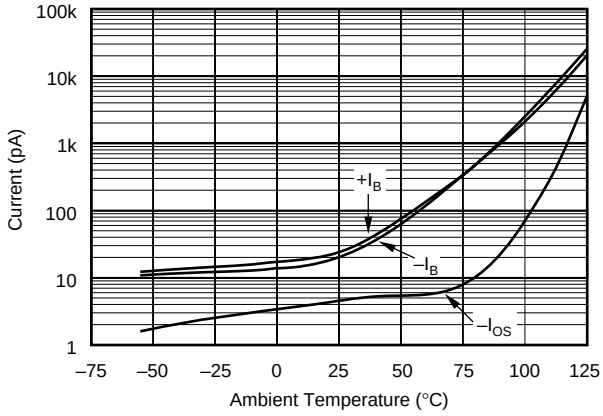
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



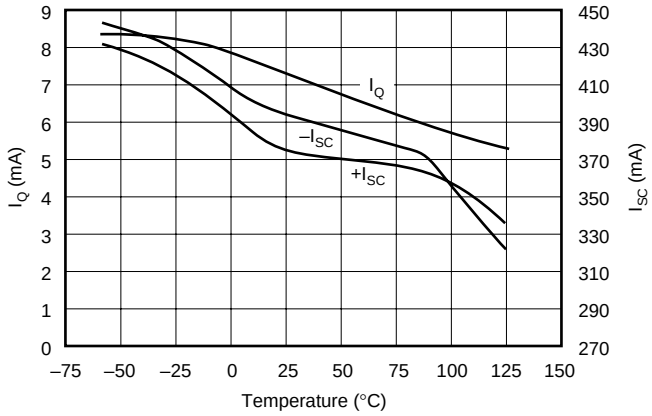
OPEN-LOOP GAIN, POWER SUPPLY REJECTION RATIO, AND COMMON-MODE REJECTION RATIO vs TEMPERATURE



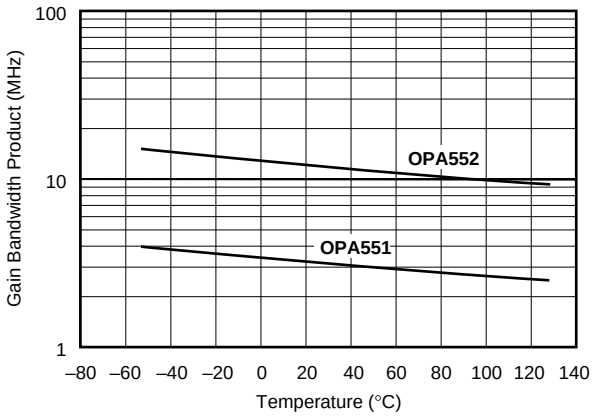
INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs TEMPERATURE



QUIESCENT CURRENT AND SHORT-CIRCUIT CURRENT vs TEMPERATURE



GAIN BANDWIDTH PRODUCT vs TEMPERATURE

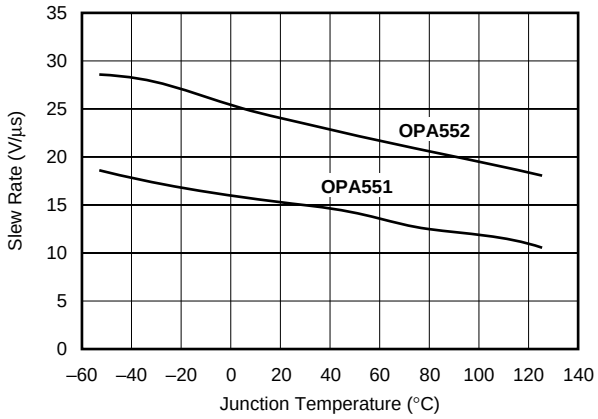


TYPICAL PERFORMANCE CURVES (Cont.)

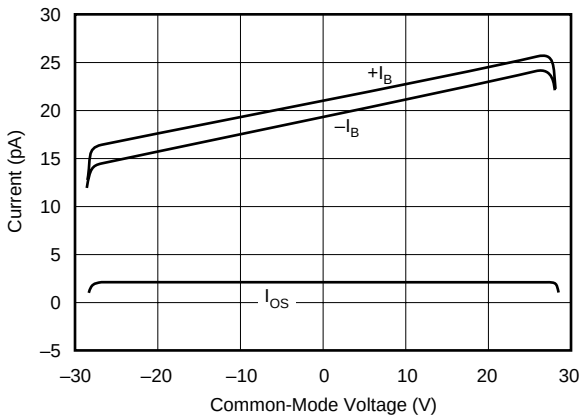
At T_J = +25°C, V_S = ±30V and R_L = 3kΩ, unless otherwise noted.

All temperatures are junction temperatures unless otherwise noted. Refer to the Applications Information section to calculate junction temperatures from ambient temperatures for a specific configuration.

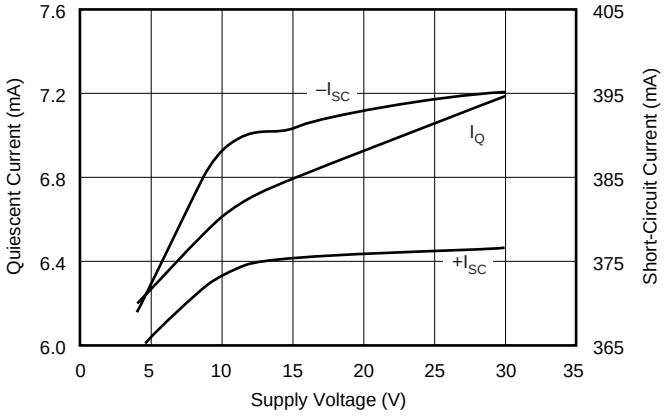
SLEW RATE vs TEMPERATURE



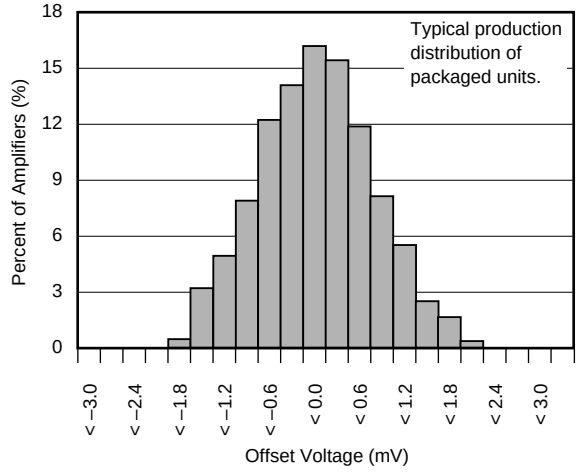
INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs COMMON-MODE VOLTAGE



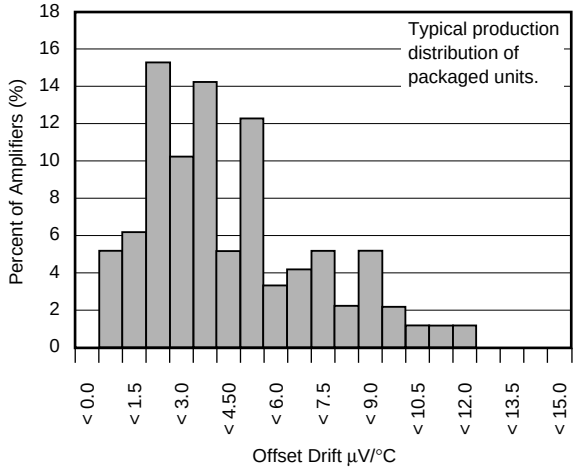
QUIESCENT CURRENT AND SHORT-CIRCUIT CURRENT vs SUPPLY VOLTAGE



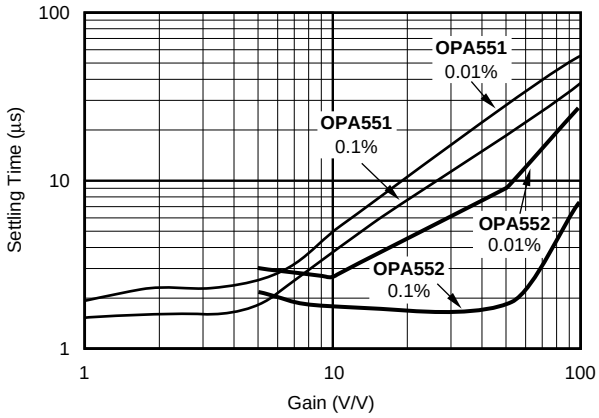
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



SETTLING TIME vs CLOSED-LOOP GAIN

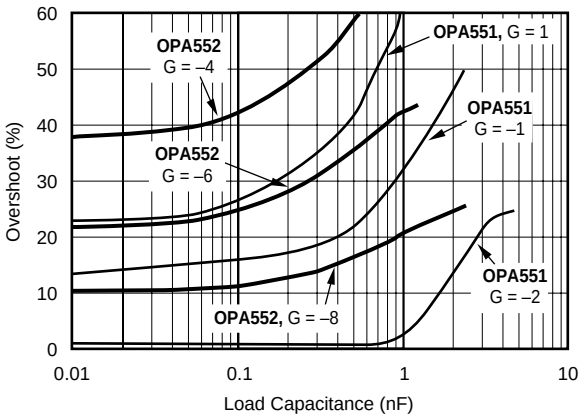


TYPICAL PERFORMANCE CURVES (Cont.)

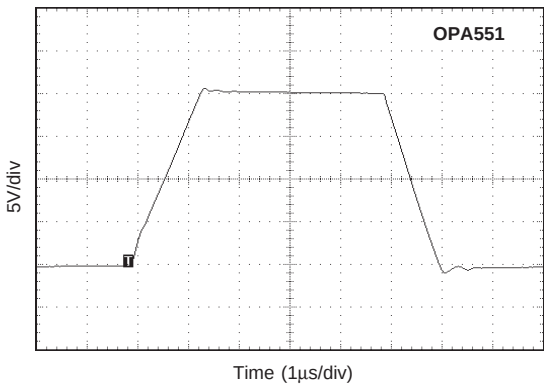
At T_J = +25°C, V_S = ±30V and R_L = 3Ω, unless otherwise noted.

All temperatures are junction temperatures unless otherwise noted. Refer to the Applications Information section to calculate junction temperatures from ambient temperatures for a specific configuration.

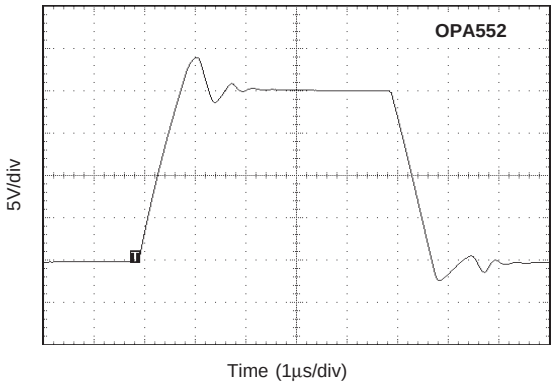
SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE



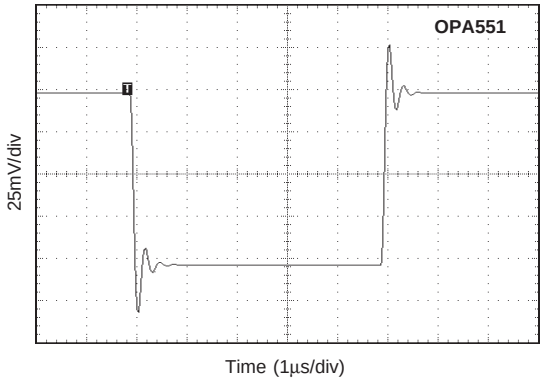
LARGE-SIGNAL STEP RESPONSE
OPA551, G = 1, C_L = 100pF



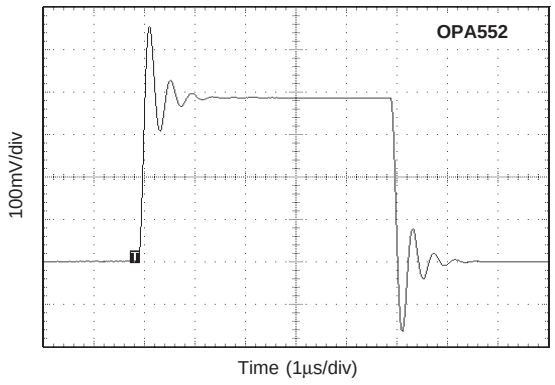
LARGE-SIGNAL STEP RESPONSE
OPA552, G = 5, C_L = 100pF



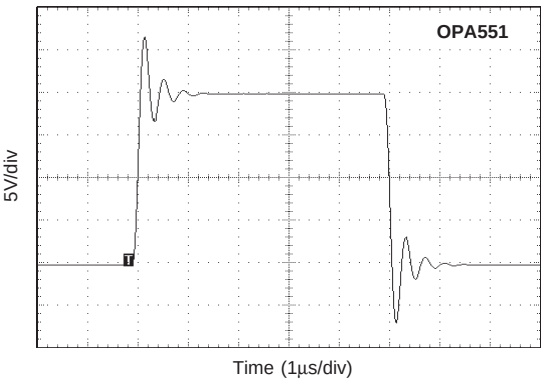
SMALL-SIGNAL STEP RESPONSE
OPA551, G = 1, C_L = 100pF



SMALL-SIGNAL STEP RESPONSE
OPA552, G = 5, C_L = 100pF



SMALL-SIGNAL STEP RESPONSE
OPA551, G = –1, C_L = 1000pF



APPLICATIONS INFORMATION

Figure 1 shows the OPA551 connected as a basic non-inverting amplifier. The OPA551 can be used in virtually any op amp configuration. OPA552 is designed for use in configurations with gains of 5 or greater. Power supply terminals should be bypassed with 0.1µF capacitors, or greater, near the power supply pins. Be sure that the capacitors are appropriately rated for the power supply voltage used. The OPA551 and OPA552 can supply output currents up to 200mA with excellent performance.

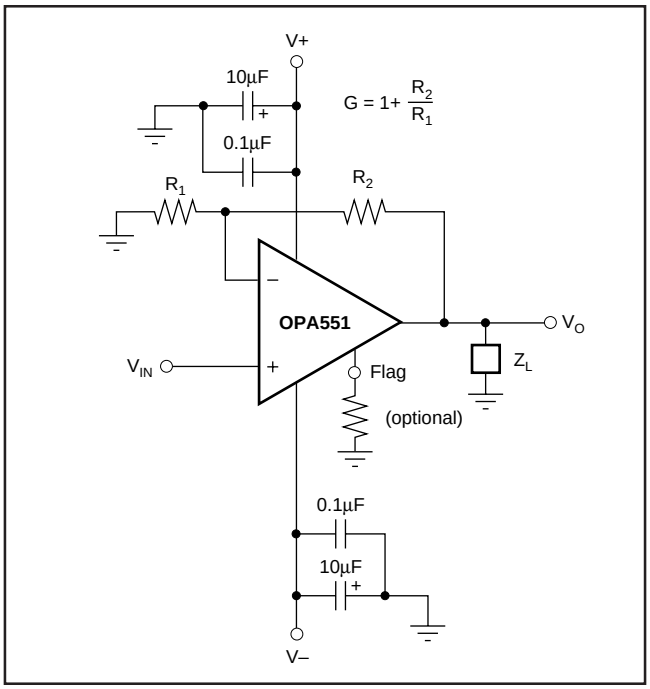


FIGURE 1. Basic Circuit Connections.

CURRENT LIMIT

The OPA551 and OPA552 are designed with internal current-limiting circuitry that limits the output current to approximately 380mA. The current limit varies with increasing junction temperature as shown in the typical curve "Current Limit vs Temperature." This, in combination with the thermal protection circuitry, provides protection from many types of overload conditions including short circuit to ground.

THERMAL PROTECTION

The OPA551 and OPA552 have thermal shutdown circuitry that protects the amplifier from damage caused by overload conditions. The thermal protection circuitry disables the output when the junction temperature reaches approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is automatically re-enabled.

The thermal shutdown function is not intended to replace proper heat sinking. Activation of the thermal shutdown circuitry is an indication of excessive power dissipation or an inadequate heat sink. Continuously running the amplifier into thermal shutdown can degrade reliability.

The Thermal Shutdown Indicator ("flag") pin can be monitored to determine if shutdown is occurring. During normal operation, the current output from the flag pin is typically 50nA. During shutdown, the current output from the flag pin increases to 120µA (typical). This current output allows for easy interfacing to external logic. See Figure 2 for two examples implementing this function.

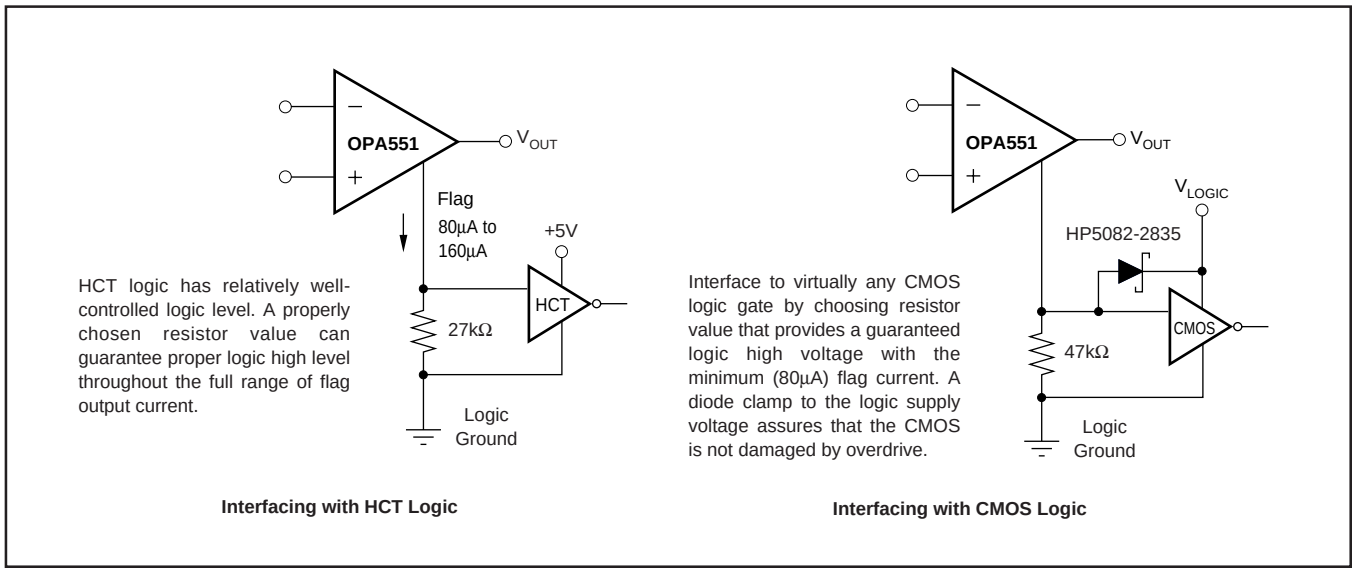


FIGURE 2. Thermal Shutdown Indicator.

POWER SUPPLIES

The OPA551 and OPA552 may be operated from power supplies of ±4V to ±30V, or a total of 60V with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. Parameters that vary significantly with operating voltage are shown in the Typical Performance Curves.

For applications that do not require symmetrical output voltage swing, power supply voltages do not need to be equal. The OPA551 and OPA552 can operate with as little as 8V between the supplies or with up to 60V between the supplies. For example, the positive supply could be set to 50V with the negative supply at –10V or vice-versa.

The SO-8 package outline shows three negative supply (V–) pins. These pins are internally connected for improved thermal performance. **Pin 4 is to be used as the primary current carrier for the negative supply. It is recommended that pins 1 and 5 not be directly connected to V– but, instead be connected to a thermal mass. DO NOT lay out the PC board to use pins 1 and 5 as feedthroughs to the negative supply. Doing so can result in a reduction of performance.**

The tab of the DDPAK-7 package is electrically connected to the negative supply (V–), however, this connection should not be used to carry current. For best thermal performance, the tab should be soldered directly to the circuit board copper area (see heat sink text).

POWER DISSIPATION

Internal power dissipation of these op amps can be quite large. Many of the specifications for the OPA551 and OPA552 are for a specified junction temperature. If the device is not subjected to internal self-heating, the junction temperature will be the same as the ambient. However, in practical applications, the device will self-heat and the junction temperature will be significantly higher than ambient. After junction temperature has been established, performance parameters that vary with junction temperature can be determined from the performance curves. The following calculation can be performed to establish junction temperature as a function of ambient temperature and the conditions of the application.

Consider the OPA551 in a circuit configuration where the load is 600Ω and the output voltage is 15V. The supplies are at ±30V and the ambient temperature (T_A) is 40°C. The θ_{JA} for the 8-pin DIP package is 100°C/W.

First, the internal heating of the op amp is as follows:

$P_{D(internal)} = I_Q \bullet V_S = 7.2mA \bullet 60V = 432mW$

The output current (I_O) can be calculated:

$$I_O = V_{OUT}/R_L = 15V/600\Omega = 25mA$$

The power being dissipated (P_D) in the output transistor of the amplifier can be calculated:

$P_{D(output\ stage)} = I_O \bullet (V_S - V_O) = 25mA \bullet (30 - 15) = 375mW$

$P_{D(total)} = P_{D(internal)} + P_{D(output\ stage)} = 432mW + 375mW = 807mW$

The resulting junction temperature can be calculated:

$$T_J = T_A + P_D\ \theta_{JA}$$

$$T_J = 40°C + 807mW \bullet 100°C/W = 120.7°C$$

Where,

T_J = junction temperature (°C)

T_A = ambient temperature (°C)

θ_{JA} = junction-to-air thermal resistance (°C/W)

For the DDPAK package, the θ_{JA} is 65°C/W with no heat sinking, resulting in a junction temperature of 92.5°C.

To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is activated. Use worst-case load and signal conditions. For good reliability, the thermal protection should trigger more than +35°C above the maximum expected ambient condition of your application. This ensures a maximum junction temperature of +125°C at the maximum expected ambient condition.

If the OPA551 or OPA552 is to be used in an application requiring more than 0.5W continuous power dissipation, it is recommended that the DDPAK package option be used. The DDPAK has superior thermal dissipation characteristics and is more easily adapted to a heat sink.

Operation from a single power supply (or unbalanced power supplies) can produce even larger power dissipation since a larger voltage can be impressed across the conducting output transistor. Consult Application Bulletin AB-039 for further information on how to calculate or measure power dissipation.

Power dissipation can be minimized by using the lowest possible supply voltage. For example, with a 200mA load, the output will swing to within 3.5V of the power supply rails. Power supplies set to no more than 3.5V above the maximum output voltage swing required by the application will minimize the power dissipation.

SAFE OPERATING AREA

The Safe Operating Area (SOA curves, Figures 3, 4, and 5) shows the permissible range of voltage and current. The curves shown represent devices soldered to a circuit board with no heat sink. The safe output current decreases as the voltage across the output transistor ($V_S - V_O$) increases. For further insight on SOA, consult Application Bulletin AB-039.

Output short circuits are a very demanding case for SOA. A short circuit to ground forces the full power supply voltage (V+ or V–) across the conducting transistor and produces a typical output current of 380mA. With ±30V

power supplies, this creates an internal dissipation of 11.4W. This far exceeds the maximum rating and is not recommended. If operation in this region is unavoidable, use the DDPAK with a heat sink.

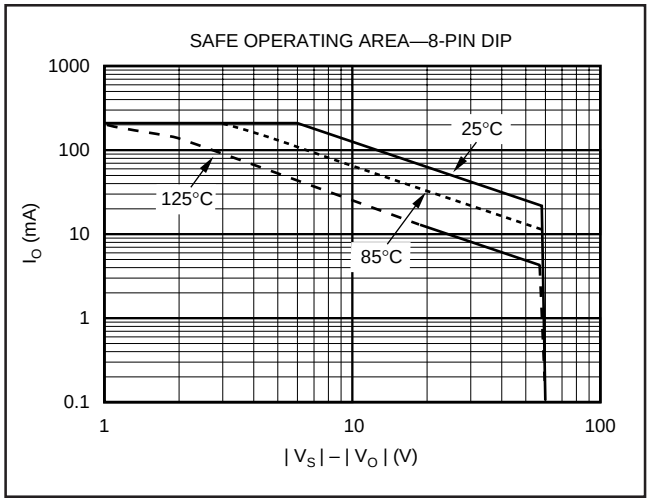


FIGURE 3. DIP-8 Safe Operating Area.

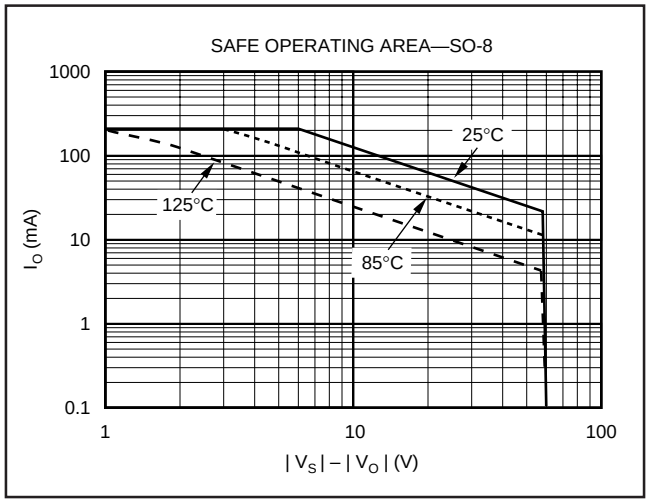


FIGURE 4. SO-8 Safe Operating Area.

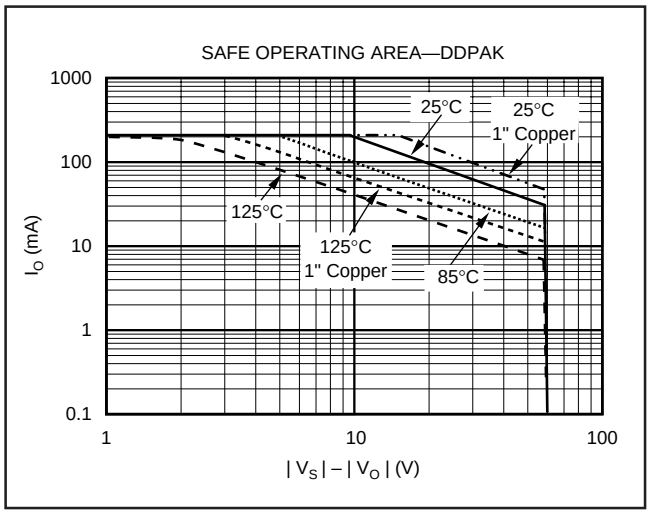


FIGURE 5. DDPAK-7 Safe Operating Area.

HEAT SINKING

Power dissipated in the OPA551 or OPA552 will cause the junction temperature to rise. For reliable operation, the junction temperature should be limited to +125°C. Many applications will require a heat sink to assure that the maximum operating junction temperature is not exceeded. The heat sink required depends on the power dissipated and on ambient conditions.

For heat sinking purposes, the tab of the DDPAK is typically soldered directly to a circuit board copper area. Increasing the copper area improves heat dissipation. Figure 6 shows typical thermal resistance from junction-to-ambient as a function of copper area.

Depending on conditions, additional heat sinking may be required. Aavid Thermal Products Inc. manufactures surface-mountable heat sinks designed specifically for use with DDPAK packages. Further information is available on Aavid's web site, www.aavid.com.

To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is activated. Use worst-case load and signal conditions. For good reliability, the thermal protection should trigger more than +25°C above the maximum expected ambient condition of your application. This produces a junction temperature of +125°C at the maximum expected ambient condition.

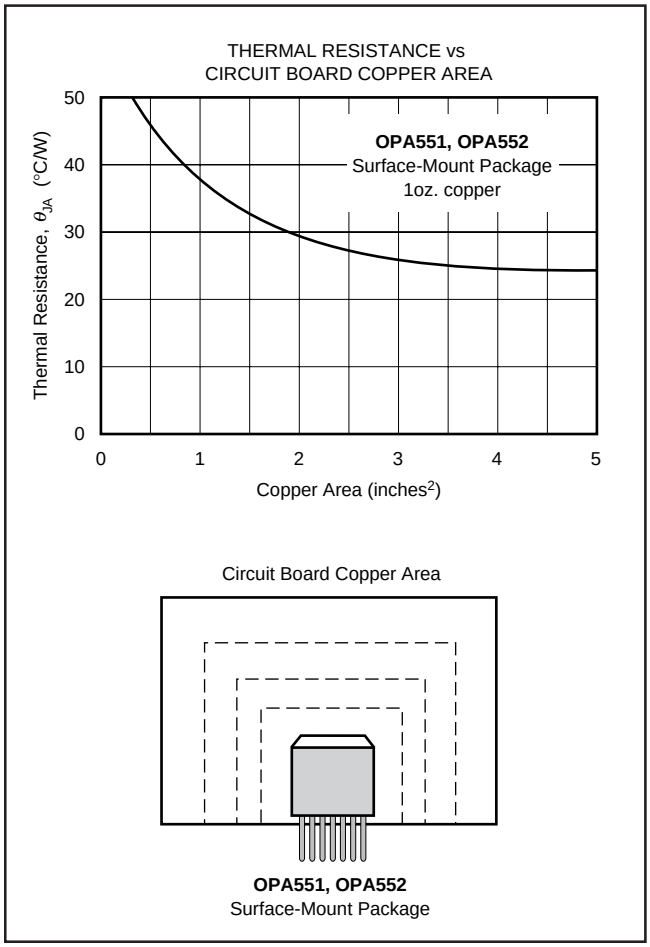


FIGURE 6. DDPAK Thermal Resistance vs Circuit Board Copper Area.

CAPACITIVE LOADS

The dynamic characteristics of the OPA551 and OPA552 have been optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and capacitive load will decrease the phase margin and may lead to gain peaking or oscillations. Figure 7 shows a circuit that preserves phase margin with capacitive load. Figure 8 shows the small-signal step response for the circuit in Figure 7. Consult Application Bulletin AB-028 for more information.

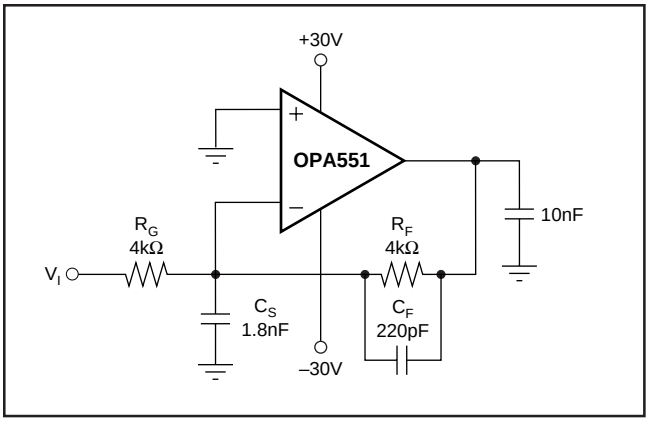


FIGURE 7. Driving Large Capacitive Loads.

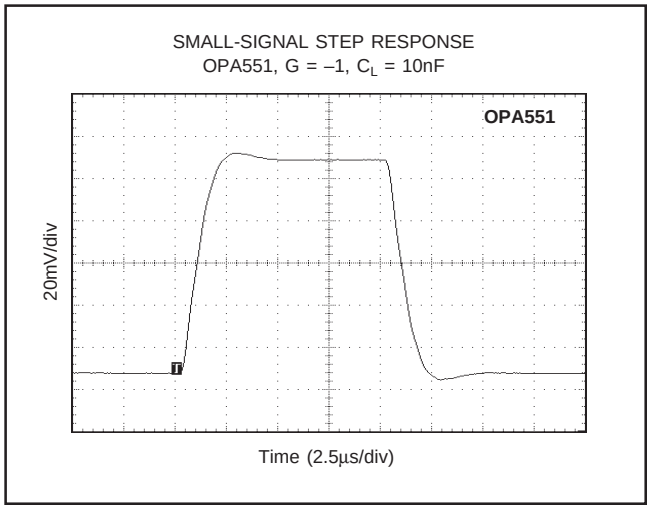


FIGURE 8. Small-Signal Step Response for Figure 7.

INCREASING OUTPUT CURRENT

In those applications where the 200mA of output current is not sufficient to drive the desired load, output current can be increased by connecting two or more OPA551s or OPA552s in parallel as shown in Figure 9. Amplifier A1 is the "master" amplifier and may be configured in virtually an op amp circuit. Amplifier A2, the "slave", is configured as a unity gain buffer. Alternatively, external output transistors can be used to boost output current. The circuit in Figure 10 is capable of supplying output currents up to 1A. Alternatively, the OPA547, OPA548, and OPA549 series power op amps should be considered for high output current drive, along with programmable current limit and output disable capability.

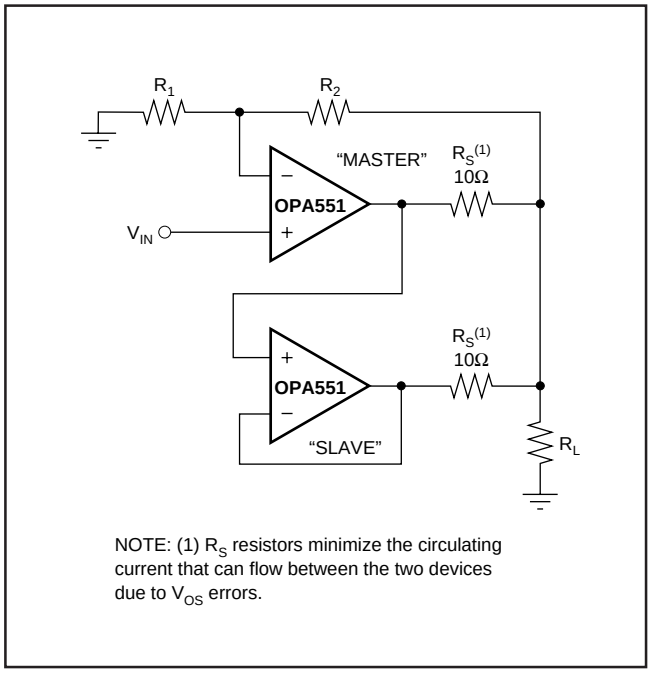


FIGURE 9. Parallel Amplifers Increase Output Current Capability.

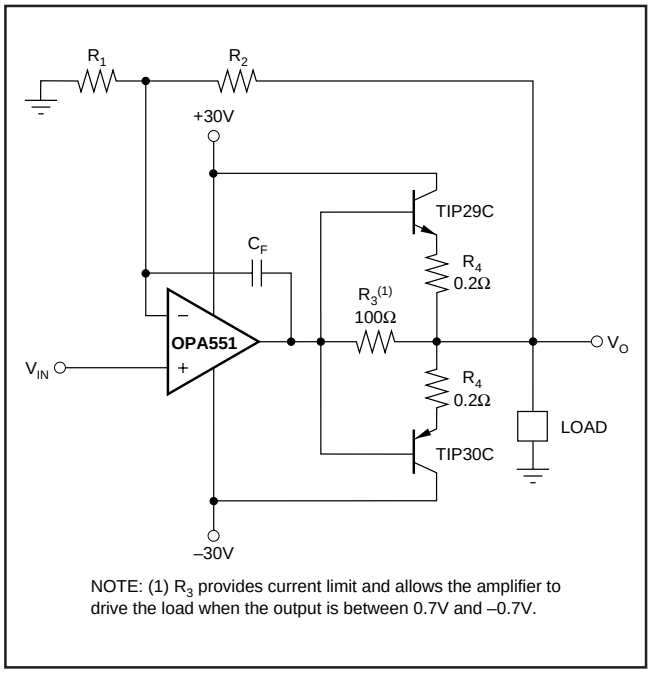


FIGURE 10. External Output Transistors Boost Output Current Up to 1 Amp.

INPUT PROTECTION

The OPA551 and OPA552 feature internal clamp diodes to protect the inputs when voltages beyond the supply rails are encountered. However, input current should be limited to 5mA. In some cases, an external series resistor may be required. Many input signals are inherently current-limtied, therefore, a limiting resistor may not be required. Please consider that a "large" series resistor, in conjunction with the input capacitance, can affect stability.

USING THE OPA552 IN LOW GAINS

The OPA552 family is intended for applications with signal gains of 5 or greater, but it is possible to take advantage of their high slew rate in lower gains using an external compensation technique in an inverting configuration. This technique maintains low noise characteristics of the OPA552 architecture at low frequencies. Depending on the application, a small increase in high frequency noise may result. This technique shapes the loop gain for good stability while giving an easily controlled second-order low-pass frequency response.

Considering only the noise gain (non-inverting signal gain) for the circuit of Figure 11, the low frequency noise gain (NG_1) will be set by the resistor ratios, while the high frequency noise gain (NG_2) will be set by the capacitor ratios. The capacitor values set both the transition frequencies and the high frequency noise gain. If this noise gain, determined by $NG_2 = 1 + C_S/C_F$, is set to a value greater than the recommended minimum stable gain for the op amp and the noise gain pole, set by $1/R_FC_F$, is placed correctly, a very well controlled, 2nd-order low-pass frequency response will result.

To choose the values for both C_S and C_F, two parameters and only three equations need to be solved. First, the target for the high frequency noise gain (NG_2) should be greater than the minimum stable gain for the OPA552. In the circuit in Figure 11, a target NG_2 of 10 is used. Second, the signal gain of –1 shown in Figure 11 sets the low frequency noise gain to $NG_1 = 1 + R_F/R_G$ (=2 in this example). Using these two gains, knowing the Gain Bandwidth Product (GBP) for the OPA552 (12MHz), and targeting a maximally flat 2nd-order, low-pass Butterworth frequency response (Q = 0.707), the key frequency in the compensation can be found.

For the values shown in Figure 11, the f_{-3dB} will be approximately 956kHz. This is less than that predicted by simply dividing the GBP by NG_1. The compensation network controls the bandwidth to a lower value while providing the full slew rate at the output and an exceptional distortion performance due to increased loop gain at frequencies below $NG_1 \bullet Z_0$. The capacitor values shown in Figure 11 are calculated for $NG_1 = 2$ and $NG_2 = 10$ with no adjustment for parasitics.

Actual circuit values can be optimized by check the small-signal step response with actual load conditions. Figure 12 shows the small-signal step response of this OPA552, G = –1 circuit with a 500pF load. It is well-behaved with no tendency to oscillate. If C_S and C_F were removed, the circuit would be unstable.

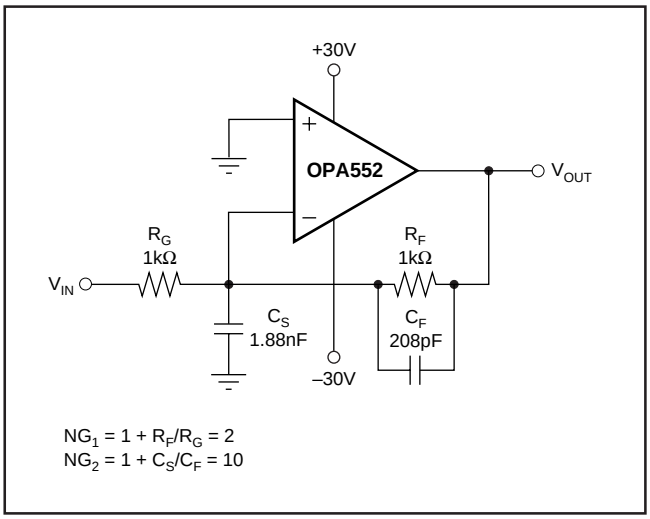


FIGURE 11. Compensation of the OPA552 for G = 1.

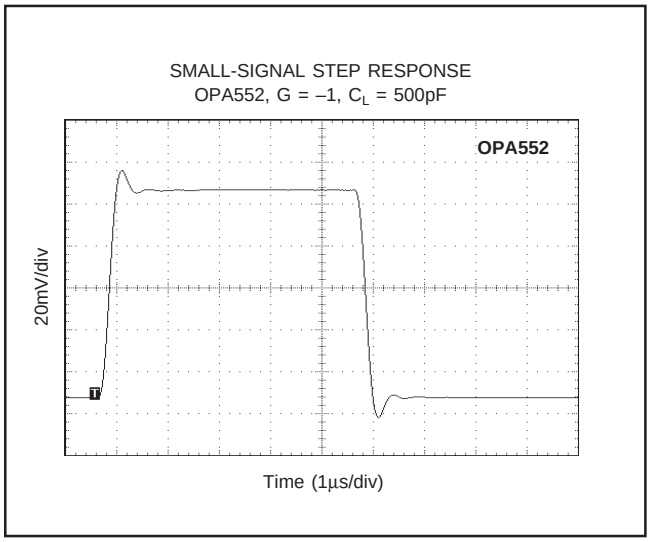


FIGURE 12. Small-Signal Step Response for Figure 11.

OFFSET VOLTAGE ERROR CALCULATION

The offset voltage (V_{OS}) of the OPA51 and OPA552 is specified with a ±30V power supply and the common-mode voltage centered between the supplies ($V_S/2$ = 0V). Additional specifications for power supply rejection and common-mode rejection are provided to allow the user to easily calculate worst-case excepted offset under the conditions of a given application.

Power Supply Rejection Ratio (PSRR) is specified in µV/V. For the OPA551 and OPA552, worst-case PSRR is 30µV/V, which means for each volt of change in total power supply voltage, the offset may shift by up to 30µV/V. Common-Mode Rejection Ratio (CMRR) is specified in dB, which can be converted to µV/V using the following equation:

$$\text{CMRR in (V/V)} = 10^{[(\text{CMRR in dB})/-20]} \quad (1)$$

For the OPA551 and OPA552, the worst-case CMRR at ±30mV supply over the full common-mode range is 96dB, or approxmately 15.8µV/V. This means that for every volt of change in common-mode, the offset may shift up to 15.8µV. These numbers can be used to calculate excursions from the specified offset voltage under different applications conditions. For example, a common application might configure the amplifier with a –48 single supply with –6V common-mode. This configuration represents a 12V variation in power supply: ±30V or 60V in the offset specification versus 48V in the application. In addition, this configuration has an 18V variation in common-mode voltage: $V_S/2$ = –24V is the specification for these power supplies, but the common-mode voltage is –6V in the application.

Calculation of the worst-case expected offset would be as follows:

$$\text{Worst-case } V_{OS} = \text{maximum specified } V_{OS} + (\text{power supply variation} \bullet \text{PSRR}) + (\text{common-mode variation} \bullet \text{CMRR}) \quad (2)$$

$$V_{OSwc} = 5\text{mV} + (12\text{V} \bullet 30\mu\text{V/V}) + (18\text{V} \bullet 15.8\mu\text{V/V}) = \pm 5.64\text{mV}$$

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
OPA551FA	OBSOLETE	DDPAK/ TO-263	KTW	7		TBD	Call TI	Call TI			
OPA551FA/500	ACTIVE	DDPAK/ TO-263	KTW	7	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		OPA551FA	Samples
OPA551FA/500G3	ACTIVE	DDPAK/ TO-263	KTW	7	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		OPA551FA	Samples
OPA551FAKTWT	ACTIVE	DDPAK/ TO-263	KTW	7	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		OPA551FA	Samples
OPA551FAKTWTG3	ACTIVE	DDPAK/ TO-263	KTW	7	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		OPA551FA	Samples
OPA551PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA551PA	Samples
OPA551PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA551PA	Samples
OPA551UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 551UA	Samples
OPA551UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 551UA	Samples
OPA551UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 551UA	Samples
OPA551UA/2K5G4	ACTIVE	SOIC	D	8		TBD	Call TI	Call TI			Samples
OPA551UAE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 551UA	Samples
OPA552FA	OBSOLETE	DDPAK/ TO-263	KTW	7		TBD	Call TI	Call TI			
OPA552FA/500	ACTIVE	DDPAK/ TO-263	KTW	7	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		OPA552FA	Samples
OPA552FA/500G3	ACTIVE	DDPAK/ TO-263	KTW	7	500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		OPA552FA	Samples
OPA552FAKTWT	ACTIVE	DDPAK/ TO-263	KTW	7	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		OPA552FA	Samples
OPA552FAKTWTG3	ACTIVE	DDPAK/ TO-263	KTW	7	50	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR		OPA552FA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
OPA552PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA552PA	Samples
OPA552PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA552PA	Samples
OPA552UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 552UA	Samples
OPA552UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 552UA	Samples
OPA552UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 552UA	Samples
OPA552UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 552UA	Samples
OPA552UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 552UA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

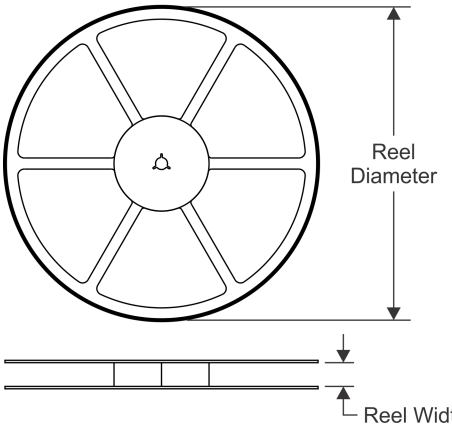
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

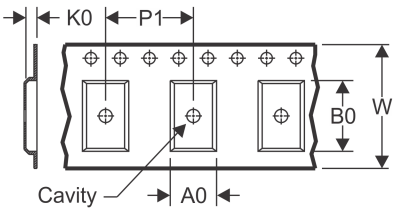
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

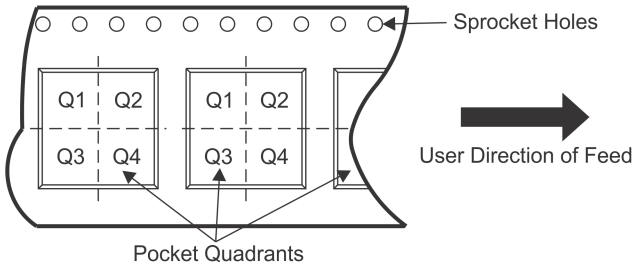


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

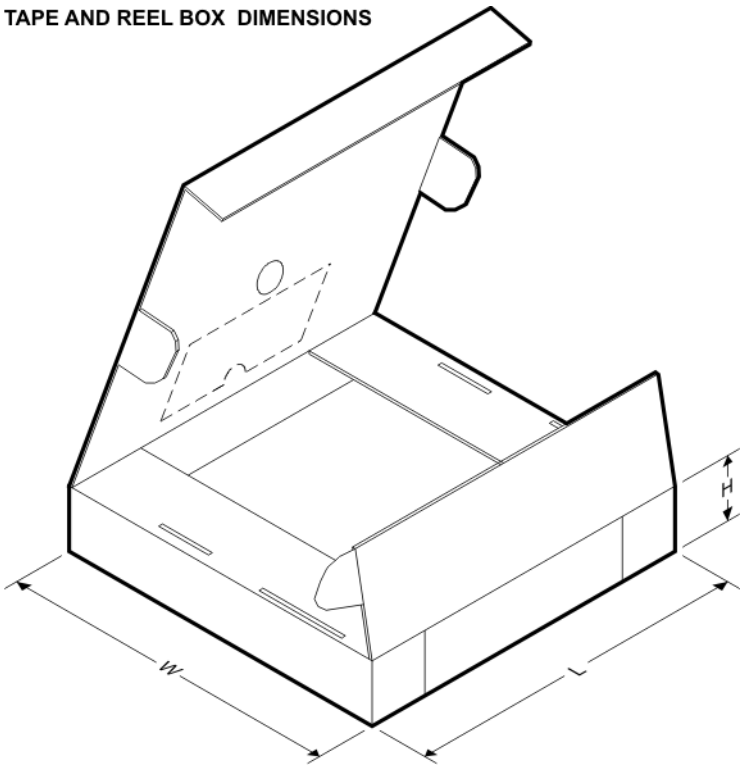
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA552FA/500	DDPAK/ TO-263	KTW	7	500	330.0	24.4	10.6	15.6	4.9	16.0	24.0	Q2
OPA552UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

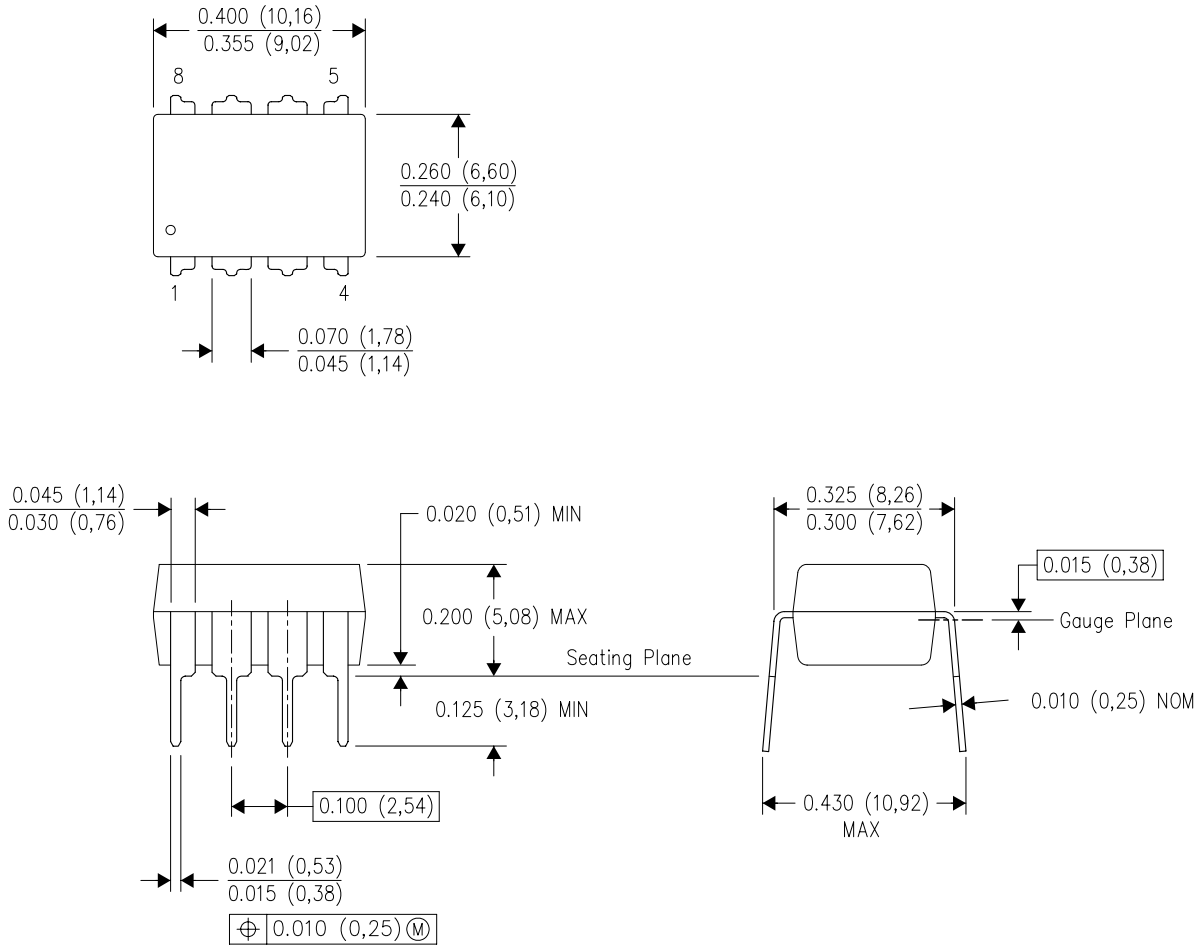
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA552FA/500	DDPAK/TO-263	KTW	7	500	367.0	367.0	45.0
OPA552UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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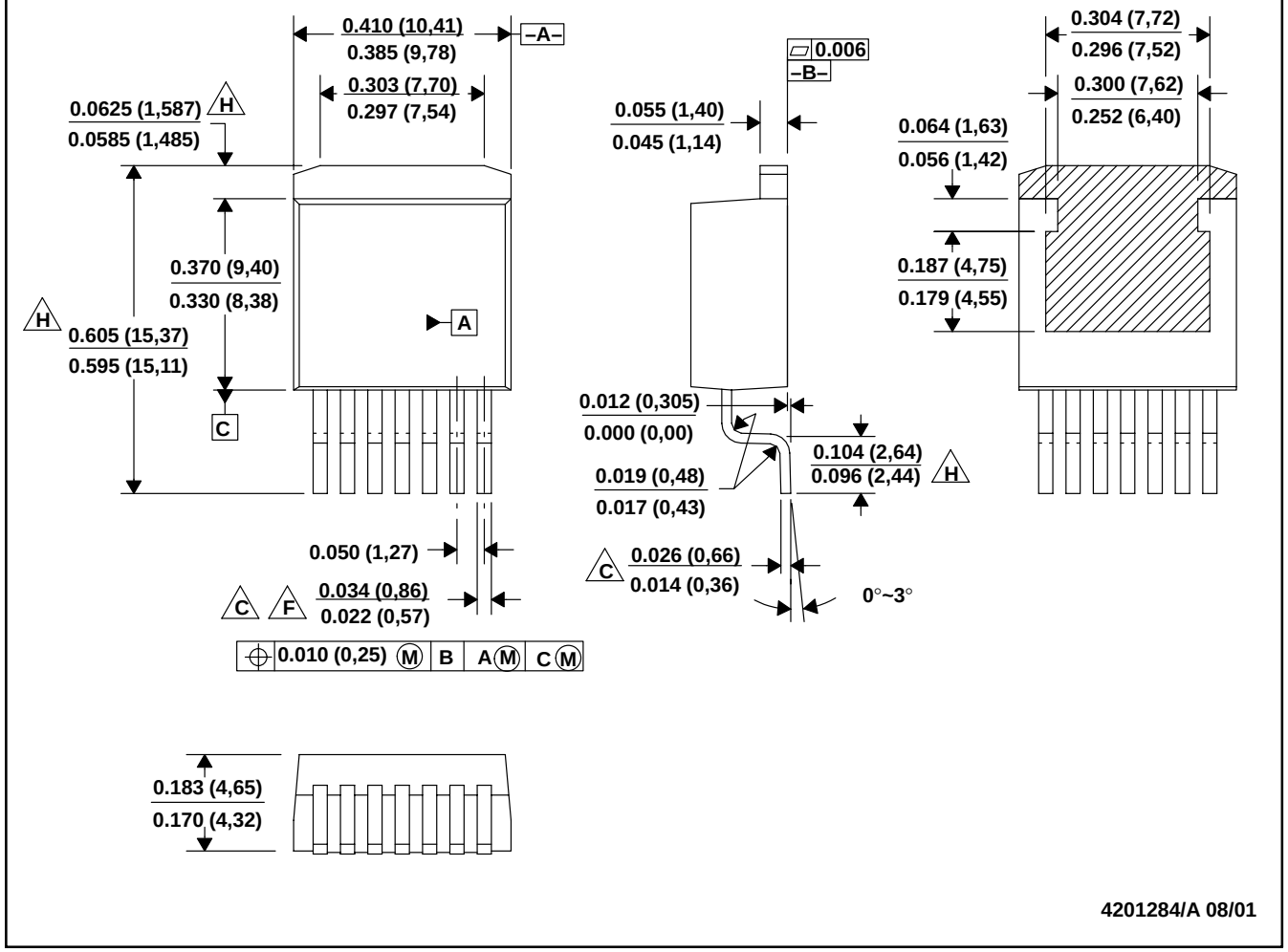
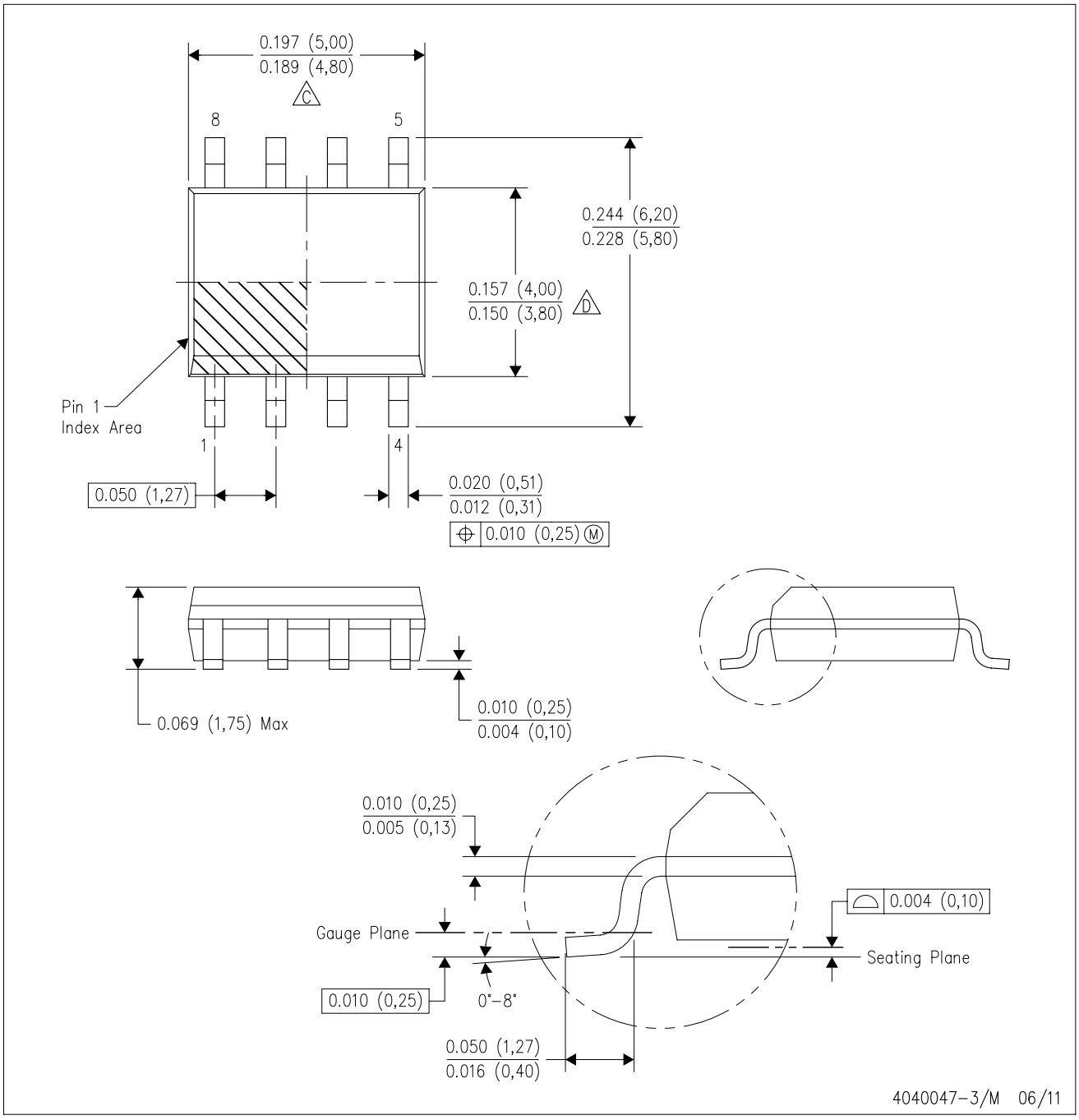
KTW (R-PSFM-G7) **PLASTIC FLANGE-MOUNT**



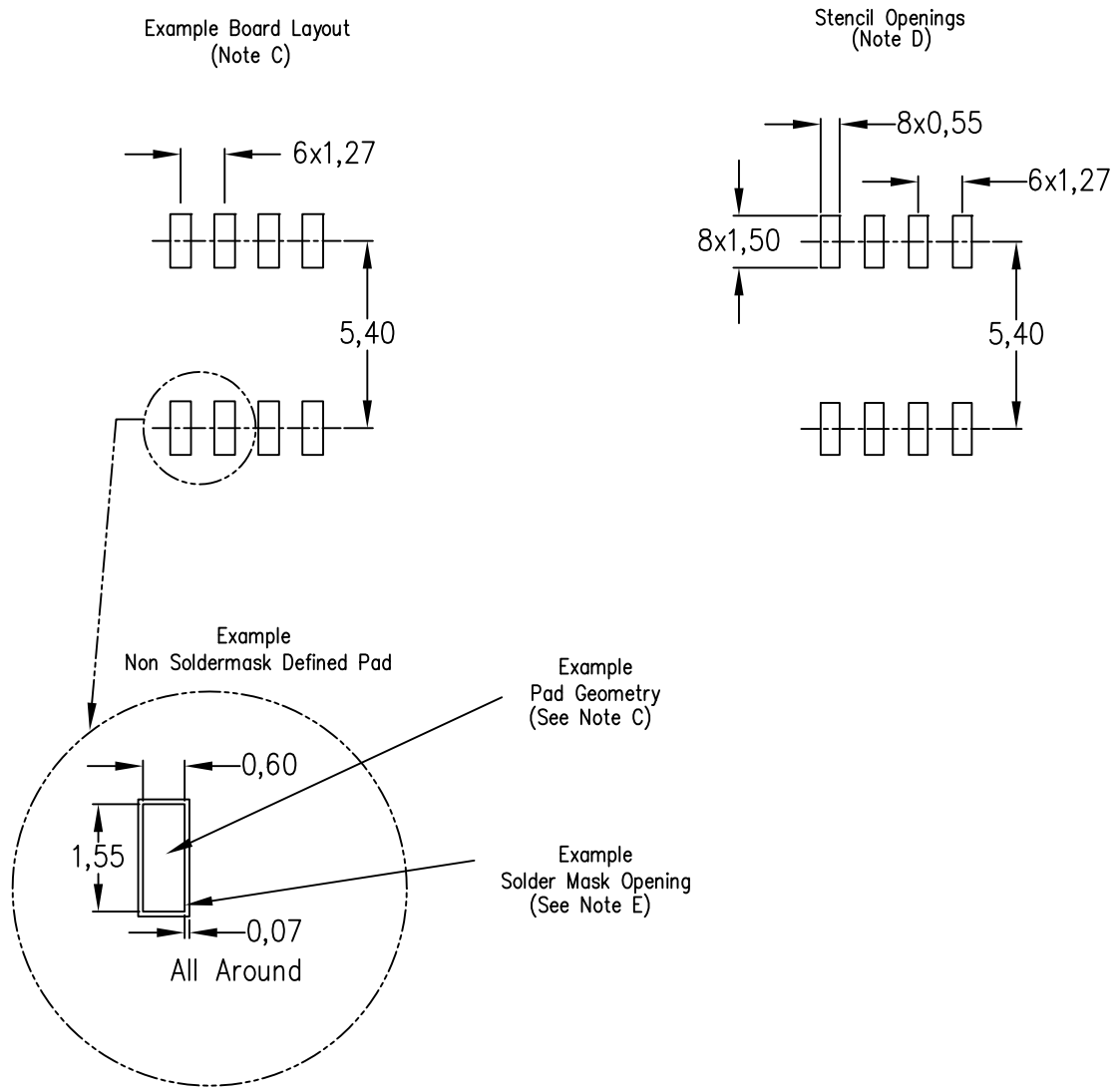
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead width and height dimensions apply to the plated lead.
D. Leads are not allowed above the Datum B.
E. Stand–off height is measured from lead tip with reference to Datum B.
F. Lead width dimension does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum dimension by more than 0.003”.
G. Cross–hatch indicates exposed metal surface.
H. Falls within JEDEC MO–169 with the exception of the dimensions indicated.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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