

INA120

Precision INSTRUMENTATION AMPLIFIER

FEATURES

- **LOW OFFSET VOLTAGE:** 25 μ V max
- **LOW OFFSET VOLTAGE DRIFT:** 0.25 μ V/ $^{\circ}$ C max
- **PIN-STRAPPED GAINS:** 1, 10, 100, 1000
- **LOW GAIN DRIFT:** 30ppm/ $^{\circ}$ C max at G = 100
- **HIGH COMMON-MODE REJECTION:** 106dB at 60Hz, G = 100

APPLICATIONS

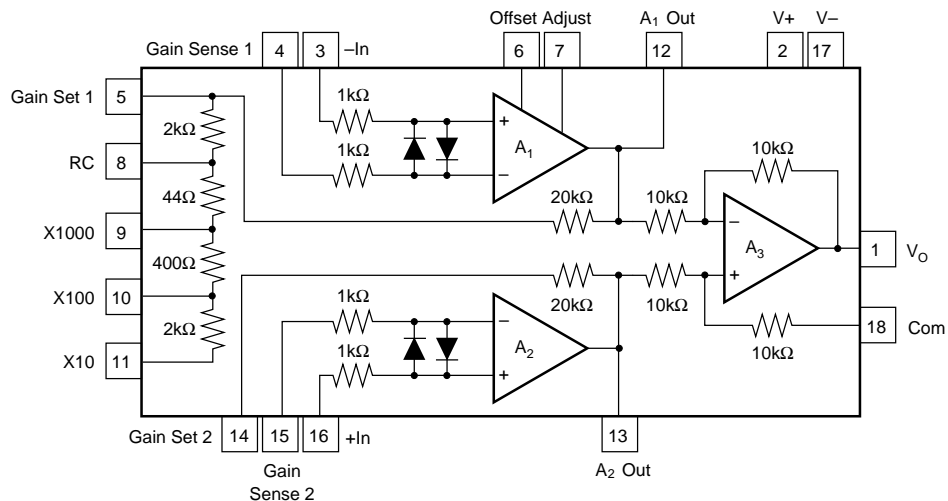
- **BRIDGE AMPLIFIER**
- **THERMOCOUPLE AMPLIFIER**
- **RTD SENSOR AMPLIFIER**
- **MEDICAL INSTRUMENTATION**
- **DATA ACQUISITION SYSTEM**
- **SWITCHED-GAIN AMPLIFIER**

DESCRIPTION

The INA120 is a precision instrumentation amplifier ideal for accurate signal acquisition. It combines precision, protected-input operational amplifiers, laser-trimmed gain-setting resistors, and a high common-mode rejection difference amplifier on a single chip.

Simple pin-strapped connections set precise gains of 1, 10, 100 or 1000. External resistors can be used to set any gain from one to 5000. Gains can be digitally selected with an external multiplexer. Gain-sense connections on the INA120 maintain accuracy when using multiplexer or gain-switching circuitry. Low power dissipation and careful on-chip thermal management reduce warm-up drift and assure excellent long-term stability.

The INA120 is available in both plastic and ceramic 18-pin DIP packages, specified for the industrial temperature range.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

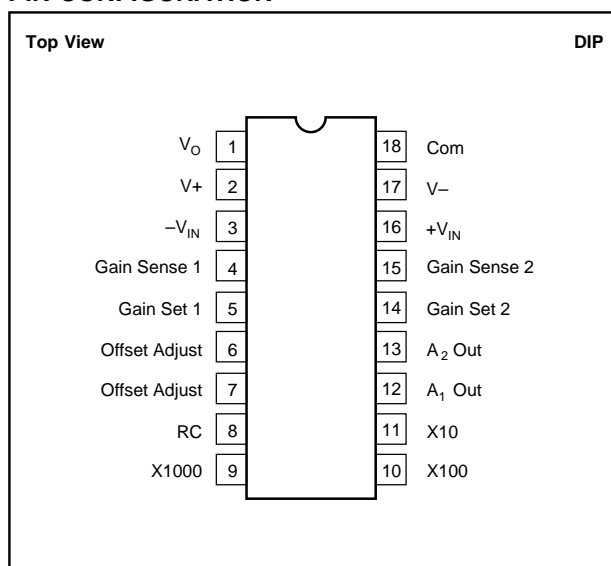
SPECIFICATIONS

At $T_A = +25^\circ\text{C}$ and $V_S = \pm 15\text{V}$ unless otherwise specified.

PARAMETER	CONDITIONS	INA120CG			INA120BG, BP			INA120AP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
GAIN		1		1000	1		1000	1		1000	V/V
Range of Gain		$1 + (2R_f/R_g)$			$1 + (2R_f/R_g)$			$1 + (2R_f/R_g)$			V/V
Gain Equation		$1 + (2R_f/R_g)$			$1 + (2R_f/R_g)$			$1 + (2R_f/R_g)$			%
Gain Error	G = 1	0.01	0.05		0.01	0.05		0.02	0.1		%
	G = 10	0.05	0.1		0.05	0.2		0.1	0.2		%
	G = 100	0.1	0.2		0.1	0.3		0.2	0.5		%
	G = 1000	0.3	0.5		0.3	1		0.5	1		%
Gain Temp Coefficient	G = 1	4	10		4	20		6	20		ppm/°C
	G = 10	4	10		4	20		8	40		ppm/°C
	G = 100	6	30		6	40		10	60		ppm/°C
	G = 1000	22	50		22	50		40	100		ppm/°C
Nonlinearity	G = 1	0.001	0.005		0.001	0.01		0.001	0.01		% of FS
	G = 10	0.002	0.005		0.002	0.01		0.002	0.01		% of FS
	G = 100	0.004	0.01		0.004	0.02		0.004	0.02		% of FS
	G = 1000	0.008	0.05		0.008	0.1		0.008	0.1		% of FS
OFFSET VOLTAGE											
Initial Offset			(10+ 300/G)	(25+ 600/G)		(50+ 300/G)	(100+ 1000/G)		(50+ 600/G)	(200+ 2000/G)	μV
vs Temperature			$(.25 + 10/G)$			$(1 + 20/G)$			$(2 + 20/G)$		$\mu\text{V}/^\circ\text{C}$
vs Power Supply	$V_S = \pm 6\text{V}$ to $\pm 18\text{V}$		$(1 + 20/G)(10 + 150/G)$			$(1 + 20/G)(20 + 250/G)$			$(1 + 20/G)(40 + 300/G)$		$\mu\text{V}/\text{V}$
INPUT BIAS CURRENT											
Initial Bias Current			± 7	± 20		± 7	± 20		± 20	± 50	nA
vs Temperature			± 0.2			± 0.2			± 0.2		nA/°C
Initial Offset Current			± 5	± 10		± 5	± 20		± 10	± 50	nA
vs Temperature			± 0.2			± 0.2			± 0.2		nA/°C
Impedance: Differential			$10^{10} \parallel 3$			$10^{10} \parallel 3$			$10^{10} \parallel 3$		$\Omega \parallel \text{pF}$
Common-Mode			$10^{10} \parallel 3$			$10^{10} \parallel 3$			$10^{10} \parallel 3$		$\Omega \parallel \text{pF}$
INPUT VOLTAGE RANGE											
Range, Linear Response		± 10	± 12.5		± 10	± 12.5		± 10	± 12.5		V
CMRR (DC, 1k Ω Source Imbalance)	G = 1	80	90		74	90		70	85		dB
	G = 10	96	106		90	106		86	95		dB
	G = 100	106	110		106	110		100	105		dB
	G = 1000	106	110		106	110		100	105		dB
NOISE											
Input Voltage Noise											$\mu\text{V p-p}$
$f_B = 0.1\text{Hz}$ to 10Hz	G = 1000		0.7			0.7			0.7		nV/ $\sqrt{\text{Hz}}$
Density; $f = 10\text{Hz}$	G = 1000		14			14			14		nV/ $\sqrt{\text{Hz}}$
$f = 100\text{Hz}$			11			11			11		nV/ $\sqrt{\text{Hz}}$
$f = 1000\text{Hz}$			10			10			10		nV/ $\sqrt{\text{Hz}}$
Input Current Noise											pAp-p
$f_B = 0.1\text{Hz}$ to 10Hz			50			50			50		pA/ $\sqrt{\text{Hz}}$
Density; $f = 10\text{Hz}$			1.8			1.8			1.8		pA/ $\sqrt{\text{Hz}}$
$f = 1\text{kHz}$			0.4			0.4			0.4		pA/ $\sqrt{\text{Hz}}$
Output Voltage Noise											$\mu\text{V p-p}$
$f_B = 0.1\text{Hz}$ to 10Hz			8			8			8		$\mu\text{V p-p}$
DYNAMIC RESPONSE											
Small Signal Bandwidth (-3dB)	G = 1		2			2			2		MHz
	G = 10		200			200			200		kHz
	G = 100		20			20			20		kHz
	G = 1000		2			2			2		kHz
Slew Rate		0.4	0.6		0.4	0.6		0.4	0.6		V/ μs
Settling Time to 0.01%	G = 1		24			24			24		μs
	G = 10		30			30			30		μs
	G = 100		50			50			50		μs
	G = 1000		200			200			200		μs
Full Power Bandwidth, $G < 200$	$V_O = \pm 10\text{V}$, $R_L = 2\text{k}\Omega$		9			9			9		kHz
Overload Recovery	50% Overdrive		2			2			2		μs
OUTPUT											
Voltage, $R_L = 2\text{k}\Omega$	Over Temperature	± 10.5	± 12.8		± 10.5	± 12.8		± 10.5	± 12.8		V
Current	Over Temperature	5	15		5	15		5	15		mA
Short-Circuit Current			24			24			24		mA
Capacitive Load, Stable Operation			4000			4000			4000		pF
POWER SUPPLY											
Rated Voltage			± 15			± 15			± 15		V
Voltage Range		± 6			± 6			± 6			V
Supply Current	$V_O = 0\text{V}$		± 2.7			± 2.7			± 2.7		mA
TEMPERATURE RANGE											
Specification		-25		+85	-25		+85	-25		+85	°C
Operation BP,AP					-40		+85	-40		+85	°C
Operation CG,BG		-55		+125	-55		+125	-55		+125	°C
Storage		-65		+150	-65		+150	-65		+150	°C

See Absolute Maximum Table.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	$\pm 18V$
Input Voltage Range	$(V+) +2$ to $(V-) -2V$
Differential Input Voltage	Total $V_s +4V$
Operating Temperature	
Ceramic G Package	$-65^\circ C$ to $+150^\circ C$
Plastic P Package	$-40^\circ C$ to $+125^\circ C$
Storage Temperature	
Ceramic G Package	$-65^\circ C$ to $+150^\circ C$
Plastic P Package	$-40^\circ C$ to $+125^\circ C$
Junction Temperature	
Ceramic G Package	$+175^\circ C$
Plastic P Package	$+125^\circ C$
Lead Temperature (soldering, 10s)	$+300^\circ C$

PACKAGE INFORMATION⁽¹⁾

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
INA120AP	18-Pin Plastic DIP	218
INA120BP	18-Pin Plastic DIP	218
INA120BG	18-Pin Ceramic DIP	158
INA120CG	18-Pin Ceramic DIP	158

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

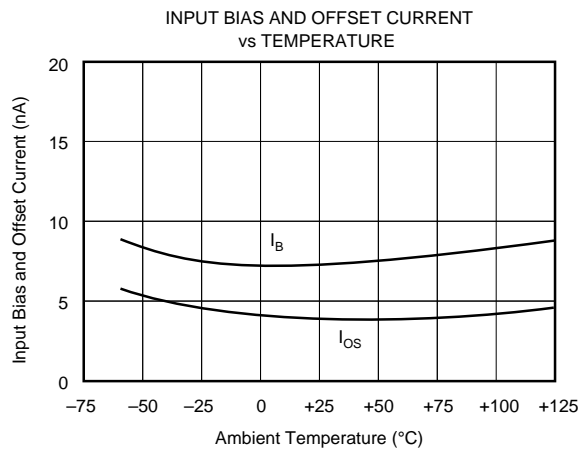
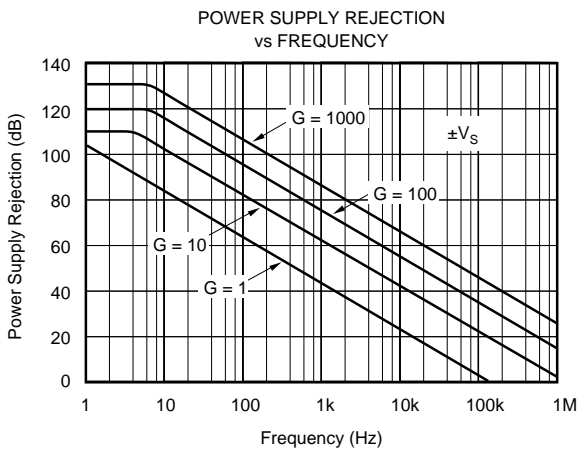
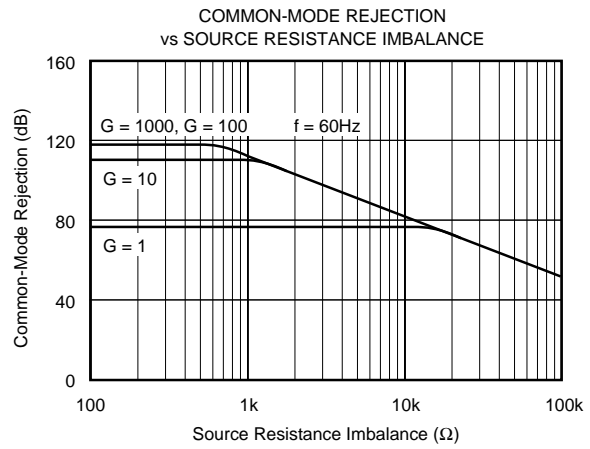
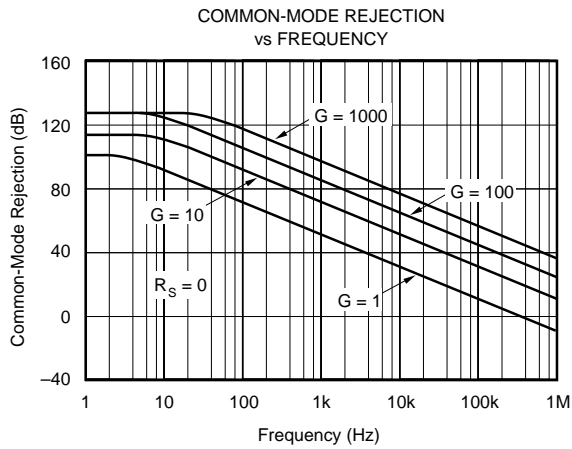
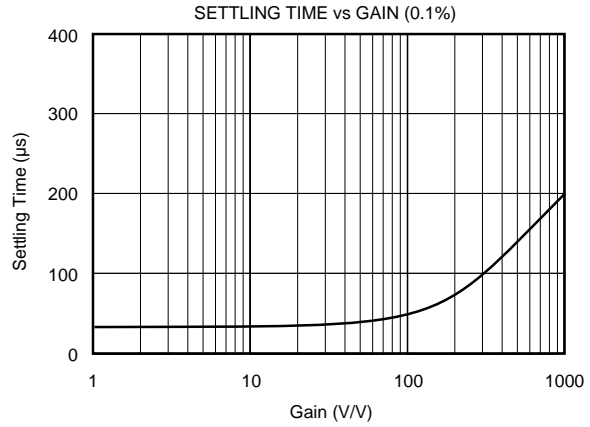
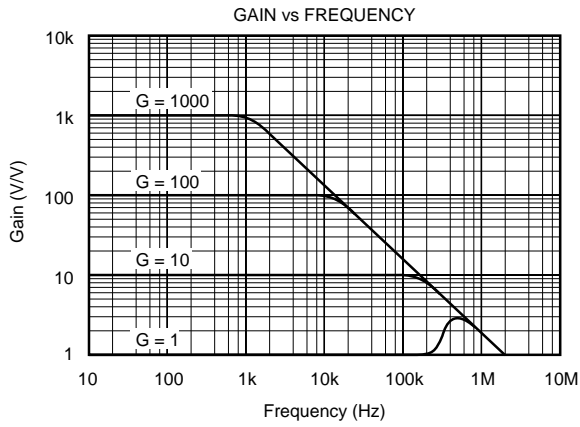
ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA120AP	18-Pin Plastic DIP	$-25^\circ C$ to $+85^\circ C$
INA120BP	18-Pin Plastic DIP	$-25^\circ C$ to $+85^\circ C$
INA120BG	18-Pin Ceramic DIP	$-25^\circ C$ to $+85^\circ C$
INA120CG	18-Pin Ceramic DIP	$-25^\circ C$ to $+85^\circ C$

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

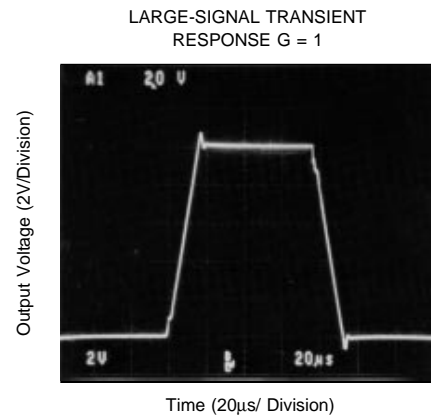
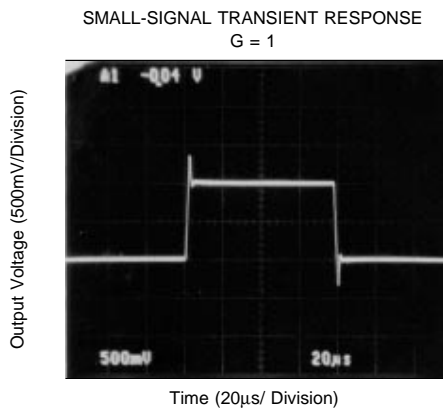
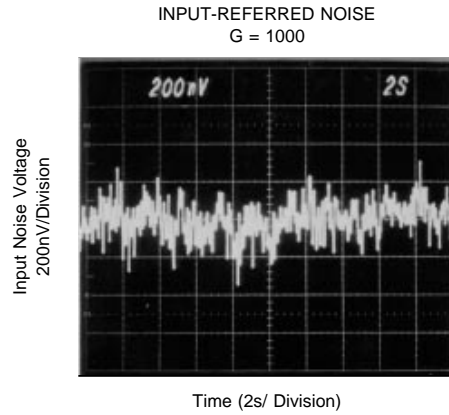
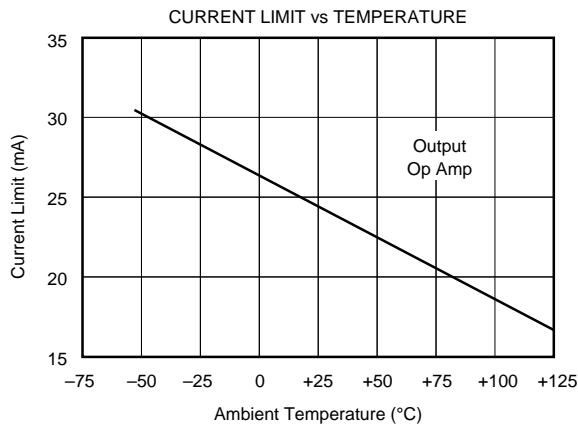
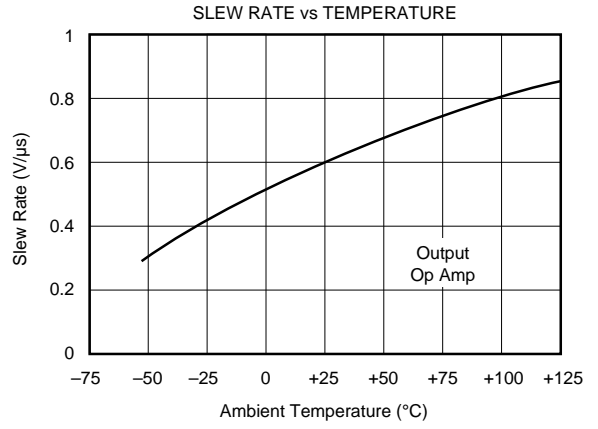
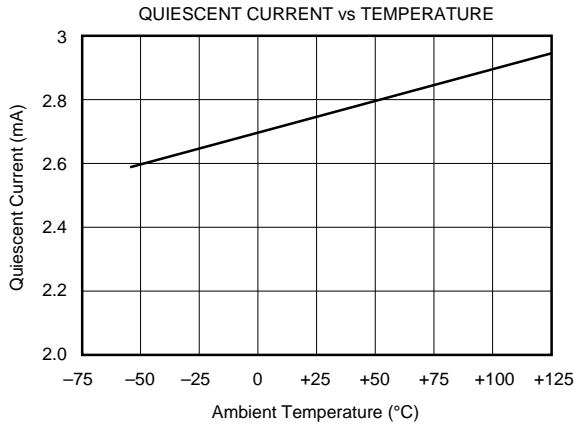
TYPICAL PERFORMANCE CURVES

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



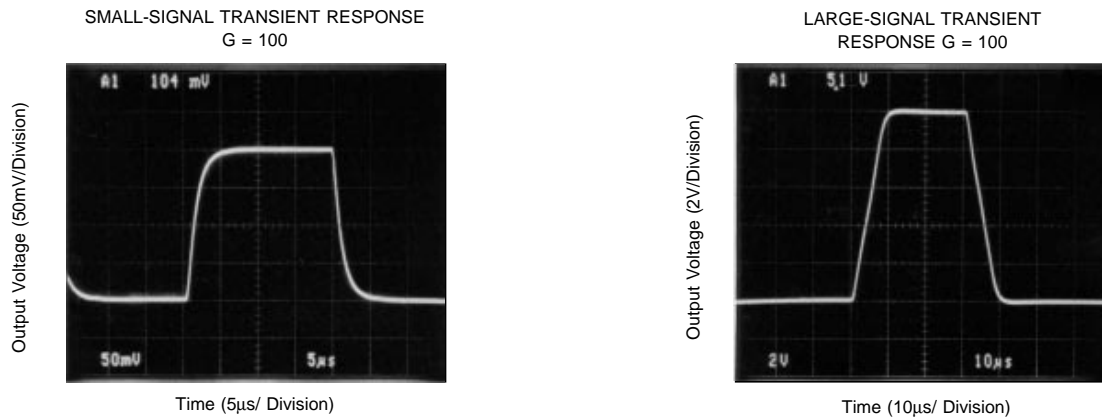
TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

$T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise noted.



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA120. Applications with noisy or high impedance power supply lines may require decoupling capacitors close to the device pins as shown. The differential input voltage is applied to pins 16 and 3.

The output is referred to the output common reference terminal, pin 18. This terminal must have a low-impedance connection to ground. A resistance of 1Ω or greater in series with the common terminal could degrade common-mode rejection beyond the specified value.

SETTING THE GAIN

Gains of 1, 10, 100 or 1000 can be configured by interconnecting the gain-set pins as shown in the table of Figure 1. These pin-strapped gains provide best gain accuracy and drift because they are determined by the ratios of accurately trimmed and matched on-chip resistors.

Digital gain control can be achieved using an analog multiplexer as shown in Figure 2. Since the switches are in series with the high impedance gain-sense connections, pins 4 and 15, their series resistance does not significantly affect gain error or drift. Gain error at $G = 1$ is slightly higher than with direct pin connections shown in Figure 1. The gain is selected with a two-bit address, A_0 and A_1 . The Multiplexer Enable control is directly connected to V_+ since a logic “low” on this line would cause the input amplifiers to run open-loop.

Other gains may be set by connecting an external resistor, R_G , as shown in Figure 3a. Gain accuracy using an external gain-setting resistor is a function of R_G and the internal $20\text{k}\Omega$ resistors. The internal resistors are typically within $\pm 0.2\%$ of nominal value and their drift under $\pm 80\text{ppm}/^\circ\text{C}$. Inaccuracy and drift of R_G will contribute additional gain error and drift.

Figure 3b shows an external gain-setting resistor connected in parallel with internal resistors. By forming a portion of the

effective R_G with internal resistors, gain accuracy and drift can be somewhat improved.

Connections available on the INA120 allow all input stage gain-setting resistors to be provided externally. A custom precision resistor network could be connected to provide the highest accuracy and lowest gain drift for non-standard gains. Impedance of this external network should be made close to that of the internal network for best performance.

OFFSET TRIMMING

Many applications require no external offset voltage trimming. Figure 4 shows optional circuits for trimming offset voltage. Since the INA120 has two amplification stages, the offset voltage is comprised of two components—the input stage offset and output stage offset.

The input stage offset is equal to the combined offset of op amps A_1 and A_2 . This input stage offset dominates at high gain. When used in gains of 100 to 1000, it is often sufficient to adjust the input stage offset with a potentiometer connected to pins 6 and 7 as shown. Connect both inputs to ground and adjust for 0V at the output, pin 1. Do not use pins 6 and 7 to trim offset voltage at $G = 1$ or to correct for offset in devices following the INA120 since this can cause excessive offset voltage drift.

At $G = 1$, offset is dominated by the output stage. Output stage offset can be trimmed by applying a correction voltage at the output reference terminal, pin 18. Low impedance must be maintained at this node to preserve the high CMR of the INA120. This is achieved by buffering the trim voltage with an op amp as shown.

At intermediate gains it may be necessary to provide both input stage and output stage offset adjustments. Again, ground both inputs. Connect a jumper between pins 9 and 11 (temporarily connects the INA120 in high gain) and adjust R_1 for 0V at the output, pin 1. Then disconnect the jumper and adjust the output offset control for 0V output.

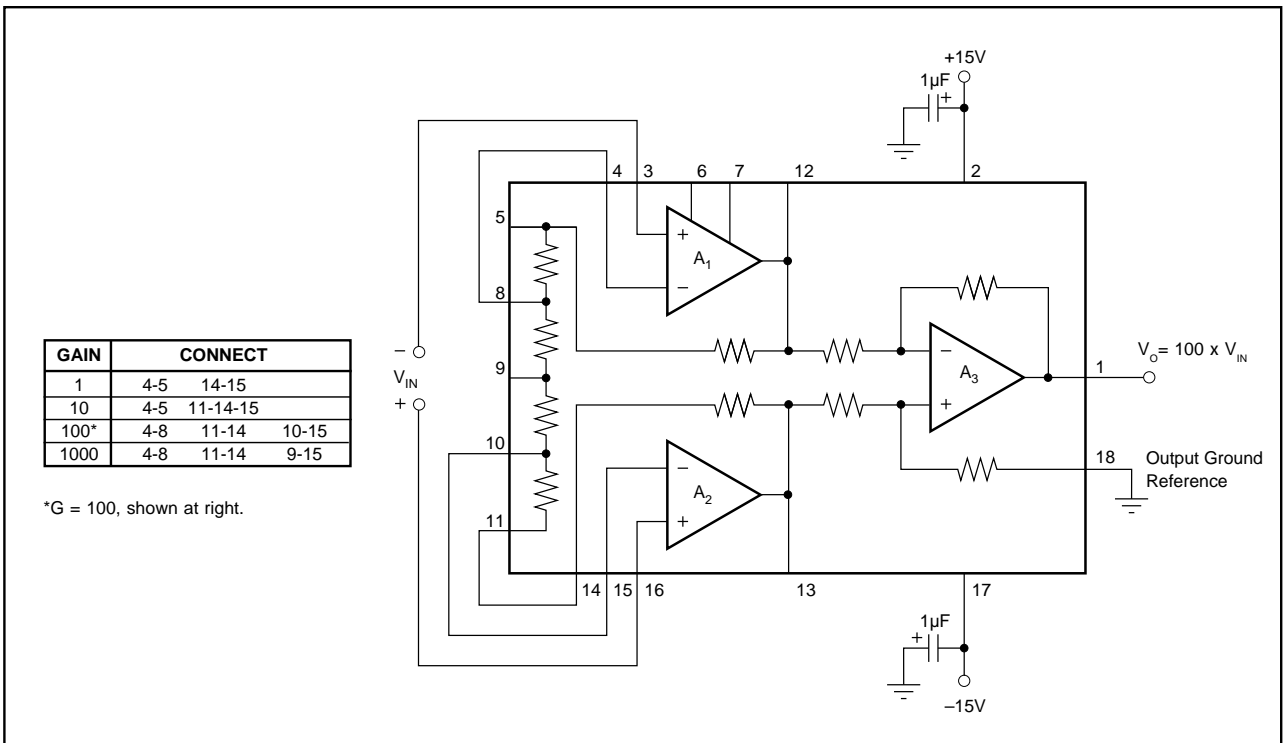


FIGURE 1. Basic Connection.

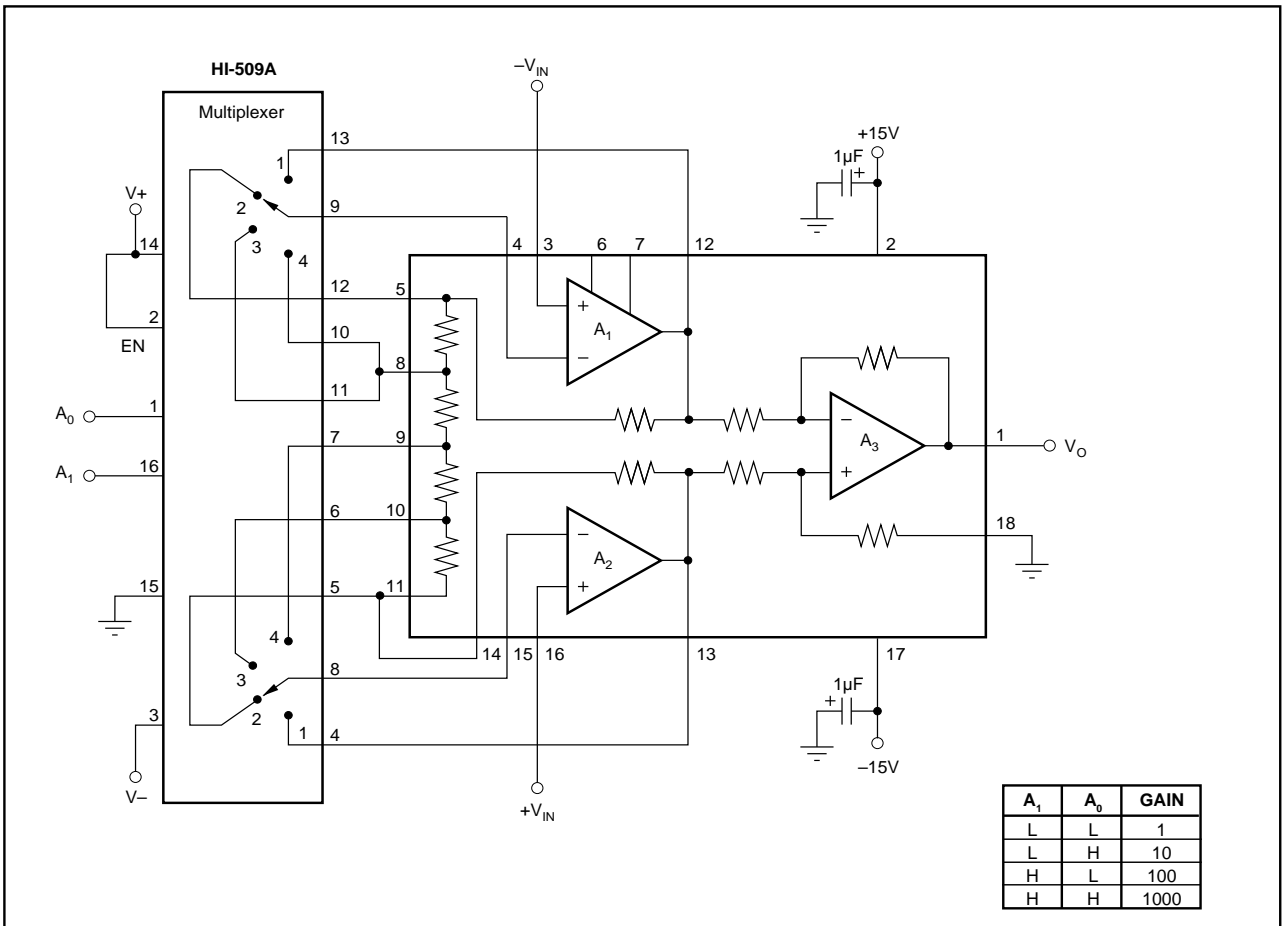


FIGURE 2. Digital Gain Control.

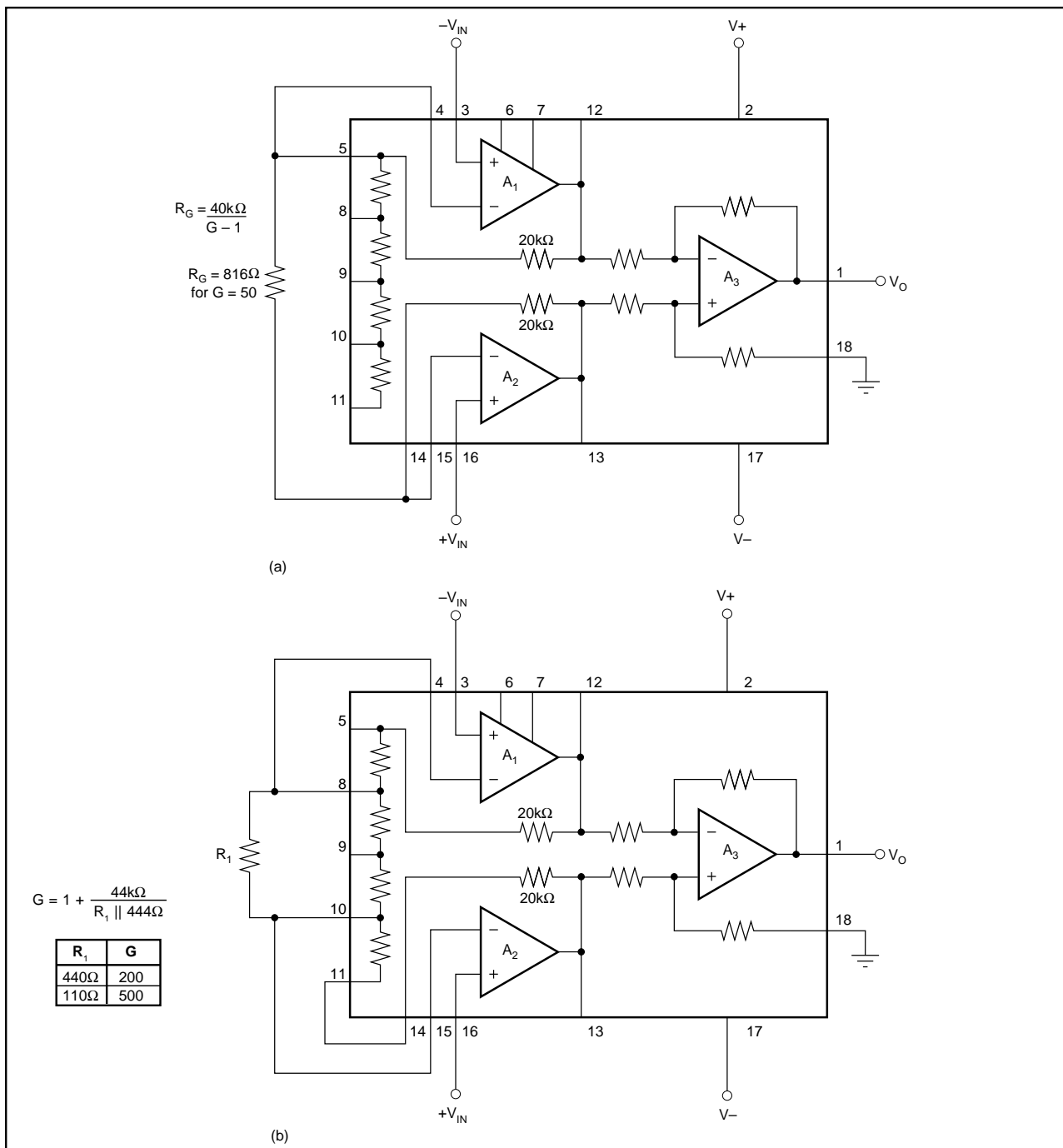


FIGURE 3. External Gain-Setting Resistors.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA120 is extremely high—approximately $10^{10}\Omega$. This does not mean, however, that no current flows in the input terminals. The input bias current of the INA120 is typically $\pm 10\text{nA}$ (it can be either polarity). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the INA120 is to function. Figure 5 shows various provisions for an input bias current path. Without an appropriate current path, the inputs will float to a potential which

exceeds the common-mode range of the INA120 and the input amplifiers will saturate.

INPUT PROTECTION

The inputs of the INA120 are protected for input voltages up to 2V beyond the power supply voltages. If the input can exceed these conditions, input clamp diodes should be provided as shown in Figure 6. R_s may not be required if the input cannot supply more than 100mA. If the input can supply larger currents, choose R_s according to the maximum source voltage, limiting current to under 100mA.

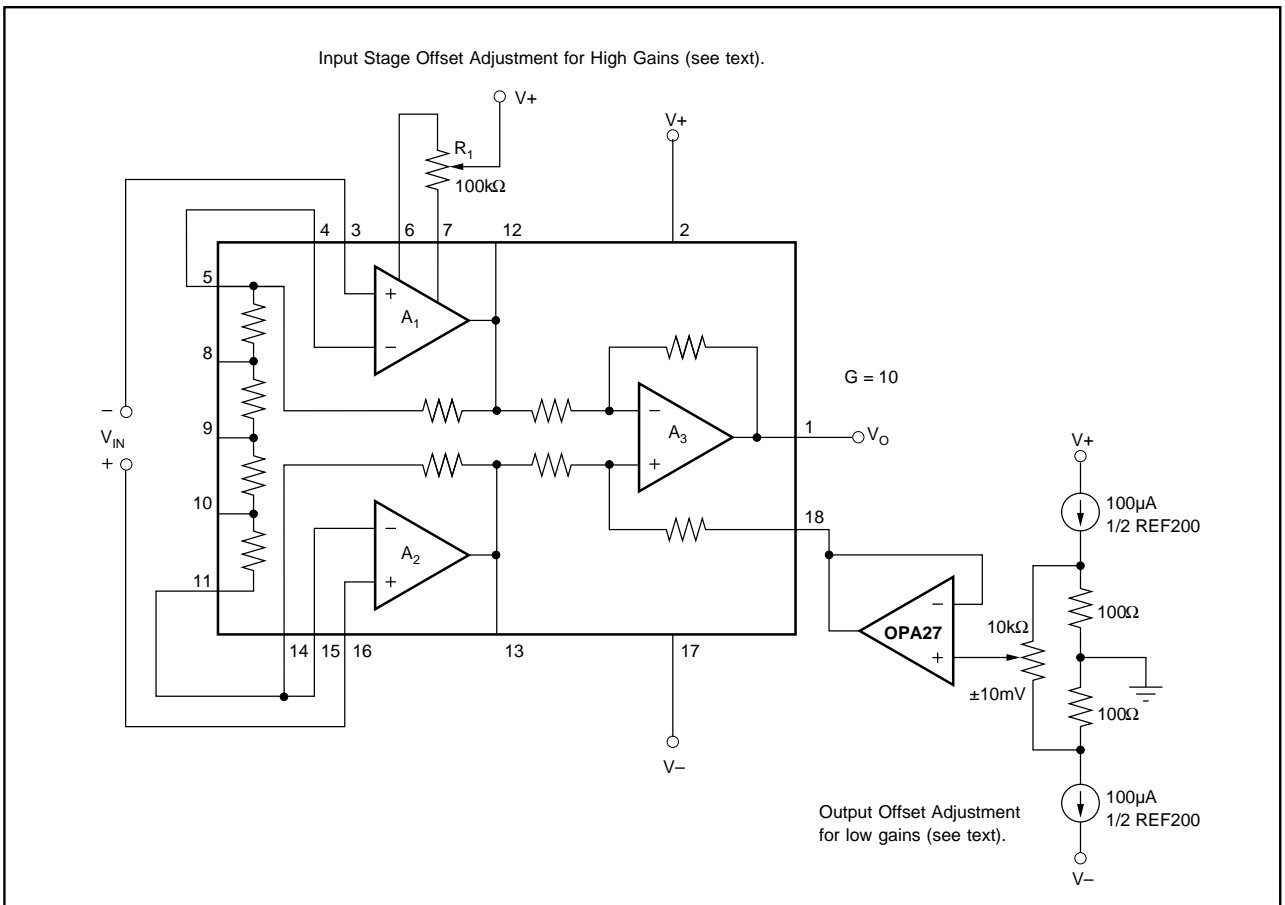


FIGURE 4. Offset Adjustment Circuits.

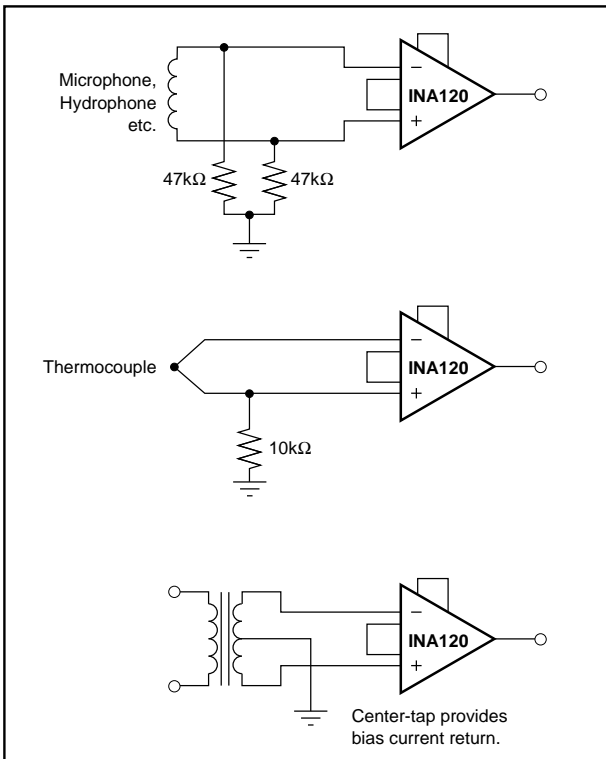


FIGURE 5. Providing an Input Bias Current Path.

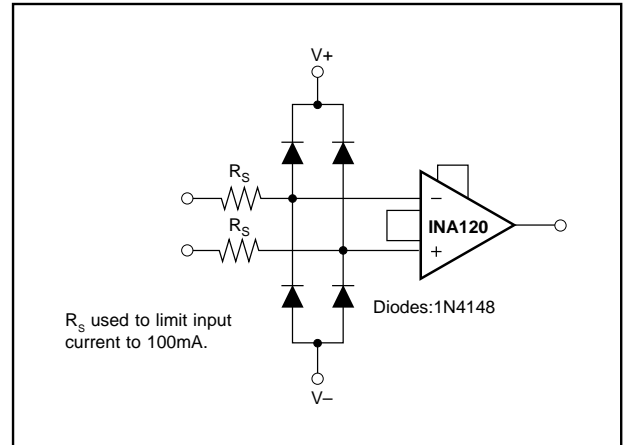


FIGURE 6. Input Protection Circuit.

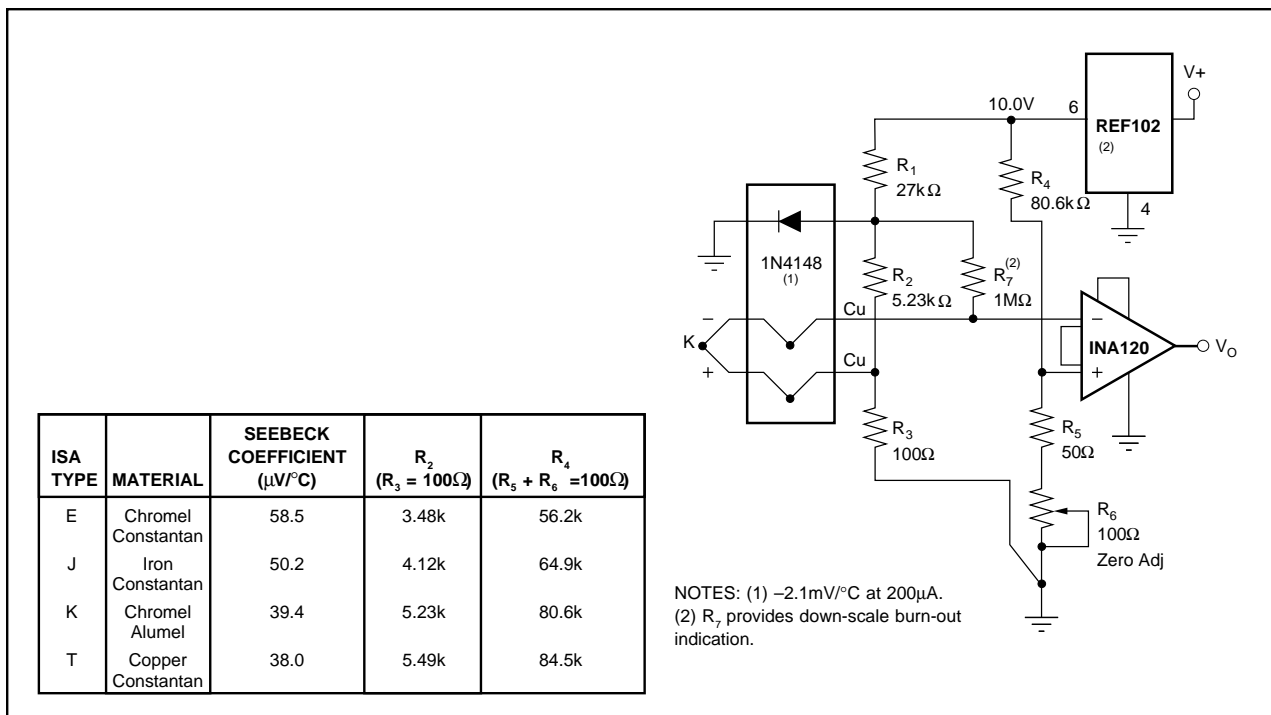


FIGURE 7. Thermocouple Amplifier With Cold Junction Compensation.

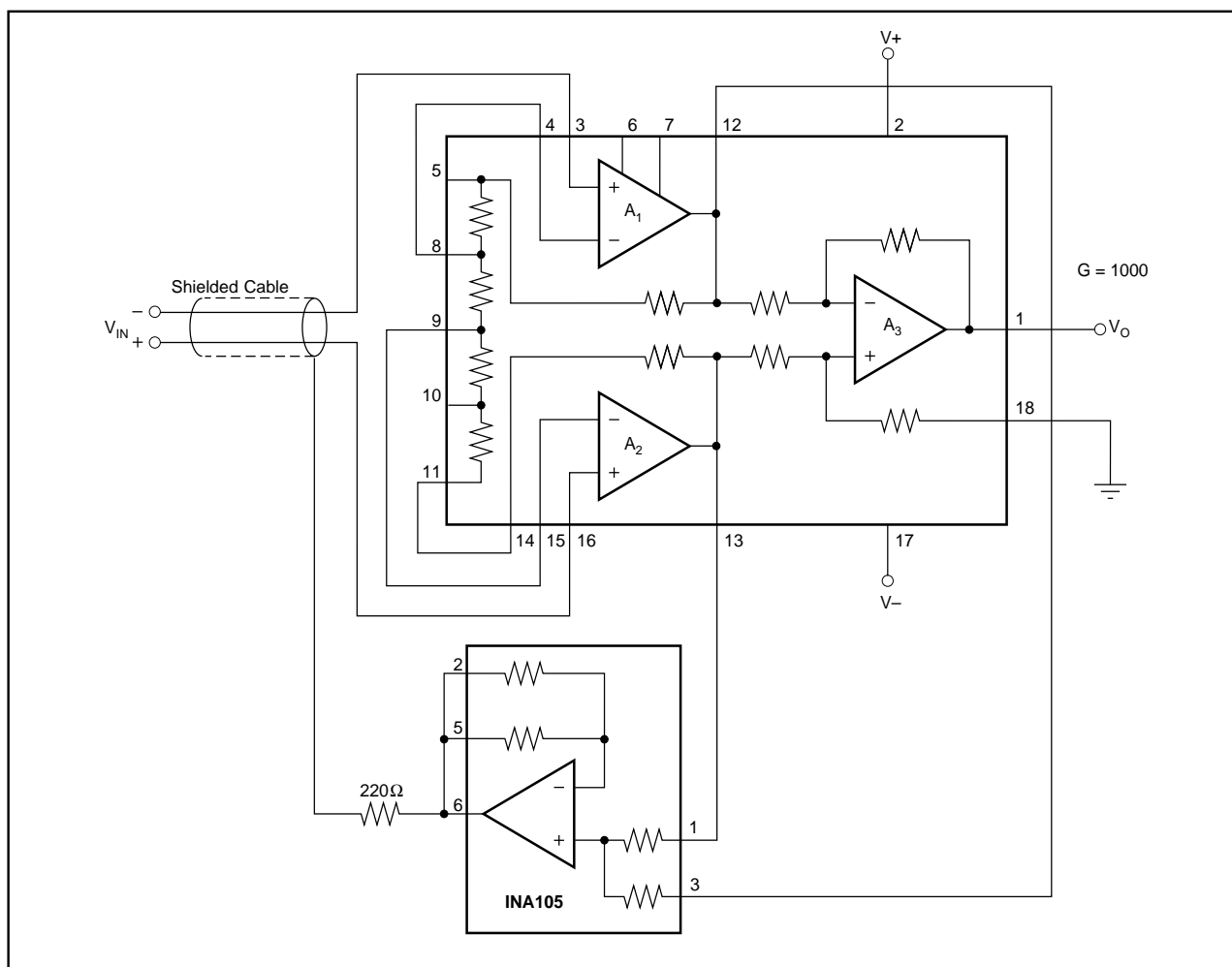


FIGURE 8. Guard Drive Circuit.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated