Easy-to-Use, Low-Power, Low-Supply TEMPERATURE SWITCH in MicroPackage

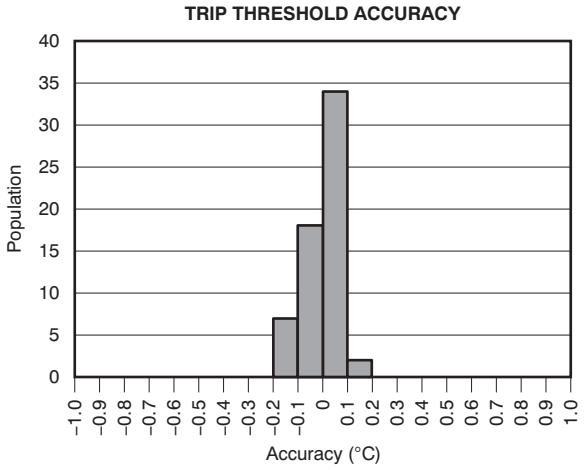
Check for Samples: TMP302A TMP302B TMP302C TMP302D

FEATURES

- **LOW POWER: 15µA (max)**
- **SOT563 PACKAGE: 1,6mm x 1,6mm x 0,6mm**
- **TRIP-POINT ACCURACY: ±0.2°C (typ) from +40°C to +125°C**
- **PIN-SELECTABLE TRIP POINTS**
- **OPEN-DRAIN OUTPUT**
- **SELECTABLE HYSTERESIS: 5°C/10°C**
- **LOW SUPPLY VOLTAGE RANGE: 1.4V to 3.6V**

APPLICATIONS

- **CELL PHONE HANDSETS**
- **PORTABLE MEDIA PLAYERS**
- **CONSUMER ELECTRONICS**
- **SERVERS**
- **POWER-SUPPLY SYSTEMS**
- **DC-DC MODULES**
- **THERMAL MONITORING**
- **ELECTRONIC PROTECTION SYSTEMS**



DESCRIPTION

The TMP302x is a temperature switch in a micropackage (SOT563). The TMP302x offers low power (15µA max) and ease-of-use through pin-selectable trip points and hysteresis.

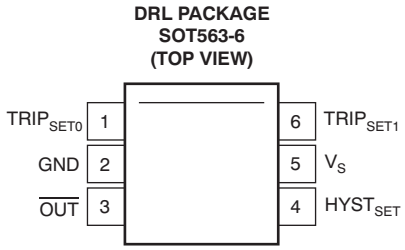
These devices require no additional components for operation; they can function independent of microprocessors or microcontrollers.

The TMP302x is available in several different versions. For additional trip points, contact a TI representative.

TMP302 Available Versions(1)

DEVICE	SELECTABLE TRIP POINTS (°C)
TMP302A	50, 55, 60, 65
TMP302B	70, 75, 80, 85
TMP302C	90, 95, 100, 105
TMP302D	110, 115, 120, 125

(1) For other available trip points, please contact a TI representative.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION(1)

PRODUCT	TRIP POINTS (°C)	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
TMP302A	50, 55, 60, 65	SOT563	DRL	OCP
TMP302B	70, 75, 80, 85	SOT563	DRL	OCT
TMP302C	90, 95, 100, 105	SOT563	DRL	OCR
TMP302D	110, 115, 120, 125	SOT563	DRL	OCS

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

		TMP302A, TMP302B, TMP302C, TMP302D	UNIT
Supply Voltage		+3.6	V
Input Pins, Voltage	$TRIP_{SET0}$, $TRIP_{SET1}$, $HYST_{SET}$	–0.5 to V_S + 0.5	V
Output Pin, Voltage	$\overline{OUT}$	–0.5 to +3.6	V
Output Pin, Current	$\overline{OUT}$	10	mA
Operating Temperature		–55 to +130	°C
Storage Temperature Range		–60 to +150	°C
Junction Temperature Range		+150	°C
ESD Rating:	Human Body Model (HBM)	2000	V
	Charged-Device Model (CDM)	1000	V
	Machine Model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

ELECTRICAL CHARACTERISTICS

At T_A = –40°C to +125°C, and V_S = +1.4V to +3.6V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	TMP302 (1)			UNIT
		MIN	TYP	MAX	
TEMPERATURE MEASUREMENT					
Trip Point Accuracy	T_A = +40°C to +125°C		±0.2	±2	°C
vs. Supply			±0.2	±0.5	°C/V
Trip Point Hysteresis	$HYST_{SET}$ = GND		5		°C
	$HYST_{SET}$ = V_S		10		°C
TEMPERATURE TRIP POINT SET					
Temperature Trip Point Set	$TRIP_{SET1}$ = GND, $TRIP_{SET0}$ = GND		Default		°C
	$TRIP_{SET1}$ = GND, $TRIP_{SET0}$ = V_S		Default + 5		°C
	$TRIP_{SET1}$ = V_S, $TRIP_{SET0}$ = GND		Default + 10		°C
	$TRIP_{SET1}$ = V_S, $TRIP_{SET0}$ = V_S		Default + 15		°C
HYSTERESIS SET INPUT					
Input Logic Levels:					
V_{IH}		0.7 × (V_S)		V_S	V
V_{IL}		–0.5		0.3 × (V_S)	V
Input Current:					
I_{IN}	0 < V_{IN} < 3.6V			1	µA
DIGITAL OUTPUT					
Output Logic Level:					
V_{OL}	V_S > 2V, I_{OL} = 3mA	0		0.4	V
	V_S < 2V, I_{OL} = 3mA	0		0.2 × (V_S)	V
POWER SUPPLY					
Operating Supply Range		1.4		3.6	V
Quiescent Current I_Q			8	15	µA
	V_S = 3.3V, T_A = +50°C		7		µA
TEMPERATURE RANGE					
Specified Range		–40		+125	°C
Operating Range		–55		+130	°C
Thermal Resistance θ_{JA}					
SOT563	JEDEC Low-K Board		+260		°C/W

(1) 100% of all units are production tested at T_A = +25°C. Over temperature specifications are specified by design.

TYPICAL CHARACTERISTICS

At T_A = +25°C and V_S = 3.3V, unless otherwise noted.

TRIP ACCURACY ERROR vs TEMPERATURE

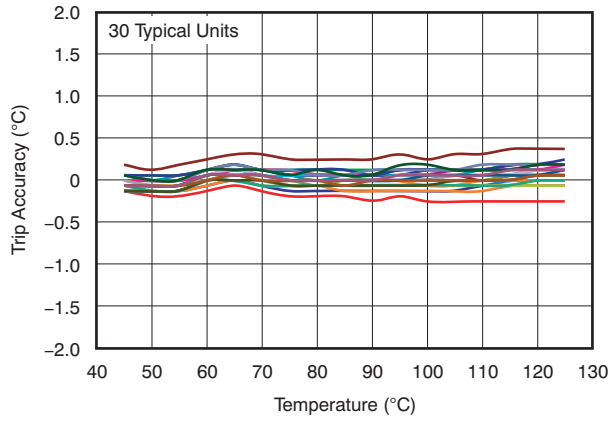


Figure 1.

QUIESCENT CURRENT vs TEMPERATURE

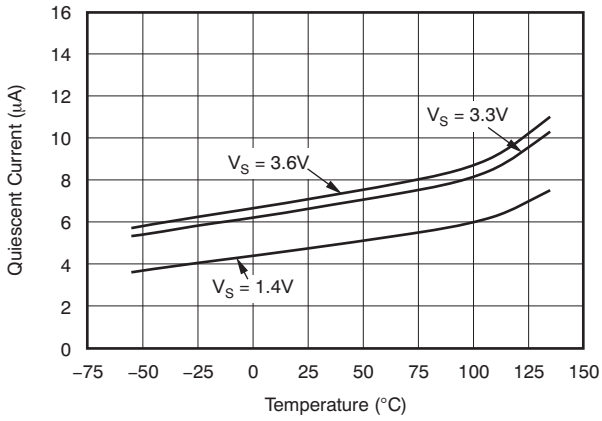


Figure 2.

TEMPERATURE STEP RESPONSE IN PERFLUORINATED FLUID AT +100°C vs TIME

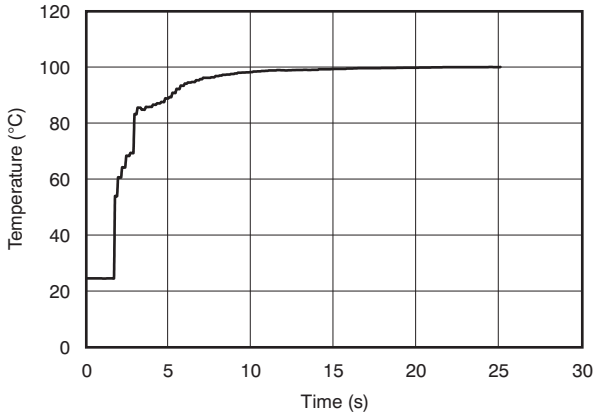


Figure 3.

THERMAL STEP RESPONSE IN AIR AT +100°C vs TIME

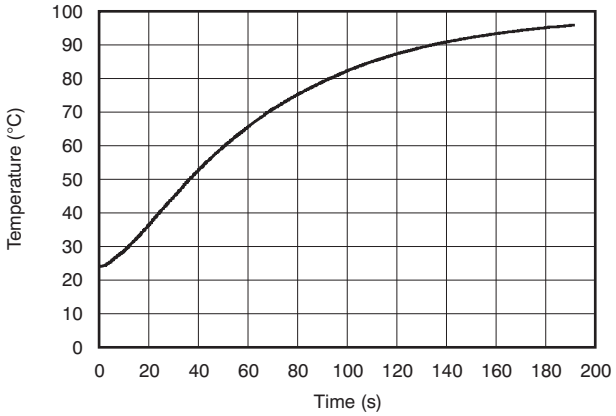


Figure 4.

TRIP THRESHOLD ACCURACY

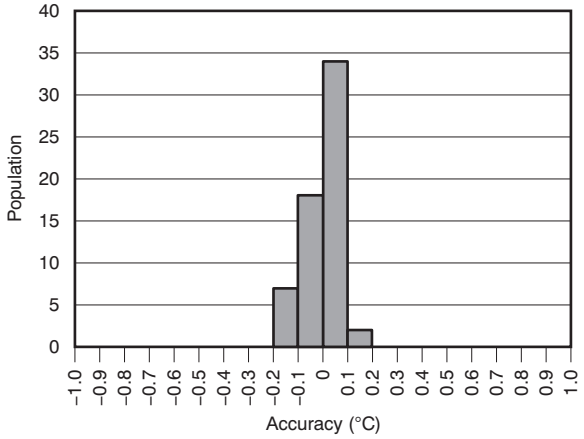


Figure 5.

OUTPUT LOGIC LEVEL LOW V_{OL} vs TEMPERATURE

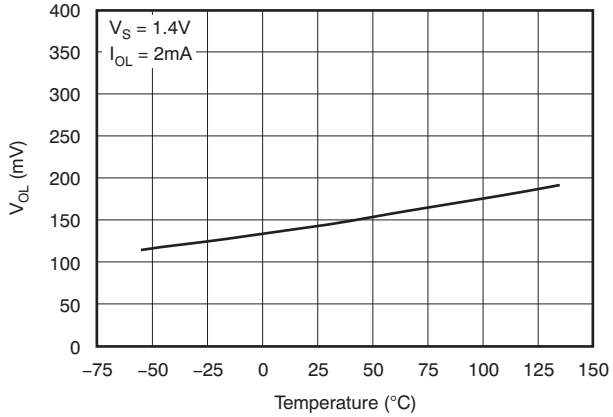


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V_S = 3.3V, unless otherwise noted.

POWER-UP AND POWER-DOWN RESPONSE

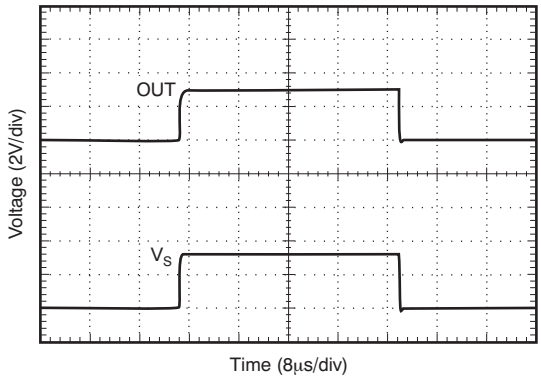


Figure 7.

POWER-UP, TRIP, AND POWER-DOWN RESPONSE

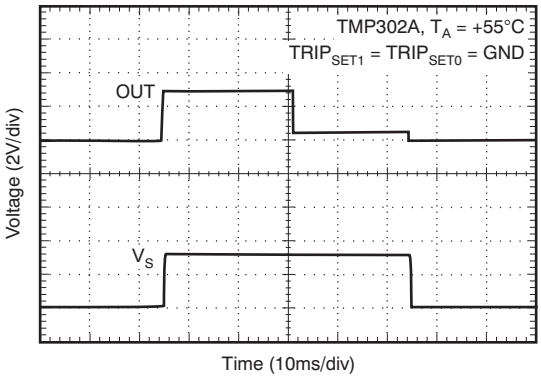


Figure 8.

APPLICATION INFORMATION

The TMP302 temperature switch is optimal for ultralow-power battery applications that require accurate trip thresholds. The trip thresholds are programmable to four different settings using the $TRIP_{SET1}$ and $TRIP_{SET0}$ pins. Table 1 shows the pin settings versus trip points.

Table 1. Trip Point vs $TRIP_{SET1}$ and $TRIP_{SET0}$

$TRIP_{SET1}$	$TRIP_{SET0}$	TMP302A	TMP302B	TMP302C	TMP302D
GND	GND	+50°C	+70°C	+90°C	+110°C
GND	V_S	+55°C	+75°C	+95°C	+115°C
V_S	GND	+60°C	+80°C	+100°C	+120°C
V_S	V_S	+65°C	+85°C	+105°C	+125°C

The typical thermal response time for the TMP302 is about 250ms. This period is the minimum time frame that it takes for the open-drain output ($\overline{OUT}$) to change its state from low to high (or vice-versa) while the device is active. A maximum low output voltage is defined as a voltage level equivalent to 0.2 × V_S; likewise, a minimum high output voltage is defined as 0.8 × V_S. It is important to note that an exception to the nominal 250ms response time occurs on power up—in this case, it is possible to achieve a thermal response in as little as 35ms.

CONFIGURING THE TMP302

The TMP302 is simple to configure. The only external components that it requires are a bypass capacitor and pull-up resistor. Power-supply bypassing is strongly recommended; use a 0.1µF capacitor placed as close as possible to the supply pin. To minimize the internal power dissipation of the TMP302, use a pull-up resistor value greater than 10kΩ from $\overline{OUT}$ to V_S. Refer to Table 1 for trip point temperature configuration. The $TRIP_{SET}$ pins can be toggled dynamically; however, the voltage of these pins must not exceed V_S. To ensure a proper logic high, the voltage must not drop below 0.7V × V_S.

$HYST_{SET}$

If the temperature trip threshold is crossed, the open-drain output ($\overline{OUT}$) goes low and does not return to its original high state (that is, V_S) until the temperature returns to a value within a hysteresis window set by the $HYST_{SET}$ pin. The $HYST_{SET}$ pin allows the user to choose between a +5°C and a +10°C hysteresis window. Table 2 shows the hysteresis window that corresponds to the $HYST_{SET}$ setting.

Table 2. $HYST_{SET}$ Window

$HYST_{SET}$	THRESHOLD HYSTERESIS
GND	+5°C
V_S	+10°C

For the specific case of the TMP302A, if the $HYST_{SET}$ pin is set to +10°C (that is, connected to V_S) and the device is configured with a +60°C trip point ($TRIP_{SET1}$ = V_S, $TRIP_{SET0}$ = GND), once this threshold is exceeded the output does not return to its original high state until it reaches +50°C. This case is more clearly illustrated in Figure 9.

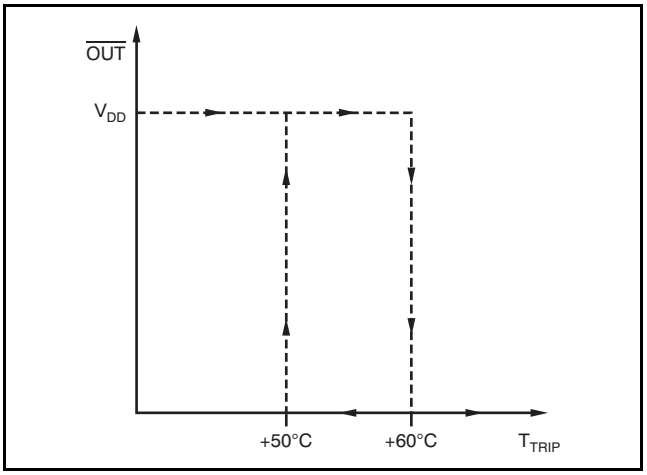


Figure 9. TMP302A; $HYST_{SET}$ = V_S; $TRIP_{SET1}$ = V_S, $TRIP_{SET0}$ = GND

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TMP302ADRLR	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCP	Samples
TMP302ADRLT	ACTIVE	SOT	DRL	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCP	Samples
TMP302BDRLR	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCT	Samples
TMP302BDRLT	ACTIVE	SOT	DRL	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCT	Samples
TMP302CDRLR	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCR	Samples
TMP302CDRLT	ACTIVE	SOT	DRL	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCR	Samples
TMP302DDRLR	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCS	Samples
TMP302DDRLT	ACTIVE	SOT	DRL	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCS	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

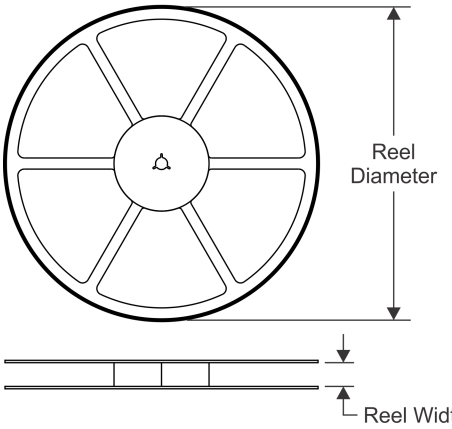
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

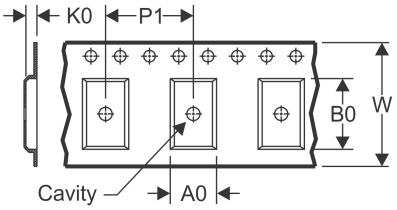
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

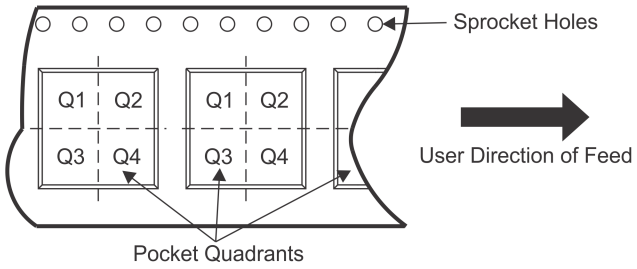


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

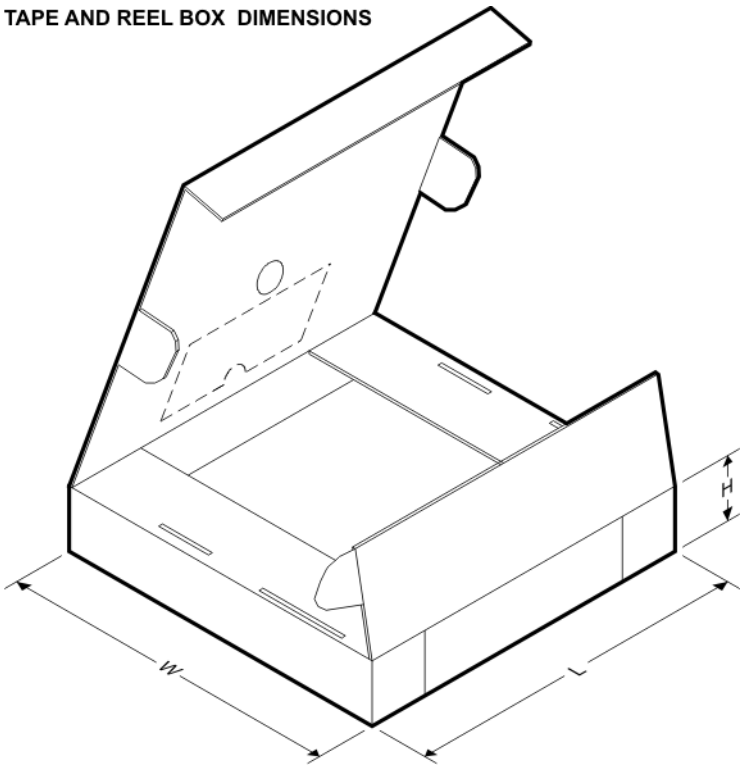
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

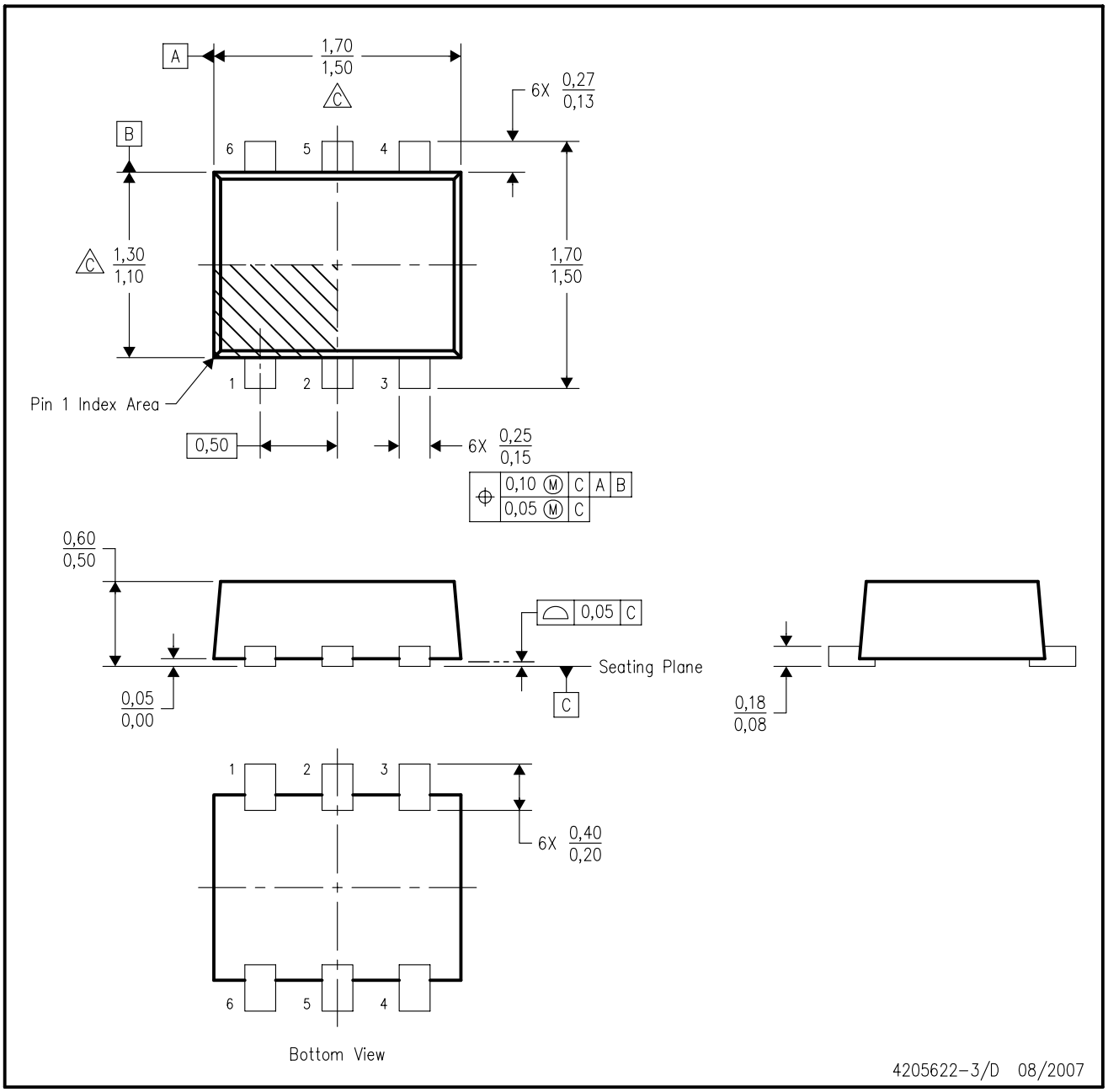
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP302ADRLR	SOT	DRL	6	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
TMP302ADRLR	SOT	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP302ADRLT	SOT	DRL	6	250	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
TMP302ADRLT	SOT	DRL	6	250	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP302BDRLR	SOT	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP302BDRLR	SOT	DRL	6	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
TMP302BDRLT	SOT	DRL	6	250	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP302BDRLT	SOT	DRL	6	250	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
TMP302CDRLR	SOT	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP302CDRLR	SOT	DRL	6	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
TMP302CDRLT	SOT	DRL	6	250	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
TMP302DDRLR	SOT	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP302DDRLR	SOT	DRL	6	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
TMP302DDRLT	SOT	DRL	6	250	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TMP302DDRLT	SOT	DRL	6	250	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



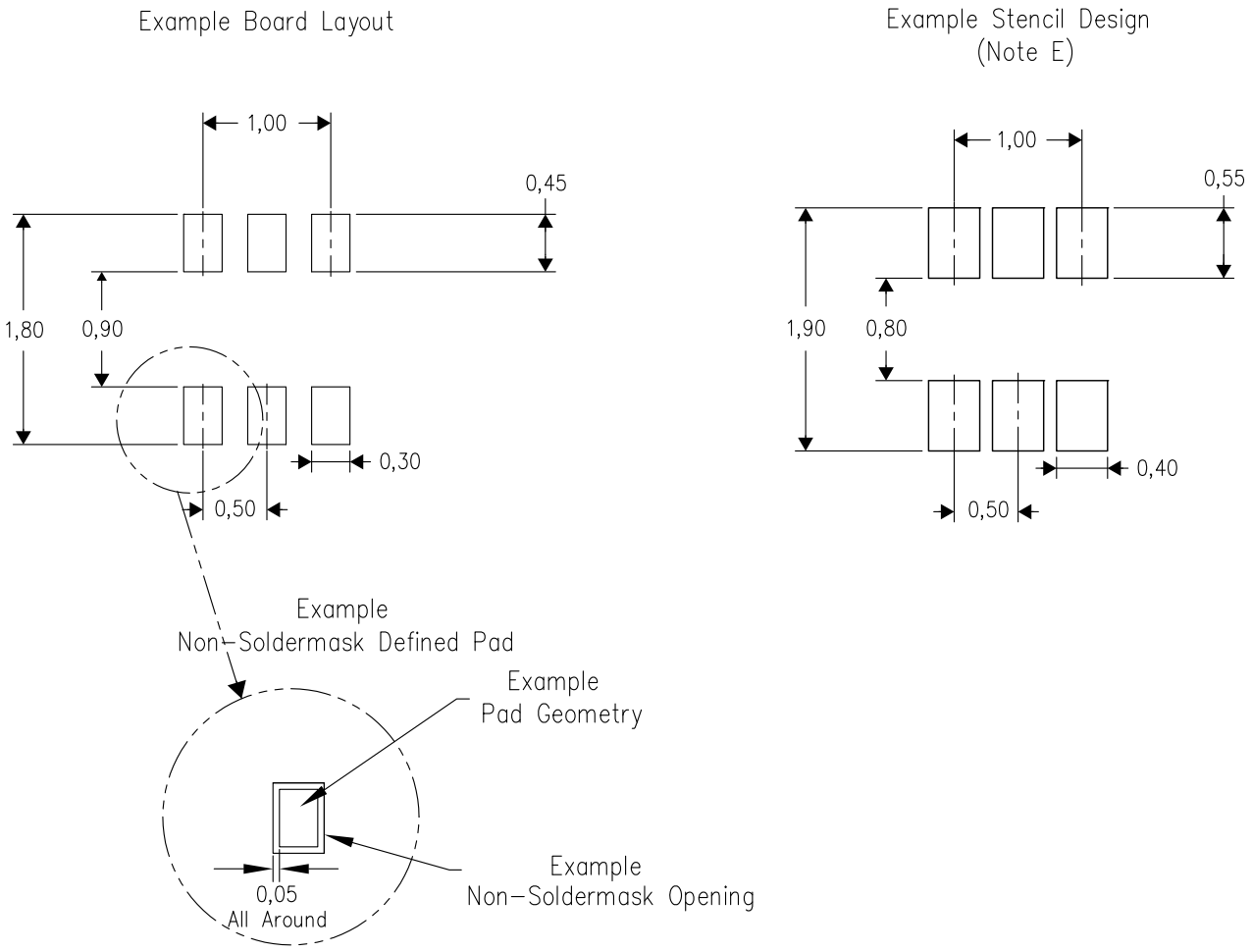
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP302ADRLR	SOT	DRL	6	4000	180.0	180.0	30.0
TMP302ADRLR	SOT	DRL	6	4000	202.0	201.0	28.0
TMP302ADRLT	SOT	DRL	6	250	180.0	180.0	30.0
TMP302ADRLT	SOT	DRL	6	250	202.0	201.0	28.0
TMP302BDRLR	SOT	DRL	6	4000	202.0	201.0	28.0
TMP302BDRLR	SOT	DRL	6	4000	180.0	180.0	30.0
TMP302BDRLT	SOT	DRL	6	250	202.0	201.0	28.0
TMP302BDRLT	SOT	DRL	6	250	180.0	180.0	30.0
TMP302CDRLR	SOT	DRL	6	4000	202.0	201.0	28.0
TMP302CDRLR	SOT	DRL	6	4000	180.0	180.0	30.0
TMP302CDRLT	SOT	DRL	6	250	180.0	180.0	30.0
TMP302DDRLR	SOT	DRL	6	4000	202.0	201.0	28.0
TMP302DDRLR	SOT	DRL	6	4000	180.0	180.0	30.0
TMP302DDRLT	SOT	DRL	6	250	202.0	201.0	28.0
TMP302DDRLT	SOT	DRL	6	250	180.0	180.0	30.0



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

DRL (R–PDSO–N6) PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265