250-MHz, CMOS Transimpedance Amplifier (TIA) with Integrated Switch and Buffer

Check for Samples: OPA1S2384, OPA1S2385

FEATURES

- **Wide Bandwidth: 250 MHz**
- **High Slew Rate: 150 V/μs**
- **Rail-to-Rail Input/Output (I/O)**
- **Fast Settling**
- **Low Input Bias Current: 3 pA**
- **High Input Impedance: 10^{13} Ω || 2 pF**
- **SPST Switch:**
  - **Low On-Resistance: 7 Ω**
  - **Low Charge Injection: 1 pC**
  - **Low Leakage Current: 10 pA**
- **Flexible Configuration:**
  - **Transimpedance Gain**
  - **External Hold Capacitor**
  - **Post-Gain**
- **Single Supply: +2.7 V to +5.5 V**
- **Low Quiescent Current: 9.8 mA**
- **Small Package: 3-mm × 3-mm SON-10**

APPLICATIONS

- **Communications:**
  - **Optical Networking: EPON, GPON**
  - **Signal Strength Monitors**
  - **Burst-Mode RSSI**
- **Photodiode Monitoring**
- **Fast Sample-and-Hold Circuits**
- **Charge Amplifiers**
- **High-Speed Integrators**

DESCRIPTION

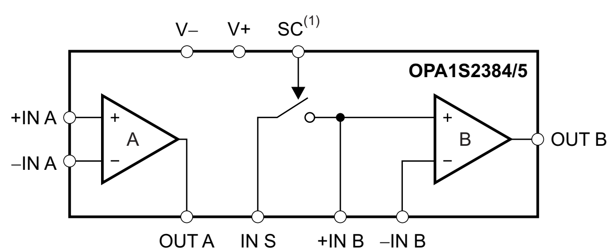
The OPA1S2384 and OPA1S2385 (OPA1S238x) combine high bandwidth, FET-input operational amplifiers with a fast SPST CMOS switch designed for applications that require the tracking and capturing of fast signals.

By providing a 250-MHz gain bandwidth product and rail-to-rail input/output swings in single-supply operation, the OPA1S238x is capable of wideband transimpedance gain and large output signal swing simultaneously. Low input bias current and voltage noise (6 nV/√Hz) make it possible to amplify extremely low-level input signals for maximum signal-to-noise ratio.

The characteristics of the OPA1S238x make this device ideally suited for use as a wideband photodiode amplifier.

In addition, the CMOS switch and subsequent buffer amplifier allow the OPA1S238x to be easily configured as a fast sample-and-hold circuit. The external hold capacitor and post-gain options make the OPA1S238x easily adoptable to a wide range of speed and accuracy requirements. Note that the OPA1S2384 closes the internal switch with a logic-high signal, and the OPA1S2385 closes the internal switch with a logic-low signal.

The OPA1S238x are optimized for low-voltage operation from as low as +2.7 V up to +5.5 V. These devices are specified for a temperature range of –40°C to +85°C.



(1) Polarity of the switch depends on ordering code.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA1S2384(2)	SON-10	DRC	–40°C to +85°C	OVAQ	OPA1S2384IDRCT	TBD
					OPA1S2384IDRCR	TBD
OPA1S2385	SON-10	DRC	–40°C to +85°C	OUZQ	OPA1S2385IDRCT	Tape and Reel, 250
					OPA1S2385IDRCR	Tape and Reel, 3000

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the INA230 product folder at www.ti.com.
(2) OPA1S2384 is product preview.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		OPA1S238x	UNIT
Supply voltage, V+ to V–		6	V
Signal input terminals, op amp section	Voltage(2)	(V–) – 0.3 to (V+) + 0.3	V
	Current(2)	±10	mA
On-state switch current; $V_{IN\ S}$, $V_{+IN\ B}$ = 0 to V+		±20	mA
Output (OUT A, OUT B) short-circuit current(3)		Continuous	
Digital input voltage range (SC pin)		–0.3 to +6	V
Digital input clamp current (SC pin)		–50	mA
Operating temperature, T_A		–40 to +125	°C
Storage temperature, T_{stg}		–65 to +150	°C
Junction temperature, T_J		+150	°C
ESD Ratings	Human body model (HBM)	4000	V
	Charged-device model (CDM)	1000	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

ELECTRICAL CHARACTERISTICS: V_{SS} = +2.7 V to +5.5 V(1) (2)

At T_A = +25°C, R_L = 1 kΩ connected to V_S / 2, and V_O = V_{CM} = V_S / 2, unless otherwise noted.

PARAMETER		CONDITIONS	OPA1S238x MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			2	8	mV
$\Delta V_{OS}/\Delta T$	Input offset voltage vs temperature	T_A = –40°C to +85°C		6		µV/°C
PSRR	Input offset voltage vs power supply	V_{CM} = V_S / 2 – 0.65 V		0.2	0.8	mV/V
	Channel separation, dc	At f = 5 MHz		10		µV/V
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	No phase reversal, rail-to-rail input	(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V	66	80		dB
		V_S = 3.3 V, (V–) – 0.1 V < V_{CM} < (V+) + 0.1 V	50	68		dB
INPUT BIAS CURRENT						
I_B	Input bias current			±3	±50	pA
I_{OS}	Input offset current			±1	±50	pA
NOISE						
	Input noise voltage density	f = 1 MHz		6		nV/√Hz
		f = 10 MHz		26		nV/√Hz
	Input current noise density	f = 1 MHz		50		fA/√Hz
INPUT CAPACITANCE						
	Differential			2		pF
	Common-mode			2		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 2.7 V, 0.3 V < V_O < (V+) – 0.3 V, R_L = 1 kΩ	88	100		dB
		V_S = 5.5 V, 0.3 V < V_O < (V+) – 0.3 V, R_L = 1 kΩ	90	110		dB
		T_A = –40°C to +85°C V_S = 5.5 V, 0.3 V < V_O < (V+) – 0.3 V, R_L = 1 kΩ	84			dB
FREQUENCY RESPONSE						
	Gain bandwidth product	V_S = 3.3 V, R_L = 1 kΩ, C_L = 10 pF, G = 10		90		MHz
		V_S = 5.0 V, R_L = 1 kΩ, C_L = 10 pF, G = 10		100		MHz
	Small-signal bandwidth	V_S = 5.0 V, G = 1, V_O = 0.1 V_{PP}, R_F = 25 Ω		250		MHz
		V_S = 5.0 V, G = 2, V_O = 0.1 V_{PP}, R_F = 25 Ω		90		MHz
SR	Slew rate	V_S = 3.3 V, G = 1, 2-V step		110		V/µs
		V_S = 5 V, G = 1, 2-V step		130		V/µs
		V_S = 5 V, G = 1, 4-V step		150		V/µs
t_r	Rise time	V_S = 5 V, G = 1, V_O = 2 V_{PP}, 10% to 90%		11		ns
t_f	Fall time	V_S = 5 V, G = 1, V_O = 2 V_{PP}, 90% to 10%		11		ns
t_s	Settling time	To 0.1%, V_S = 3.3 V, G = 1, 2-V step		30		ns
		To 0.01%, V_S = 3.3 V, G = 1, 2-V step		60		ns
	Overload recovery time	V_S = 3.3 V, V_{IN} × Gain = V_S		5		ns
OUTPUT						
	Voltage output swing from supply rails	V_S = 5.5 V, R_L = 1 kΩ		100		mV
	Short-circuit current	V_S = 5.0 V		100		mA
		V_S = 3.3 V		50		mA
	Closed-loop output impedance			0.05		Ω
	Open-loop output impedance			35		Ω

(1) Parameters with MIN and MAX specification limits are 100% production tested at +25ºC, unless otherwise noted. Over temperature limits are based on characterization and statistical analysis.
(2) Specified by design and/or characterization; not production tested.

ELECTRICAL CHARACTERISTICS: V_{SS} = +2.7 V to +5.5 V(1) (2) (continued)

At T_A = +25°C, R_L = 1 kΩ connected to V_S / 2, and V_O = V_{CM} = V_S / 2, unless otherwise noted.

PARAMETER		CONDITIONS	OPA1S238x MIN	OPA1S238x TYP	OPA1S238x MAX	UNIT
POWER SUPPLY						
V_S	Operating supply range		2.7		5.5	V
I_Q	Quiescent current	V_S = 5.5 V, I_O = 0 mA		9.8	12	mA
TEMPERATURE						
	Specified range		–40		+85	°C
	Operating range		–40		+125	°C
	Storage range		–65		+150	°C

ELECTRICAL CHARACTERISTICS: Switch Section(1)

At T_A = +25°C and V_S = 3.3 V, unless otherwise noted.

PARAMETER		CONDITIONS	OPA1S238x MIN	OPA1S238x TYP	OPA1S238x MAX	UNIT
DC						
	Analog voltage range	V_S = 2.7 V to 5.5 V	0		V_{S+}	V
r_{on}	On-state resistance	V_{IN} = V+ / 2, I_{COM} = 10 mA		7	16	Ω
I_{lkg}	Off-state leakage current	V_{IN} = V+ / 2, $V_{+IN\ B}$ = 0 V	–0.5	0.01	0.5	nA
DYNAMIC						
t_{ON}	Turn-on time	V_{IN} = V+ / 2, C_L = 35 pF, R_L = 300 Ω		20		ns
t_{OFF}	Turn-off time	V_{IN} = V+ / 2, C_L = 35 pF, R_L = 300 Ω		15		ns
Q_C	Charge injection	C_L = 1 nF		1		pC
BW	Bandwidth	Signal = 0 dBm (0.632 mV_{PP}, 50 Ω)		450		MHz
	Off isolation	f = 1 MHz, signal = 1 Vrms, 50 Ω		–82		dB
	Off capacitance (IN_S)	Switch open, f = 1 MHz, V_{BIAS} = 0 V		6.5		pF
	Off capacitance (+IN_B)	Switch open, f = 1 MHz, V_{BIAS} = 0 V		8.5		pF
	On capacitance (IN_S)	Switch closed, f = 1 MHz, V_{BIAS} = 0 V		13		pF
	On capacitance (+IN_B)	Switch closed, f = 1 MHz, V_{BIAS} = 0 V		15		pF
DIGITAL CONTROL INPUT (SC pin)						
V_{IH}	High-level input voltage	V_S = 5.5 V, T_A = –40°C to +85°C	2.4		V_{S+}	V
		V_S = 3.3 V, T_A = –40°C to +85°C	2.0		V_{S+}	V
V_{IL}	Low-level input voltage		0		0.9	V
$I_{lkg(SC)}$	Input leakage current	$V_{IN\ S}$ = V+ or 0 V	–0.5	0.01	0.5	µA
		T_A = –40°C to +85°C	–5		5	µA
	Input capacitance			3		pF

(1) Parameters with MIN and MAX specification limits are 100% production tested at +25ºC, unless otherwise noted. Over temperature limits are based on characterization and statistical analysis.

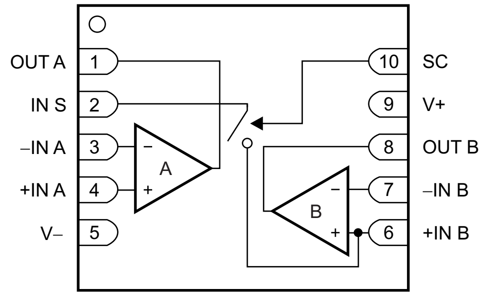
THERMAL INFORMATION

THERMAL METRIC(1)		OPA1S238x DRC (SON) 10 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	46.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	53.8	°C/W
θ_{JB}	Junction-to-board thermal resistance	21.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.9	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	6.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PIN CONFIGURATION

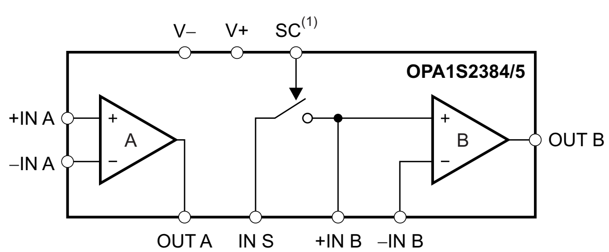
**DRC PACKAGE
DFN-10
(TOP VIEW)**



PIN DESCRIPTIONS

PIN		DESCRIPTION
NAME	NO.	
+IN A	4	Noninverting input of amplifier channel A
–IN A	3	Inverting input of amplifier channel A
+IN B	6	Noninverting input of amplifier channel B
–IN B	7	Inverting input of amplifier channel B
IN S	2	Switch input
OUT A	1	Voltage output of amplifier channel A
OUT B	8	Voltage output of amplifier channel B
SC	10	Switch control pin. This logic input pin controls the SPST switch operation. For the OPA1S2384, a logic-low signal opens the switch and a logic-high signal closes the switch. For the OPA1S2385, a logic-low signal closes the switch and a logic high signal opens the switch.
V+	9	Positive supply voltage pin. Connect this pin to a voltage +2.7V to +5.5V.
V–	5	Negative supply voltage pin. Connect this pin to the ground (0 V) rail of the single-supply system power supply.

FUNCTIONAL BLOCK DIAGRAM



(1) Polarity of the SC pins depends on ordering option.

TYPICAL CHARACTERISTICS

At T_A = +25°C, R_L = 1 kΩ connected to V_S / 2, and V_O = V_{CM} = V_S / 2, unless otherwise noted.

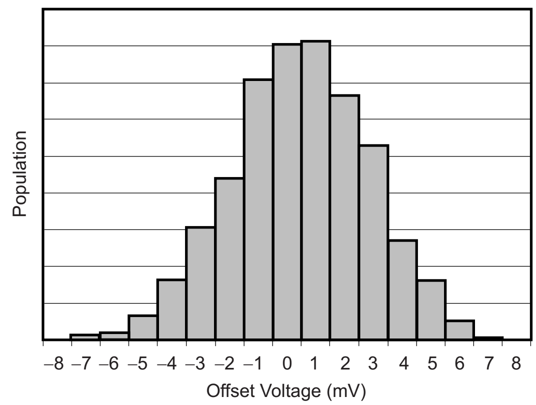


Figure 1. OFFSET VOLTAGE PRODUCTION DISTRIBUTION

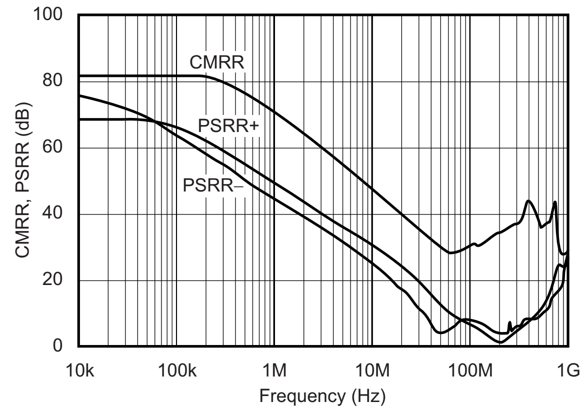


Figure 2. COMMON-MODE REJECTION RATIO AND POWER-SUPPY REJECTION RATIO vs FREQUENCY

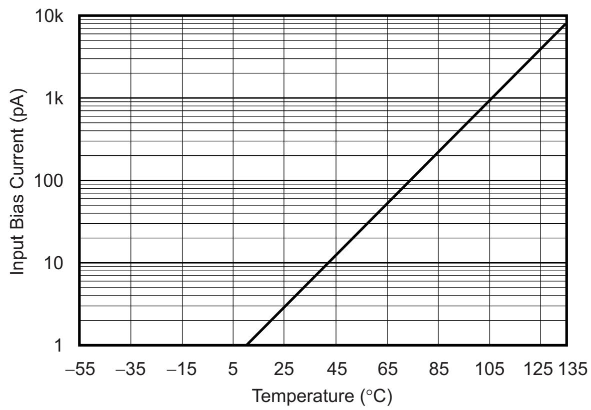


Figure 3. INPUT BIAS CURRENT vs TEMPERATURE

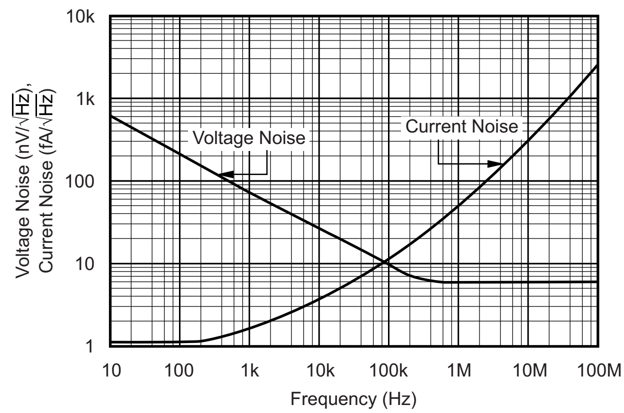


Figure 4. INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY

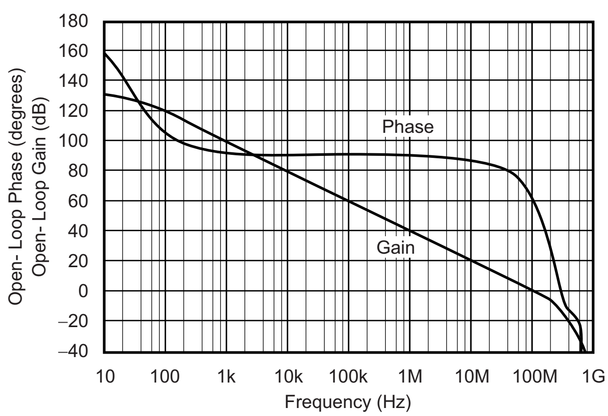


Figure 5. OPEN-LOOP GAIN AND PHASE

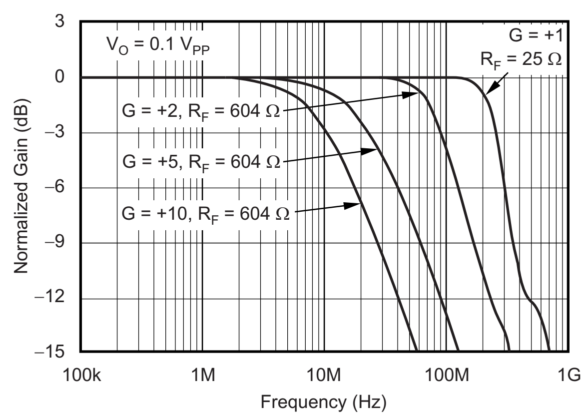


Figure 6. NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 1 kΩ connected to V_S / 2, and V_O = V_{CM} = V_S / 2, unless otherwise noted.

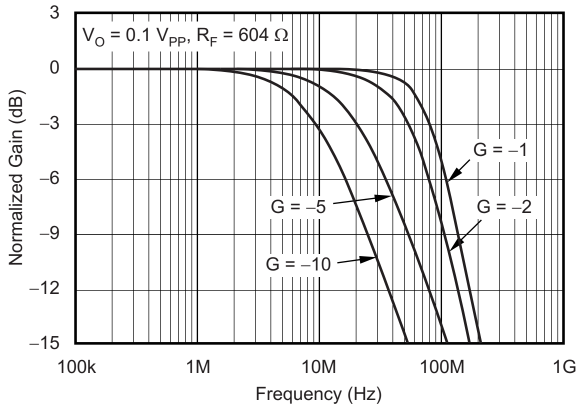


Figure 7. INVERTING SMALL-SIGNAL FREQUENCY RESPONSE

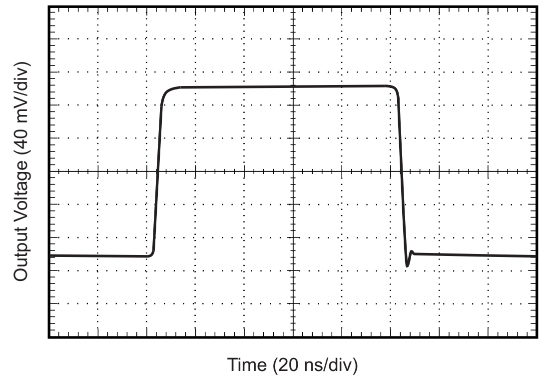


Figure 8. NONINVERTING SMALL-SIGNAL STEP RESPONSE

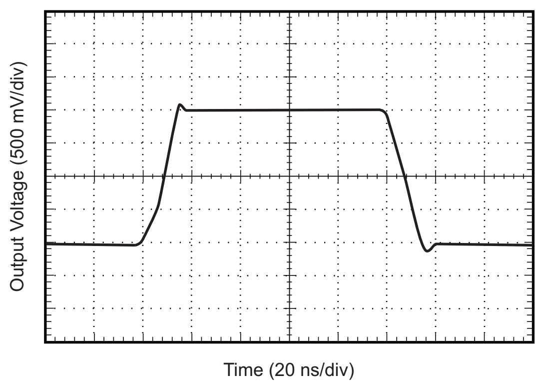


Figure 9. NONINVERTING LARGE-SIGNAL STEP RESPONSE

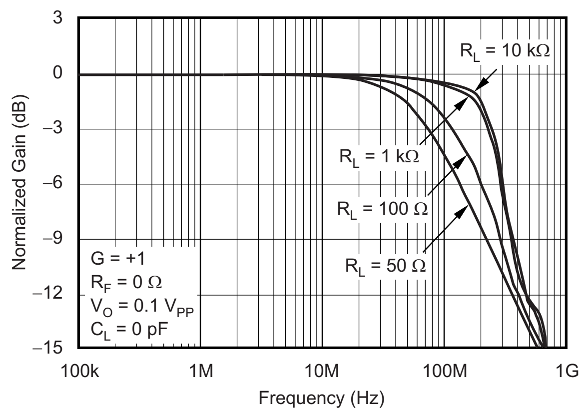


Figure 10. FREQUENCY RESPONSE FOR VARIOUS R_L

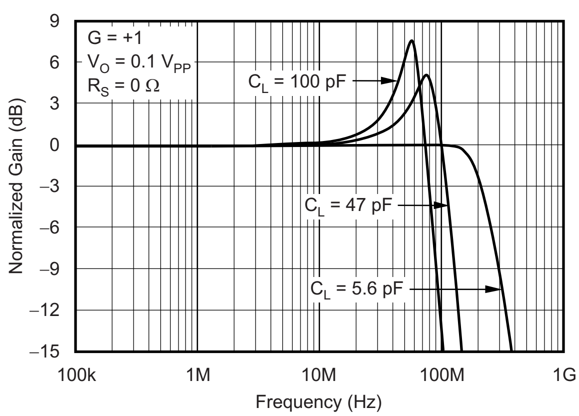


Figure 11. FREQUENCY RESPONSE FOR VARIOUS C_L

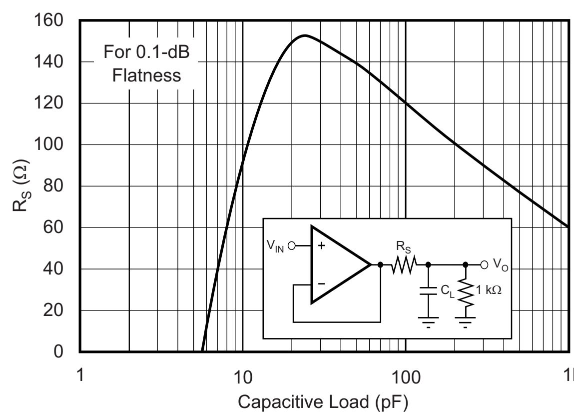


Figure 12. RECOMMENDED R_S vs CAPACITIVE LOAD

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 1 kΩ connected to V_S / 2, and V_O = V_{CM} = V_S / 2, unless otherwise noted.

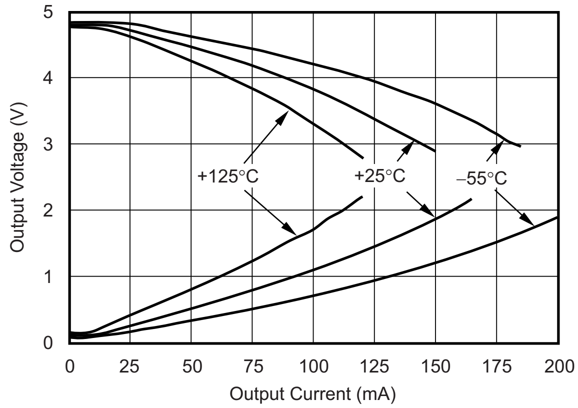


Figure 13. OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

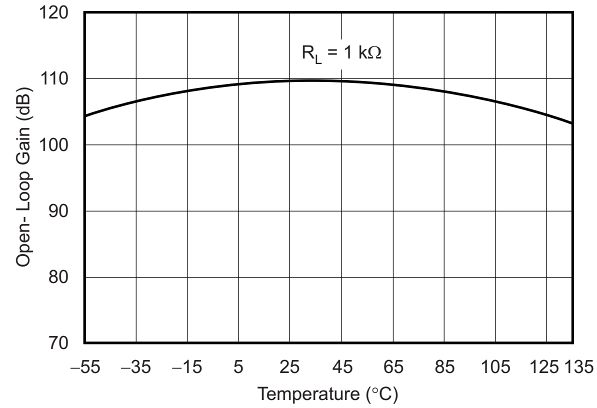


Figure 14. OPEN−LOOP GAIN vs TEMPERATURE

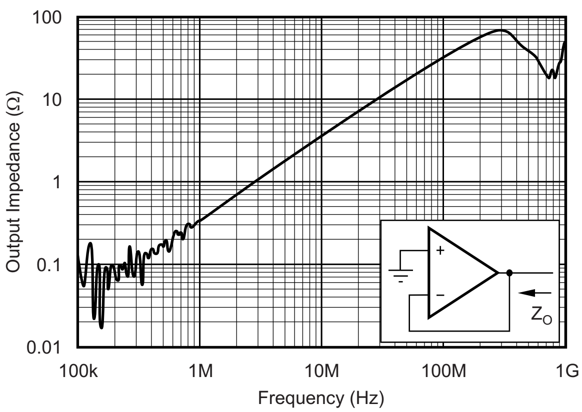


Figure 15. CLOSED−LOOP OUTPUT IMPEDANCE vs FREQUENCY

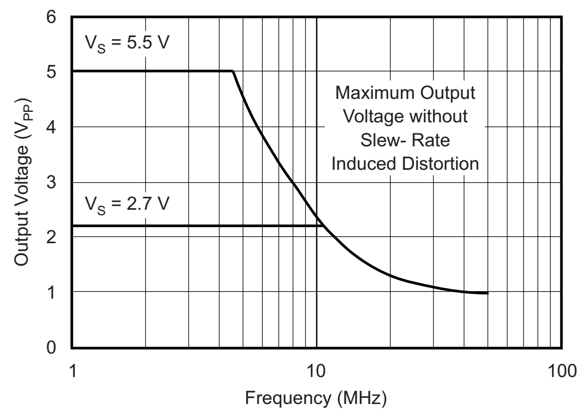


Figure 16. MAXIMUM OUTPUT VOLTAGE vs FREQUENCY

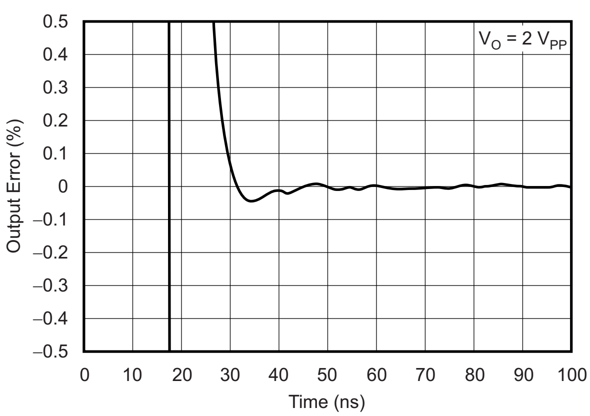


Figure 17. OUTPUT SETTLING TIME TO 0.1%

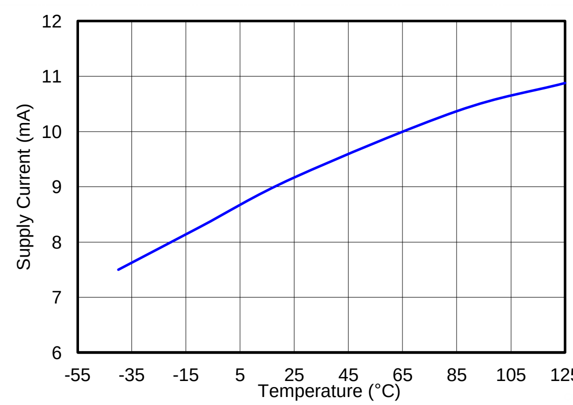


Figure 18. SUPPLY CURRENT vs TEMPERATURE

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 1 kΩ connected to V_S / 2, and V_O = V_{CM} = V_S / 2, unless otherwise noted.

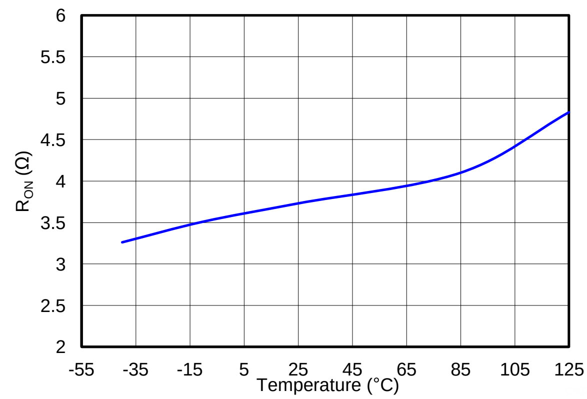


Figure 19. R_{ON} vs TEMPERATURE

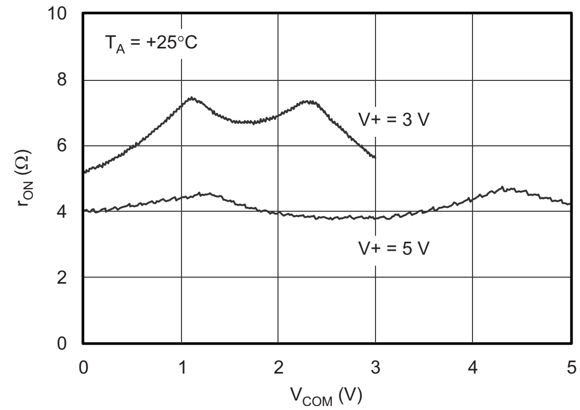


Figure 20. r_{ON} vs V_{COM}

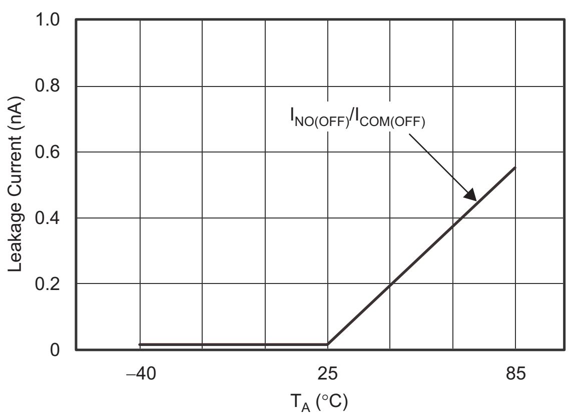


Figure 21. LEAKAGE CURRENT vs TEMPERATURE

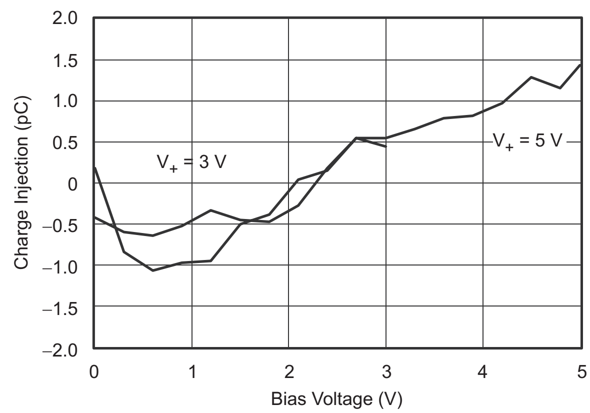


Figure 22. CHARGE-INJECTION (Q_C) vs V_{COM}

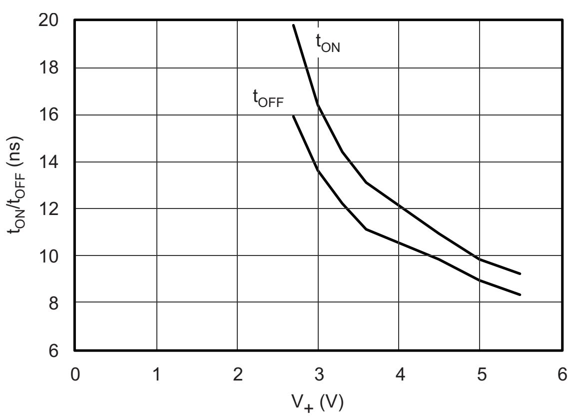


Figure 23. t_{ON} AND t_{OFF} vs SUPPLY VOLTAGE

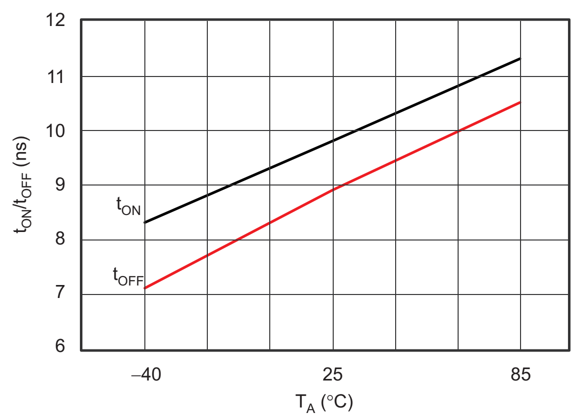


Figure 24. t_{ON} AND t_{OFF} vs TEMPERATURE (V+ = 5 V)

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, R_L = 1 kΩ connected to V_S / 2, and V_O = V_{CM} = V_S / 2, unless otherwise noted.

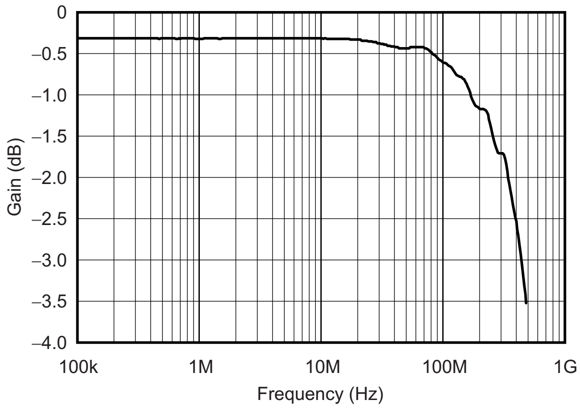


Figure 25. GAIN vs FREQUENCY

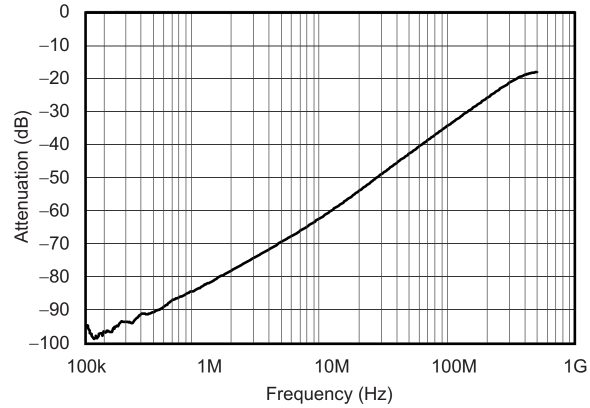


Figure 26. OFF ISOLATION vs FREQUENCY

APPLICATION INFORMATION

OPERATING VOLTAGE

The OPA1S238x operates over a power-supply range of +2.7 V to +5.5 V. Supply voltages higher than +6 V (absolute maximum) can permanently damage the device. Parameters that vary over supply voltage or over temperature are shown in the *Typical Characteristics* section of this data sheet.

INPUT VOLTAGE

The OPA1S238x input common-mode voltage range extends 0.1 V beyond the supply rails. Under normal operating conditions, the input bias current is approximately 3 pA. Input voltages exceeding the supply voltage can cause excessive current to flow into or out of the input pins. If there is a possibility that this operating condition may occur, the inputs must be protected. Momentary voltages that exceed the supply voltage can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor between the signal and the input pin of the device.

OUTPUT VOLTAGE

Rail-to-rail output is achieved by using a class AB output stage with common-source transistors. For high-impedance loads (> 200 Ω), the output voltage swing is typically 100 mV from the supply rails. With 10-Ω loads, a useful output swing can be achieved while maintaining high open-loop gain; see Figure 13.

OUTPUT DRIVE

The OPA1S238x output stage can supply a continuous output current of ±100 mA and still provide approximately 2.7 V of output swing on a 5-V supply; see Figure 13.

The OPA1S238x provides peak currents of up to 200 mA, which corresponds to the typical short-circuit current. Therefore, an on-chip thermal shutdown circuit is provided to protect the OPA1S238x from dangerously-high junction temperatures. At +160°C, the protection circuit shuts down the amplifier. Normal operation resumes when the junction temperature cools to below +140°C.

CAPACITIVE LOAD AND STABILITY

The OPA1S238x can drive a wide range of capacitive loads. However, all op amps can become unstable under certain conditions. Op amp configuration, gain, and load value are just a few of the factors to consider when determining stability. An op amp in a unity-gain configuration is most susceptible to the effects of capacitive loading. The capacitive load reacts with the op amp output resistance, along with any additional load resistance, to create a pole in the small-signal response that degrades the phase margin; see Figure 12 for details.

The OPA1S238x topology enhances its ability to drive capacitive loads. In unity gain, these op amps perform well with large capacitive loads. See Figure 10 and Figure 11 for details.

One method of improving capacitive load drive in the unity-gain configuration is to insert a 10-Ω to 20-Ω resistor in series with the output. This resistor significantly reduces ringing with large capacitive loads. For details about stability with certain output capacitors, see Figure 11. However, if there is a resistive load in parallel with the capacitive load, R_S creates a voltage divider, This voltage divider, introduces a dc error at the output and slightly reduces output swing. This error may be insignificant. For instance, with R_L = 10 kΩ and R_S = 20 Ω, there is only about a 0.2% error at the output.

WIDEBAND TRANSIMPEDANCE AMPLIFIER

Wide bandwidth, low input bias current and low current noise make the OPA1S238x an ideal wideband, photodiode, transimpedance amplifier for low-voltage, single-supply applications. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequencies.

POWER DISSIPATION

Power dissipation depends on power-supply voltage, signal, and load conditions. With dc signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor. Power dissipation can be minimized by using the lowest possible power-supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a dc output voltage of one-half the power-supply voltage. Dissipation with ac signals is lower. Application bulletin AB-039 (SBOA022), *Power Amplifier Stress and Power Handling Limitations*, explains how to calculate or measure power dissipation with unusual signals and loads, and is available for download at www.ti.com.

Repeated activation of the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +150°C, maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered at +160°C. However, for reliable operation, design your system to operate at a maximum of 35°C below the thermal protection trigger temperature (that is, +125°C or less).

TYPICAL APPLICATIONS

The following sections show typical applications of the OPA1S238x and explain their basic functionality.

Signal Strength Detection

The OPA1S238x can be used to detect the signal strength of a fast changing optical signal. Figure 27 shows a simplified circuit for this application.

Optical sensors like photodiodes often generate a current that is proportional to the amount of light detected by these sensors. The current generated by this sensor is represented by the current source I_{IN}, as shown in Figure 27. One of the OPA1S238x op amps is configured in a transimpedance configuration. If it is assumed that this op amp behaves like an ideal op amp, then all the current generated by I_{IN} flows through R1 and generates a voltage drop of I_{IN} × R1. The voltage at the output of this op amp can then be calculated by $V_{TIA} = V_{BIAS} + I_{IN} \times R1$. This calulation assumes ideal components.

In real-life applications, the current generated by I_{IN} can change very quickly. The current at a specific point in time can be measured by using the internal switch of the OPA1S238x. When the switch is closed, the C2 capacitor is charged to the output voltage level of the first amplifier (V_{TIA}). By opening the switch, the output is disconnected from C2, and the voltage at the noninverting terminal of the second op amp remains at the same voltage level as when the switch was opened. The second op amp is configured in a buffer configuration and prevents the C2 capacitor from being discharged by a load at the V_{OUT} terminal.

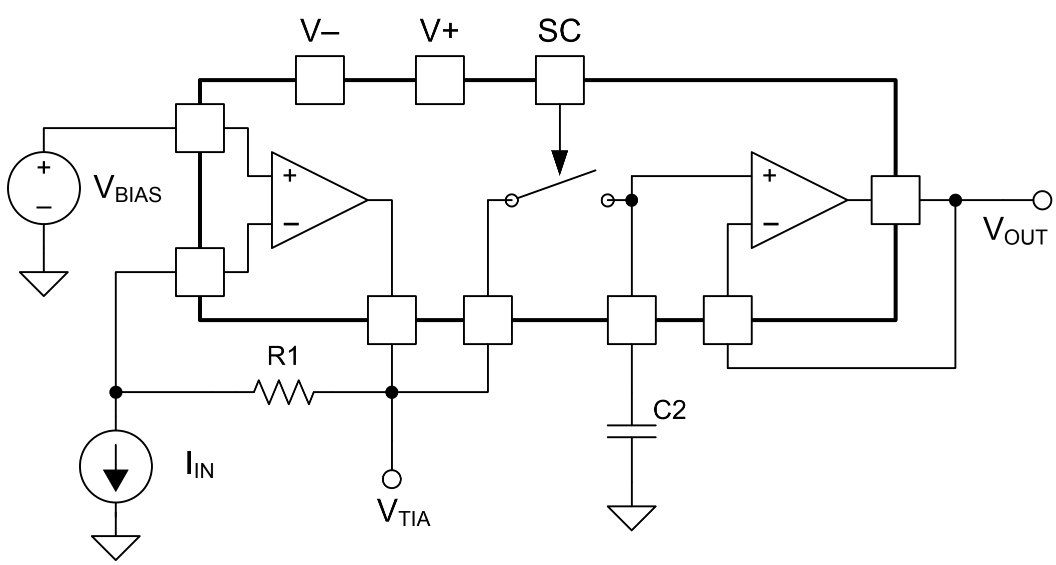


Figure 27. Signal Strength Detection

Sample and Hold

The OPA1S238x can be used in a basic sample-and-hold configuration. Figure 28 shows the simplified circuit for this application.

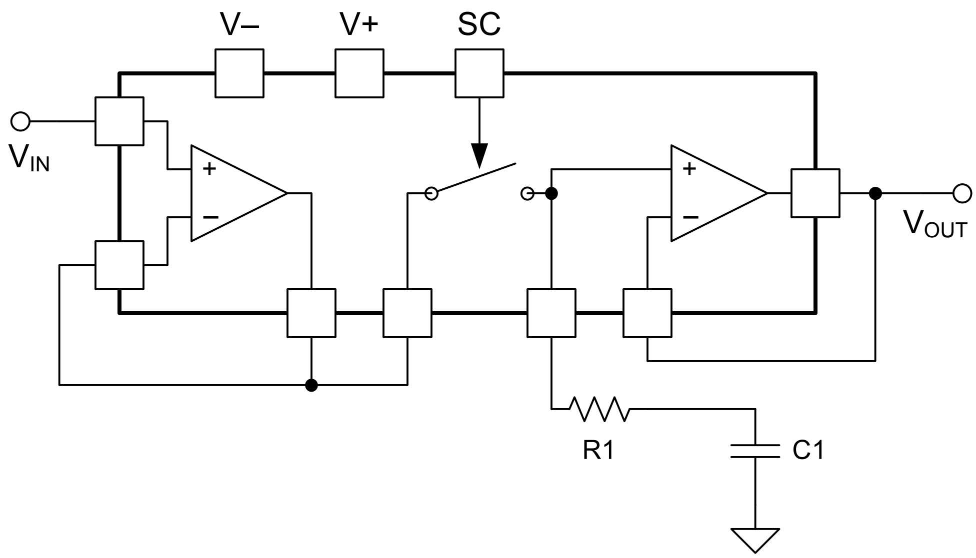


Figure 28. Sample-and-Hold Circuit

This sample-and-hold circuit can be used to sample the V_{IN} voltage at a specific point in time and hold it at V_{OUT}. This functionality is especially useful when fast-moving signals must be digitized.

When the switch connecting the two op amps is closed, the circuit operates in *track mode*. In track mode, if ideal components are assumed, the voltage at V_{OUT} follows the voltage at V_{IN}, only delayed by a filter consisting of R1 and C1.

As soon as the internal switch is opened, the output voltage no longer follows the input voltage. If ideal components are assumed again, the change in C1 remains constant and voltage at V_{OUT} reflects the voltage at V_{IN} at the moment that the switch was opened.

The values of R1 and C1 must be chosen depending on the bandwidth of the input signal, the sample time, and the hold time. Long hold times require larger capacitors in order to reduce the error from any leakage currents coming out of C1. Short sample times require smaller capacitors to allow for fast settling. Choose the R1 value according to Figure 12 to prevent ringing or excessive damping.

There are several error sources that should be considered when designing a sample-and-hold circuit. The most important ones are:

- **Aperture Time** is the time required for a switch to open and remove the charging signal from the capacitor after the mode control signal has changed from sample to hold.
- **Effective Aperture Time** is the difference in propagation delay times of the analog signal and the mode control signal from their respective input pins to the switch.
- **Charge Offset** is the output voltage change that results from a charge transfer into the hold capacitor through stray capacitance when Hold mode is enabled.
- **Droop Rate** is the change in output voltage over time during Hold mode as a result of hold capacitor leakage, switch leakage, and bias current of the output amplifier.
- **Drift Current** is the net leakage current affecting the hold capacitor during Hold mode.
- **Hold Mode Feedthrough** is the fraction of the input signal that appears at the output while in Hold mode. It is primarily a function of switch capacitance, but may also be increased by poor layout practices.
- **Hold Mode Settling Time** is the time required for the sample-to-hold transient to settle within a specified error band.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
OPA1S2385IDRCR	PREVIEW	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OUZQ	
OPA1S2385IDRCT	PREVIEW	SON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OUZQ	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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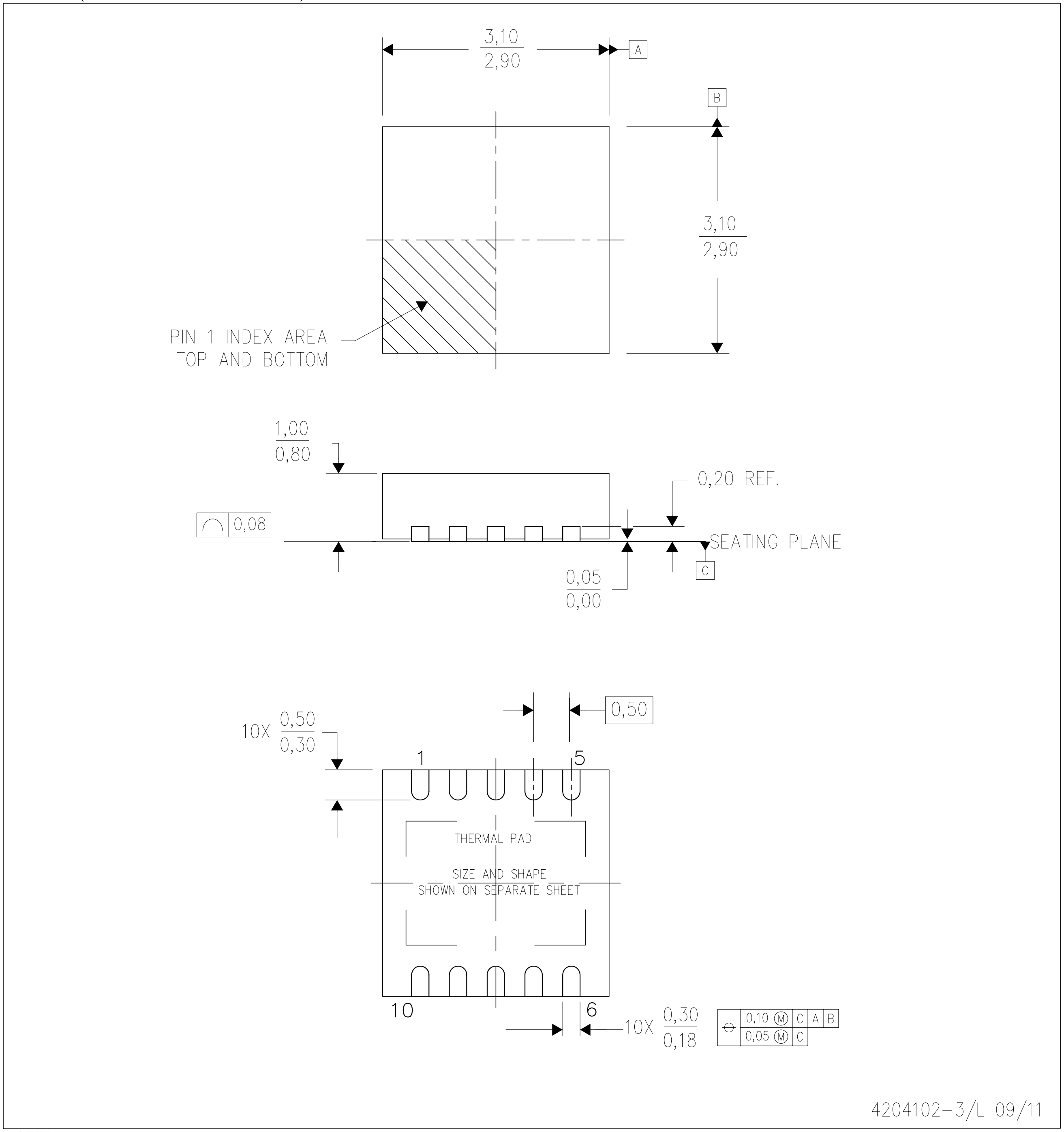
DRC (S-PVSON-N10) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No-Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

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