Zerø-Drift, High-Voltage, Programmable Gain Instrumentation Amplifier

Check for Samples: PGA281

FEATURES

- **Wide Input Range: ±15.5 V at ±18 V Supply**
- **Binary Gain Steps: 128 V/V to 1/8 V/V**
- **Additional Scaling Factor: 1 V/V and 1⅜ V/V**
- **Low Offset Voltage: 3 μV at G = 128**
- **Near-Zero Long-Term Drift of Offset Voltage**
- **Near-Zero Gain Drift: 0.5 ppm/°C**
- **Excellent Linearity: 1.5 ppm**
- **Excellent CMRR: 140 dB**
- **High Input Impedance**
- **Very Low 1/f Noise**
- **Differential Signal Output**
- **Overload Detection**
- **TSSOP-16 Package**

APPLICATIONS

- **High-Precision Signal Instrumentation**
- **Multiplexed Data Acquisition**
- **High-Voltage Analog Input Amplifiers**
- **Universal Industrial Analog Inputs**

DESCRIPTION

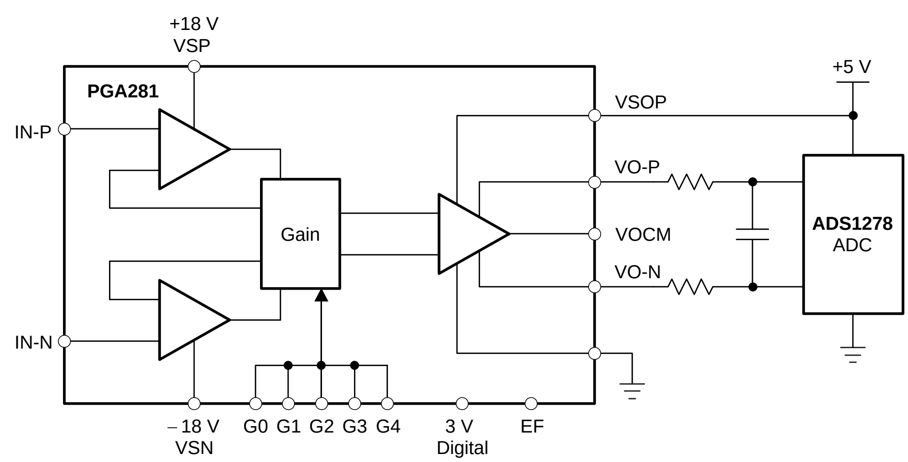
The PGA281 is a high-precision instrumentation amplifier with digitally-controllable gain and signal-integrity test capability. This device offers low offset voltage, near-zero offset and gain drift, excellent linearity, and nearly no 1/f noise, with superior common-mode and supply rejection to support high-resolution, precision measurement. The 36-V supply capability and wide, high-impedance input range comply with requirements for universal signal measurement.

The PGA281 is available in a TSSOP-16 package and is specified over a temperature range of –40°C to +105°C.

RELATED PRODUCTS

FEATURES	PRODUCT
23-bit resolution, ΔΣ analog-to-digital converter	ADS1259
Chopper-stabilized instrumentation amplifier, RR I/O, 5-V single supply	INA333
High-precision PGA, G = 1, 10, 100, and 1000	PGA204
High-precision PGA, JFET input, G = 1, 2, 4, and 8	PGA206

PRODUCT PREVIEW



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
PGA281	TSSOP-16	PW	PGA281A

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		PGA281	UNIT
Supply voltage	VSN to VSP	40	V
	GND to VSOP, and GND to DVDD	6	V
Signal input terminals, voltage(2)		VSN – 0.5 to VSP + 0.5	V
Signal input terminals, current(2)		±10	mA
Output short-circuit(3)		Continuous	
Operating temperature		–55 to +140	°C
Storage temperature		–65 to +150	°C
Junction temperature		+150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM)	2000	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Terminals are diode-clamped to the power-supply (VON and VOP) rails. Signals that can swing more than 0.5 V beyond the supply rails must be current-limited.
(3) Short-circuit to GND or VSOP, respectively, GND or DVDD.

PRODUCT PREVIEW

THERMAL INFORMATION

THERMAL METRIC(1)		PGA281 PW (TSSOP) 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	TBD	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	TBD	
θ_{JB}	Junction-to-board thermal resistance	TBD	
ψ_{JT}	Junction-to-top characterization parameter	TBD	
ψ_{JB}	Junction-to-board characterization parameter	TBD	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	TBD	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, VSP = +15 V, VSN = –15 V, GND = 0 V, VSOP = 5 V, DVDD = +3 V, R_L = 2.5 kΩ to VSOP / 2 = VOCM, G = 1 V/V, V_{CM} = 0 V, and differential input and output, unless otherwise noted.

PARAMETER		TEST CONDITIONS	PGA281 MIN	PGA281 TYP	PGA281 MAX	UNIT
INPUT						
V_{OS}	Offset voltage, RTI (1)	Gain = 1 V/V or 1.375 V/V		±50	±250	µV
		Gain = 128 V/V		±3	±15	µV
dV_{OS}/dT	vs Temperature (2)	Gain = 1 V/V, T_A = –40°C to +105°C		±0.2	±0.6	µV/°C
		Gain = 128 V/V, T_A = –40°C to +105°C		±0.03	±0.17	µV/°C
PSR	vs Power supply, RTI	VSP – VSN = 10 V and 36 V, gain = 1 V/V, 128 V/V		±0.3	±3	µV/V
	Long-term stability (3)	Gain = 128 V/V		3.5		nV/month
	Input impedance	Single-ended and differential		>1		GΩ
	Input capacitance	Single-ended (SE)		12		pF
	Input voltage range	Gain = 1 V/V, gain = 128 V/V T_A = –40°C to +105°C	(VSN) + 2.5		(VSP) – 2.5	V
CMR	Common-mode rejection, RTI	Gain = 1 V/V		±0.3	±3	µV/V
		Gain = 128 V/V		±0.08	±0.8	µV/V
		Gain = 128 V/V, T_A = –40°C to +105°C		±0.1	±1.5	µV/V
SINGLE-ENDED OUTPUT CONNECTION (4)						
V_{OS}	Offset voltage, RTI, SE out	Gain = 1 V/V, 1.375 V/V, SE		±120		µV
		Gain = 128 V/V, SE		±3		µV
dV_{OS}/dT	vs Temperature, SE out	Gain = 1 V/V, SE, T_A = –40°C to +105°C		0.6		µV/°C
		Gain = 64 V/V, SE, T_A = –40°C to +105°C		0.05		µV/°C
INPUT BIAS CURRENT (5)						
I_B	Bias current	Gain = 1 V/V		±0.3	±1	nA
		Gain = 128 V/V		±0.8	±2	nA
		Gain = 1 V/V, gain = 128 V/V T_A = –40°C to +105°C		±0.6	±2	nA
I_{OS}	Offset current	Gain = 1 V/V, gain = 128 V/V		±0.1	±0.5	nA
		Gain = 1 V/V, gain = 128 V/V T_A = –40°C to +105°C		±0.9	±2	nA
NOISE						
e_{NI}	Voltage noise, RTI; target	f = 0.01 Hz to 10 Hz, R_S = 0 Ω, gain = 128 V/V		420		nV_{PP}
		f = 1 kHz, R_S = 0 Ω, gain = 128 V/V		22		$nV/\sqrt{Hz}$
		f = 0.01 Hz to 10 Hz, R_S = 0 Ω, gain = 1 V/V		4.5		μV_{PP}
		f = 1 kHz, R_S = 0 Ω, gain = 1 V/V		240		$nV/\sqrt{Hz}$
I_N	Current noise, RTI	f = 0.01 Hz to 10 Hz, R_S = 10 MΩ, gain = 128 V/V		1.7		pA_{PP}
		f = 1 kHz, R_S = 10 MΩ, gain = 128 V/V		90		$fA/\sqrt{Hz}$

(1) RTI: Referred to input.
(2) Specified by design; not production tested.
(3) 300-hour life test at +150°C demonstrated randomly distributed variation in the range of measurement limits.
(4) For single-ended (SE) output mode, see TBD section and typical characteristic graphs; signal between VOP and VOCM.
(5) See TBD section and typical characteristic graphs.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

At T_A = +25°C, VSP = +15 V, VSN = –15 V, GND = 0 V, VSOP = 5 V, DVDD = +3 V, R_L = 2.5 kΩ to VSOP / 2 = VOCM, G = 1 V/V, V_{CM} = 0 V, and differential input and output, unless otherwise noted.

	PARAMETER	TEST CONDITIONS	PGA281 MIN	TYP	MAX	UNIT
GAIN (Output Swing = ±4.5 V(6))						
	Range of input gain		⅛		128	V/V
	Output gain			1 or 1⅜		V/V
	Gain error, all binary steps	All gains		±0.03%	±0.15%	
		T_A = –40°C to +105°C, no load, all gains except gain = 128 V/V(7) (8)		-0.5	±2	ppm/°C
		T_A = –40°C to +105°C, no load, gain = 128 V/V(7)(8)		-1	±3	ppm/°C
	Gain step matching(9) (gain to gain)	No load, all gains		See TBD		
	Nonlinearity	No load, all gains(10)		1.5	10	ppm
		No load, all gains, T_A = –40°C to +105°C(7)		3		ppm
OUTPUT						
	Voltage Output Swing from Rail(9)	VSOP = 5 V, load current 2 mA T_A = –40°C to +105°C		40	100	mV
		VSOP = 2.7 V, load current 1.5 mA T_A = –40°C to +105°C			100	mV
	Capacitive load drive			500		pF
I_{SC}	Short-circuit current	To VSOP / 2, gain = 1.375 V/V	7	15	25	mA
	Output Resistance	Both VOP and VON outputs		200		mΩ
VOCM						
	Voltage range for VOCM	VSP – 2 V > VOCM, T_A = –40°C to +105°C	(GND) + 0.1		(VSOP) – 0.1	V
$I_{B(VOCM)}$	Bias current into VOCM			3	100	nA
	VOCM input resistance			1		GΩ
FREQUENCY RESPONSE						
GBP	Gain bandwidth product(9)	Gain > 4 V/V		6		MHz
SR	Slew rate(9), 4 V_{PP} output step	Gain = 1 V/V, C_L = 100 pF		1		V/µs
		Gain = 8 V/V, C_L = 100 pF		2		V/µs
		Gain = 128 V/V, C_L = 100 pF		1		V/µs
t_S	Settling time(9)	To 0.01%, gain = 8 V/V, V_O = 8-V_{PP} step		20		µs
		To 0.001%, gain = 8 V/V, V_O = 8-V_{PP} step		30		µs
		To 0.01%, gain = 128 V/V, V_O = 8-V_{PP} step		40		µs
		To 0.001%, gain = 128 V/V, V_O = 8-V_{PP} step		40		µs
	Overload recovery, input(9)	0.5 V over supply, gain = ⅛ V/V to 128 V/V		8		µs
	Overload recovery, output(9)	±5.5-V_{PP} input, gain = 1 V/V		6		µs

(6) Gains smaller than ½ are measured with smaller output swing.
(7) Specified by design; not production tested.
(8) See TBD for typical gain error drift of various gain settings.
(9) See TBD section and typical characteristic graphs.
(10) Only gain = 1 is production tested.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

At T_A = +25°C, VSP = +15 V, VSN = –15 V, GND = 0 V, VSOP = 5 V, DVDD = +3 V, R_L = 2.5 kΩ to VSOP / 2 = VOCM, G = 1 V/V, V_{CM} = 0 V, and differential input and output, unless otherwise noted.

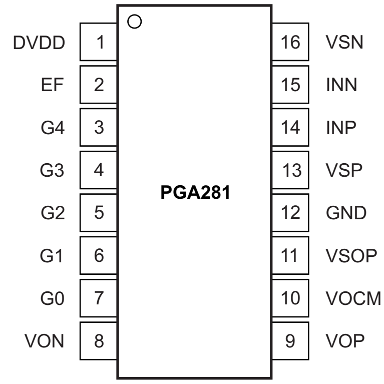
	PARAMETER	TEST CONDITIONS	PGA281 MIN	TYP	MAX	UNIT
DIGITAL I/O (Supply = 2.7 V to 5.5 V)						
	Input (logic low threshold)		0		0.2(DVDD)	V
	Input (logic high threshold)		0.8(DVDD)		DVDD	V
	Output (logic low)	I_{OUT} = 4 mA, sink			0.7	V
	Output (logic high)	I_{OUT} = 2 mA, source	DVDD – 0.5			V
POWER SUPPLY: Input Stage (VSN – VSP)						
	Specified Voltage Range	T_A = –40°C to +105°C	10		36	V
	Operating voltage range		10		38	V
$I_{Q(VSP)}$	Quiescent current , VSP pin	T_A = –40°C to +105°C		2.4	3	mA
$I_{Q(VSN)}$	Quiescent current, VSN pin	T_A = –40°C to +105°C		2.1	3	mA
POWER SUPPLY: Output Stage (VSOP – GND)						
	Specified Voltage Range	VSP – 1.5 V ≥ VSOP, T_A = –40°C to +105°C	2.7		5.5	V
	Voltage range for VSOP, upper limit	(VSP – 2 V) > VOCM, (VSP – 5 V) > GND		(VSP)		V
	Voltage range for GND	(VSP – 2 V) > VOCM, VSP ≥ VSOP	(VSN)		(VSP) – 5	V
$I_{Q(VSOP)}$	Quiescent current, VSOP pin	T_A = –40°C to +105°C		0.75	1	mA
POWER SUPPLY: Digital (DVDD – GND)						
	Specified voltage range	T_A = –40°C to +105°C	2.7		5.5	V
	Voltage range for DVDD, upper limit			(VSP) – 1		V
	Voltage range for GND, lower limit			(VSN)		V
$I_{Q(DVDD)}$	Quiescent current[11]	Static condition, no external load, DVDD = 3 V, T_A = –40°C to +105°C		0.07	0.13	mA
TEMPERATURE						
	Specified range		–40		+105	°C
	Operating range		–55		+140	°C

(11) See TBD section and typical characteristic graphs.

PRODUCT PREVIEW

PIN CONFIGURATION

TSSOP-16
PW PACKAGE
(TOP VIEW)



PIN DESCRIPTIONS

PIN		DESCRIPTION	PIN		DESCRIPTION
NAME	NUMBER		NAME	NUMBER	
DVDD	1	Digital supply	INN	15	Signal input, inverting
EF	2	Error flag (out)	INP	14	Signal input, noninverting
GND	12	Ground	VOCM	10	Input, output common-mode voltage
G0	7	Gain option 1 (see Table 1)	VON	8	Inverting signal output
G1	6	Gain option 2 (see Table 1)	VOP	9	Noninverting signal output
G2	5	Gain option 3 (see Table 1)	VSOP	11	Positive supply for output
G3	4	Gain option 4 (see Table 1)	VSN	16	Negative high-voltage supply
G4	3	Gain option 5 (see Table 1)	VSP	13	Positive high-voltage supply

Table 1. Gain Control

G3:G0	G4 = 0	G4 = 1
0000	0.125	0.172
0001	0.25	0.344
0010	0.5	0.688
0011	1	1.375
0100	2	2.75
0101	4	5.5
0110	8	11
0111	16	22
1000	32	44
1001	64	88
1010	128	176
1011	0.125	0.172
1100	0.125	0.172
1101	0.125	0.172
1110	0.125	0.172
1111	0.125	0.172

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PGA281AIPW	PREVIEW	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-40 to 125	PGA 281	
PGA281AIPWR	PREVIEW	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-40 to 125	PGA 281	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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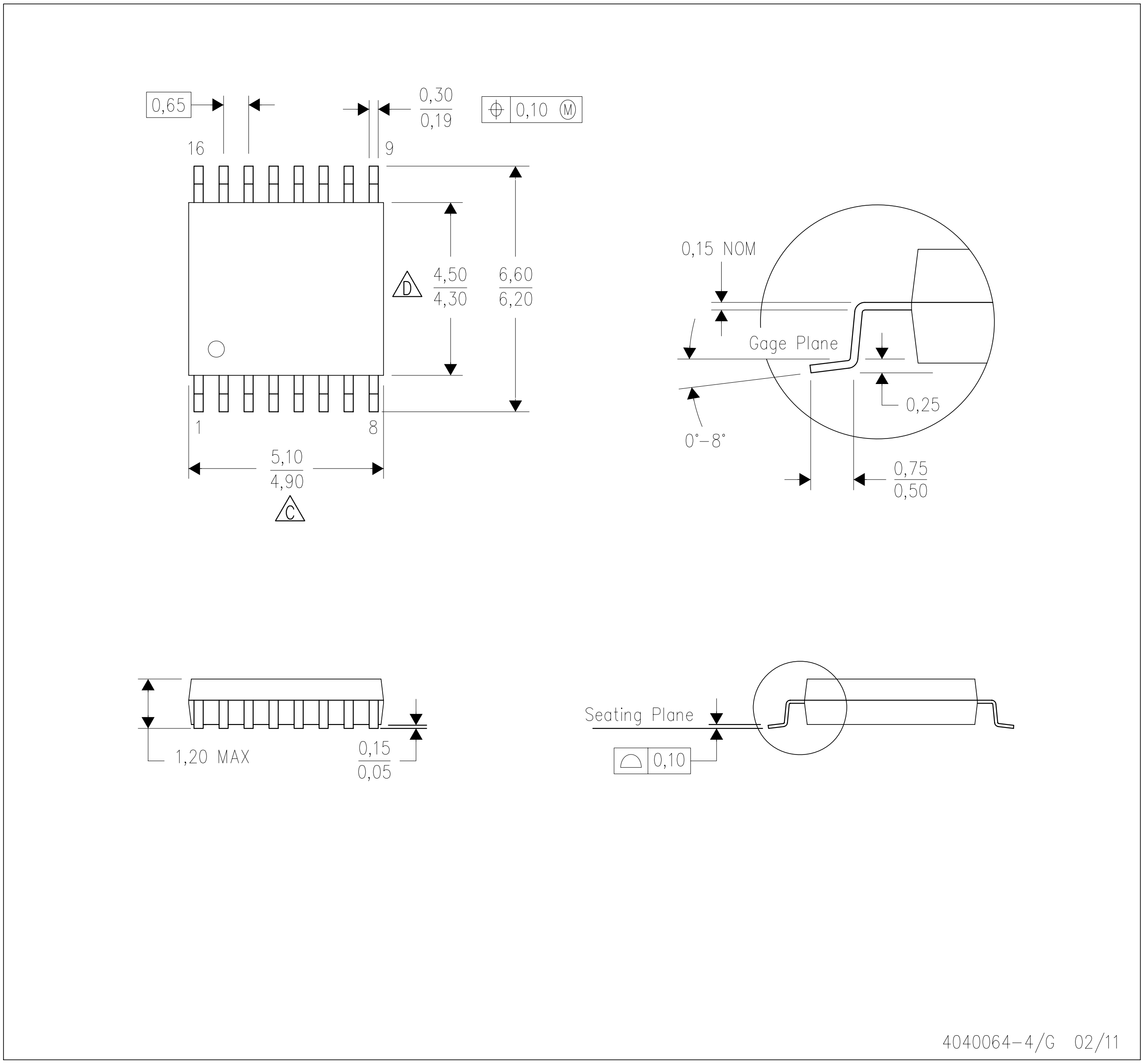
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

IMPORTANT NOTICE

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