Low-Offset, Rail-to-Rail I/O Operational Amplifier Precision Catalog

Check for Samples: OPA317, OPA2317, OPA4317

FEATURES

- **Supply Voltage: 1.8 V to 5.5 V**
- **microPackages:**
  - **Single: SOT23-5, SC-70, SOIC-8**
  - **Dual: MSOP-8, SOIC-8**
  - **Quad: SOIC-14, TSSOP-14**
- **Low Offset Voltage: 20 µV (typ)**
- **CMRR: 108 dB (typ)**
- **Quiescent Current: 35 µA (max)**
- **Gain Bandwidth: 300 kHz**
- **Rail-to-Rail Input/Output**
- **Internal EMI/RFI Filtering**

APPLICATIONS

- **Battery-Powered Instruments**
- **Temperature Measurements**
- **Transducer Applications**
- **Electronic Scales**
- **Medical Instrumentation**
- **Handheld Test Equipment**
- **Current Sense**

DESCRIPTION

The OPA317 series of CMOS operational amplifiers offer precision performance at a very competitive price. These devices are members of the Zerø-Drift family of amplifiers that use a proprietary autocalibration technique to simultaneously provide low offset voltage (90 µV max) and near-zero drift over time and temperature at only 35 µA (max) of quiescent current.

The OPA317 family features rail-to-rail input and output in addition to near flat 1/f noise, making this amplifier ideal for many applications, and much easier to design into a system. These devices are optimized for low-voltage operation as low as +1.8 V (±0.9 V) and up to +5.5 V (±2.75 V).

The OPA317 (single version) is available in the SC70-5, SOT23-5, and SOIC-8 packages. The OPA2317 (dual version) is offered in MSOP-8 and SOIC-8 packages. The OPA4317 is offered in the standard SOIC-14 and TSSOP-14 packages, as well as in the space-saving VQFN-14 package. All versions are specified for operation from –40°C to +125°C.

PRODUCT FAMILY PACKAGE COMPARISON

DEVICE	NUMBER OF CHANNELS	PACKAGE-LEADS				
		SOIC	SOT23	SC70	MSOP	TSSOP
OPA317	1	8	5	5	–	–
OPA2317	2	8	–	–	8	–
OPA4317	4	14	–	–	–	14

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE AND ORDERING INFORMATION(1)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
Supply voltage, V_S = (V+) – (V–)		+7	V
Signal input terminals, voltage(2)		(V–) –0.3 to (V+) + 0.3	V
Signal input terminals, current(2)		±10	mA
Output short-circuit(3)		Continuous	
Operating temperature		–40 to +150	°C
Storage temperature		–65 to +150	°C
Junction temperature		+150	°C
Electrostatic discharge (ESD) ratings:	Human body model (HBM)	4000	V
	Charged device model (CDM)	1000	V
	Machine model (MM)	400	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

THERMAL INFORMATION: OPA317

THERMAL METRIC[1]		OPA317			UNITS
		D (SOIC)	DBV (SOT23)	DCK (SC70)	
		8 PINS	5 PINS	5 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	140.1	220.8	298.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	89.8	97.5	65.4	
θ_{JB}	Junction-to-board thermal resistance	80.6	61.7	97.1	
ψ_{JT}	Junction-to-top characterization parameter	28.7	7.6	0.8	
ψ_{JB}	Junction-to-board characterization parameter	80.1	61.1	95.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

THERMAL INFORMATION: OPA2317

THERMAL METRIC[1]		OPA2317		UNITS
		D (SOIC)	DGK (MSOP)	
		8 PINS	8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	124.0	180.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	73.7	48.1	
θ_{JB}	Junction-to-board thermal resistance	64.4	100.9	
ψ_{JT}	Junction-to-top characterization parameter	18.0	2.4	
ψ_{JB}	Junction-to-board characterization parameter	63.9	99.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

THERMAL INFORMATION: OPA4317

THERMAL METRIC[1]		OPA4317		UNITS
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	83.8	120.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	70.7	34.3	
θ_{JB}	Junction-to-board thermal resistance	59.5	62.8	
ψ_{JT}	Junction-to-top characterization parameter	11.6	1.0	
ψ_{JB}	Junction-to-board characterization parameter	37.7	56.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS: V_S = +1.8 V to +5.5 V

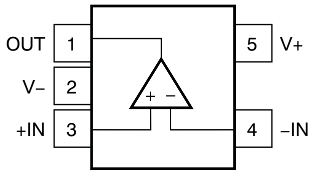
At T_A = +25°C, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA317, OPA2317, OPA4317			UNIT
			MIN	TYP	MAX	
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = +5 V		20	±90	μV
		T_A = –40°C to +125°C, V_S = +5 V			±100	μV
dV_{OS}/dT	vs temperature	T_A = –40°C to +125°C		0.05		μV/°C
PSRR	vs power supply	T_A = –40°C to +125°C, V_S = +1.8 V to +5.5 V		1	10	μV/V
	Long-term stability (1)			See (1)		
	Channel separation, dc			5		μV/V
INPUT BIAS CURRENT						
I_B	Input bias current			±275		pA
		OPA4317		±155		pA
		T_A = –40°C to +125°C		±300		pA
I_{OS}	Input offset current			±400		pA
		OPA4317		±140		pA
NOISE						
e_n	Input voltage noise density	f = 1 kHz		55		$\text{nV}/\sqrt{\text{Hz}}$
	Input voltage noise	f = 0.01 Hz to 1 Hz		0.3		μV_{PP}
		f = 0.1 Hz to 10 Hz		1.1		μV_{PP}
i_n	Input current noise	f = 10 Hz		100		$\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	T_A = –40°C to +125°C (V–) – 0.1 V < V_{CM} < (V+) + 0.1 V	95	108		dB
		OPA4317, T_A = –40°C to +125°C (V–) – 0.1 V < V_{CM} < (V+) + 0.1 V, V_S = 5.5 V	95	108		dB
INPUT CAPACITANCE						
	Differential			2		pF
	Common-mode			4		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	T_A = –40°C to +125°C, (V–) + 100 mV < V_O < (V+) – 100 mV, R_L = 10 kΩ	100	110		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product	C_L = 100 pF		300		kHz
SR	Slew rate	G = +1		0.15		V/μs
OUTPUT						
	Voltage output swing from rail	T_A = –40°C to +125°C		30	100	mV
I_{SC}	Short-circuit current			±5		mA
C_L	Capacitive load drive			See Typical Characteristics		
	Open-loop output impedance	f = 350 kHz, I_O = 0		2		kΩ
POWER SUPPLY						
V_S	Specified voltage range		1.8		5.5	V
I_Q	Quiescent current per amplifier	T_A = –40°C to +125°C, I_O = 0		21	35	μA
	Turn-on time	V_S = +5 V		100		μs
TEMPERATURE						
	Specified range		–40		+125	°C
	Operating range		–40		+150	°C
	Storage range		–65		+150	°C

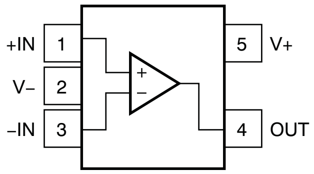
(1) 300-hour life test at +150°C demonstrated randomly distributed variation of approximately 1 μV.

PIN CONFIGURATIONS

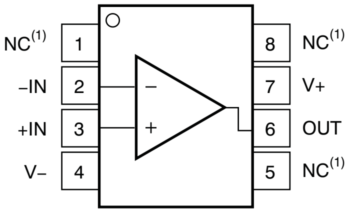
**OPA317
SOT23-5
(TOP VIEW)**



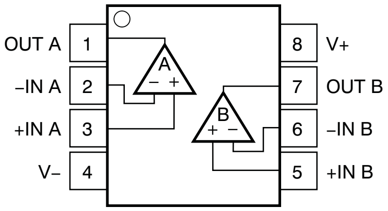
**OPA317
SC70-5
(TOP VIEW)**



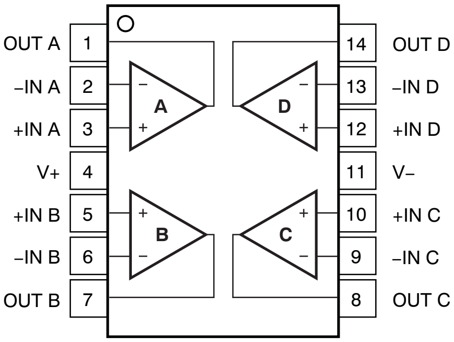
**OPA317
SOIC-8
(TOP VIEW)**



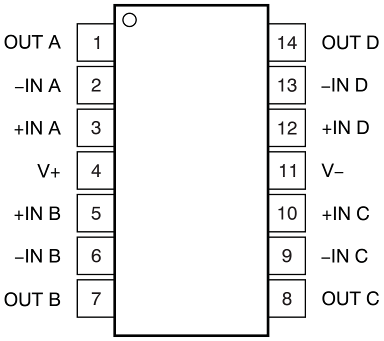
**OPA2317
SOIC-8, MSOP-8
(TOP VIEW)**



**OPA4317
SOIC-14
(TOP VIEW)**



**OPA4317
TSSOP-14
(TOP VIEW)**



TYPICAL CHARACTERISTICS

At T_A = +25°C, C_L = 0 pF, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

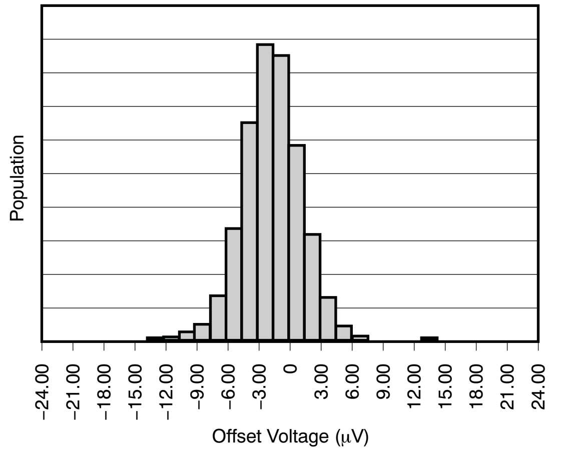


Figure 1. OFFSET VOLTAGE PRODUCTION DISTRIBUTION

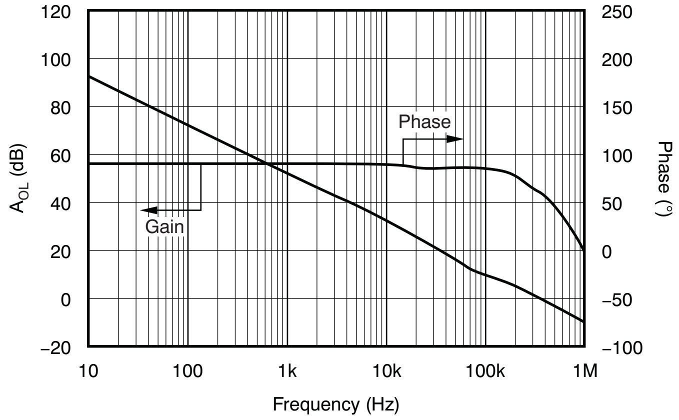


Figure 2. OPEN-LOOP GAIN vs FREQUENCY

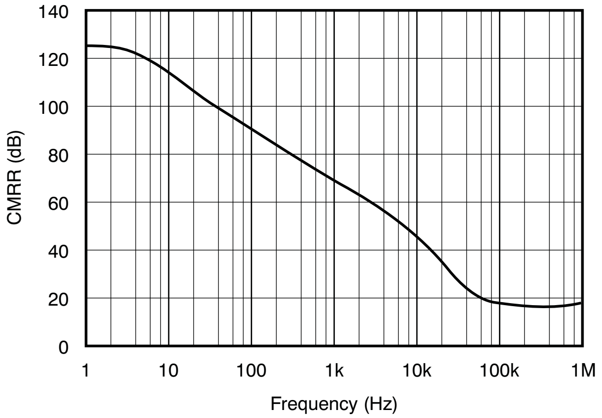


Figure 3. COMMON-MODE REJECTION RATIO vs FREQUENCY

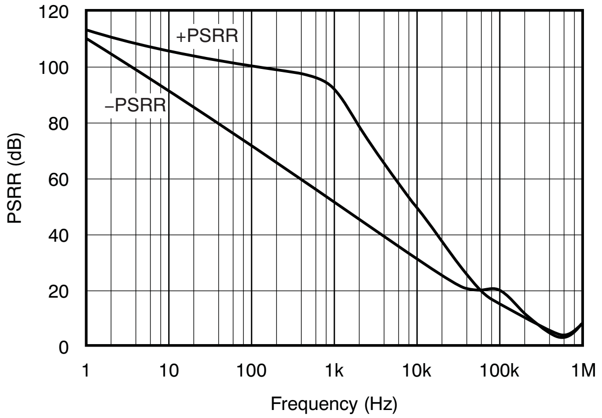


Figure 4. POWER-SUPPLY REJECTION RATIO vs FREQUENCY

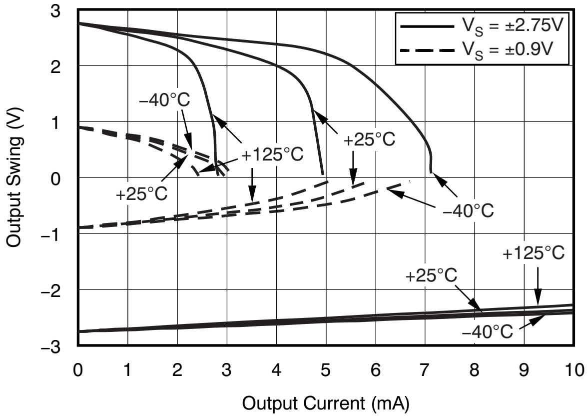


Figure 5. OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

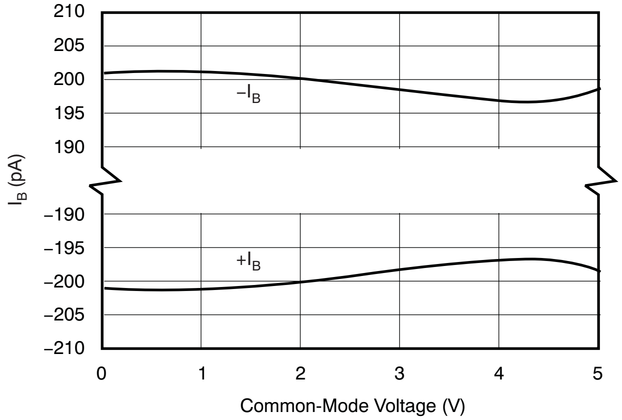


Figure 6. INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, C_L = 0 pF, R_L = 10 kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

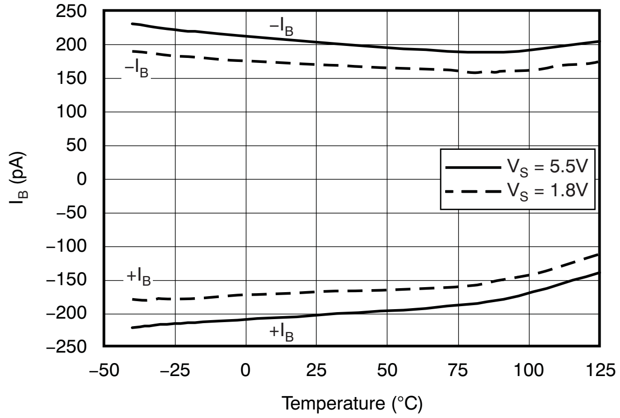


Figure 7. INPUT BIAS CURRENT vs TEMPERATURE

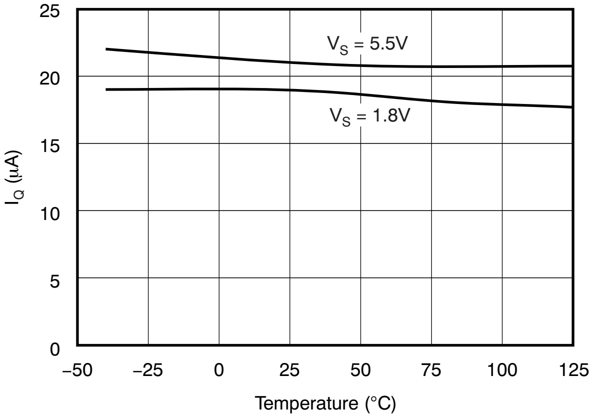


Figure 8. QUIESCENT CURRENT vs TEMPERATURE

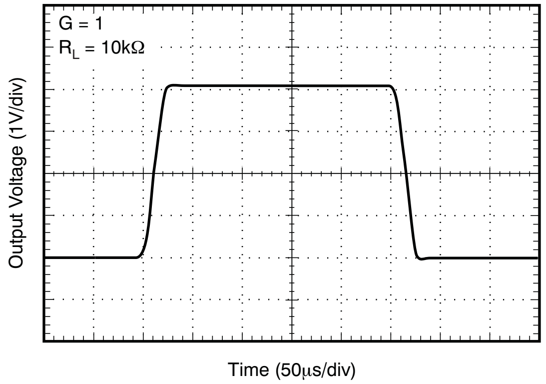


Figure 9. LARGE-SIGNAL STEP RESPONSE

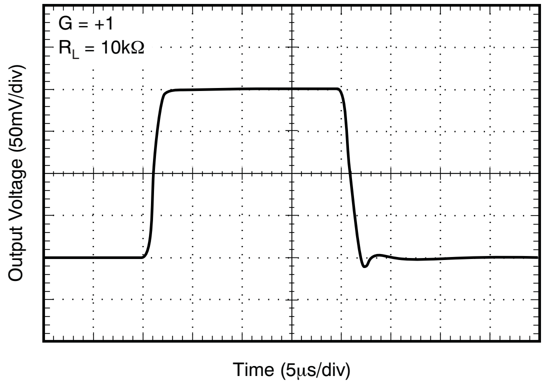


Figure 10. SMALL-SIGNAL STEP RESPONSE

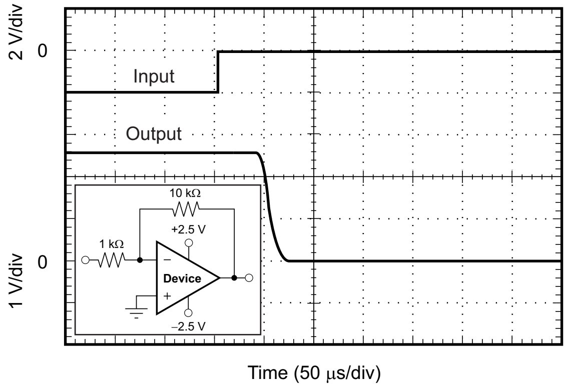


Figure 11. POSITIVE OVER-VOLTAGE RECOVERY

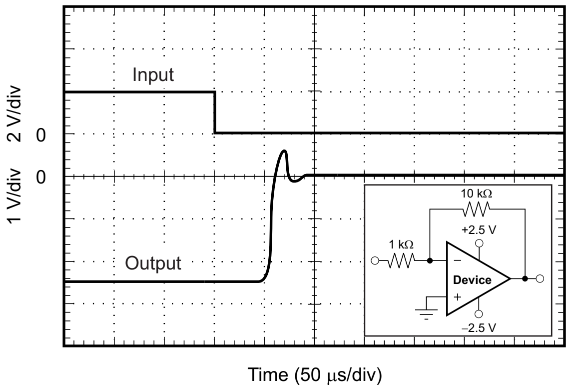


Figure 12. NEGATIVE OVER-VOLTAGE RECOVERY

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, C_L = 0 pF, R_L = 10 kΩ connected to midsupply, $V_{CM} = V_{OUT}$ = midsupply, unless otherwise noted.

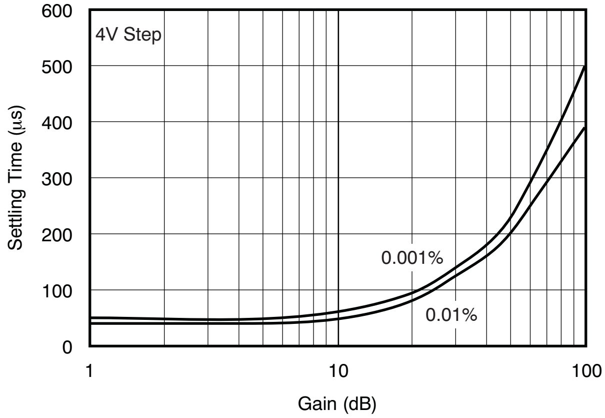


Figure 13. SETTLING TIME vs CLOSED-LOOP GAIN

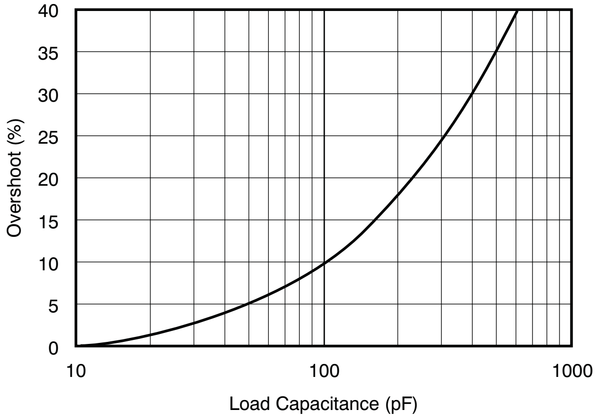


Figure 14. SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE

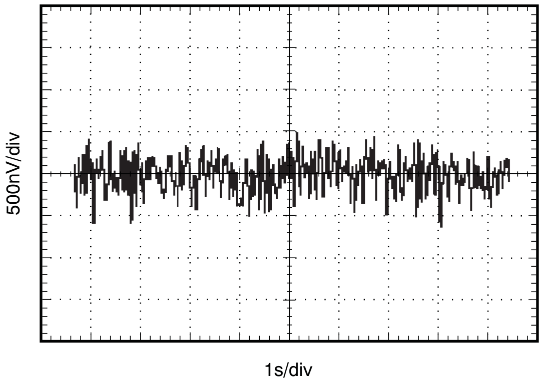


Figure 15. 0.1Hz TO 10Hz NOISE

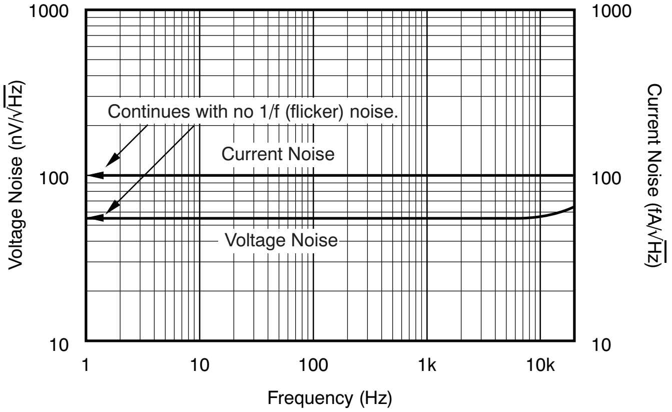


Figure 16. CURRENT AND VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

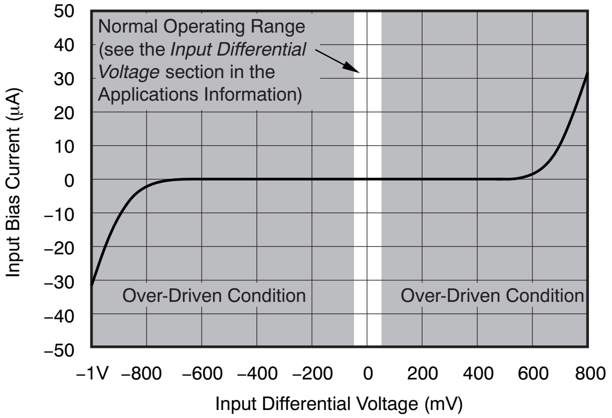


Figure 17. INPUT BIAS CURRENT vs INPUT DIFFERENTIAL VOLTAGE

APPLICATIONS INFORMATION

The OPA317, OPA2317, and OPA4317 are unity-gain stable, precision operational amplifiers free from unexpected output and phase reversal. Proprietary Zerø-Drift circuitry gives the benefit of low input offset voltage over time and temperature, as well as lowering the 1/f noise component. As a result of the high PSRR, these devices work well in applications that run directly from battery power without regulation. The OPA317 family is optimized for low-voltage, single-supply operation. These miniature, high-precision, low quiescent current amplifiers offer high-impedance inputs that have a common-mode range 100 mV beyond the supplies, and a rail-to-rail output that swings within 100 mV of the supplies under normal test conditions. The OPA317 series are precision amplifiers for cost-sensitive applications.

OPERATING VOLTAGE

The OPA317 series op amps can be used with single or dual supplies from an operating range of V_S = +1.8 V (±0.9 V) up to +5.5 V (±2.75 V).

CAUTION

Supply voltages greater than +7 V can permanently damage the device.

See the Absolute Maximum Ratings table. Key parameters that vary over the supply voltage or temperature range are shown in the *Typical Characteristics* section of this data sheet.

INPUT VOLTAGE

The OPA317, OPA2317, and OPA4317 input common-mode voltage range extends 0.1 V beyond the supply rails. The OPA317 is designed to cover the full range without the troublesome transition region found in some other rail-to-rail amplifiers.

Typically, input bias current is about 200 pA; however, input voltages exceeding the power supplies can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor, as shown in Figure 18.

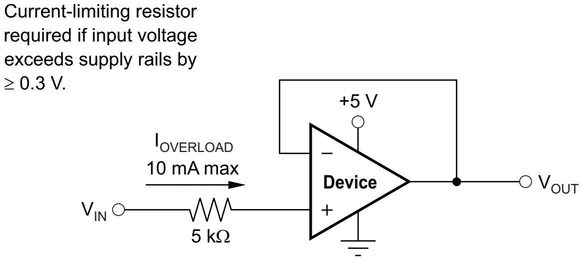


Figure 18. Input Current Protection

INPUT DIFFERENTIAL VOLTAGE

The typical input bias current of the OPA317 during normal operation is approximately 200 pA. In overdriven conditions, the bias current can increase significantly (see Figure 17).The most common cause of an overdriven condition occurs when the op amp is outside of the linear range of operation. When the output of the op amp is driven to one of the supply rails, the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front-end input chopping switches that combine with 10-kΩ electromagnetic interference (EMI) filter resistors to create the equivalent circuit shown in Figure 19. Note that the input bias current remains within specification within the linear region.

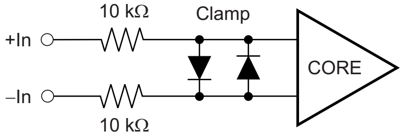


Figure 19. Equivalent Input Circuit

INTERNAL OFFSET CORRECTION

The OPA317, OPA2317, and OPA4317 op amps use an auto-calibration technique with a time-continuous, 125-kHz op amp in the signal path. This amplifier is zero-corrected every 8 µs using a proprietary technique. Upon power-up, the amplifier requires approximately 100 µs to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

EMI SUSCEPTIBILITY AND INPUT FILTERING

Operational amplifiers vary in their susceptibility to EMI. If conducted EMI enters the operational amplifier, the dc offset observed at the amplifier output may shift from its nominal value while the EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPA317 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 8 MHz (–3 dB), with a roll-off of 20 dB per decade.

ACHIEVING OUTPUT SWING TO THE OP AMP NEGATIVE RAIL

Some applications require output voltage swings from 0 V to a positive full-scale voltage (such as +2.5 V) with excellent accuracy. With most single-supply op amps, problems arise when the output signal approaches 0 V, near the lower output swing limit of a single-supply op amp. A good single-supply op amp may swing close to single-supply ground, but will not reach ground. The output of the OPA317, OPA2317, and OPA4317 can be made to swing to ground, or slightly below, on a single-supply power source. To do so requires the use of another resistor and an additional, more negative power supply than the op amp negative supply. A pull-down resistor can be connected between the output and the additional negative supply to pull the output down below the value that the output would otherwise achieve, as shown in Figure 20.

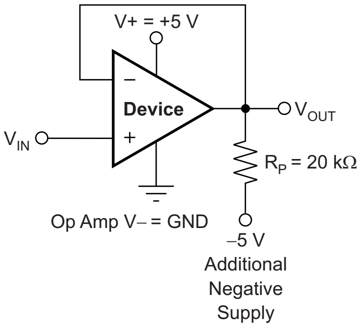


Figure 20. For V_{OUT} Range to Ground

The OPA317, OPA2317, and OPA4317 have an output stage that allows the output voltage to be pulled to its negative supply rail, or slightly below, using the technique previously described. This technique only works with some types of output stages. The OPA317, OPA2317, and OPA4317 have been characterized to perform with this technique; the recommended resistor value is approximately 20 kΩ. Note that this configuration increases the current consumption by several hundreds of microamps. Accuracy is excellent down to 0 V and as low as –2 mV. Limiting and nonlinearity occurs below –2 mV, but excellent accuracy returns as the output drives back up above –2 mV. Lowering the resistance of the pull-down resistor allows the op amp to swing even further below the negative rail. Use resistances as low as 10 kΩ to achieve excellent accuracy down to –10 mV.

APPLICATION CIRCUITS

Figure 21 shows the basic configuration for a bridge amplifier. A low-side current shunt monitor is shown in Figure 22.

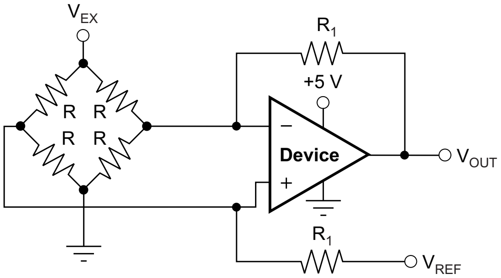
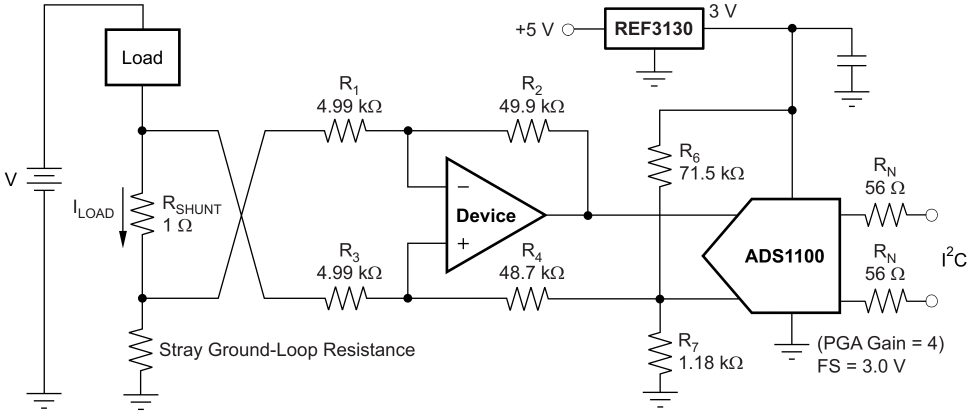


Figure 21. Single Op Amp Bridge Amplifier



NOTE: 1% resistors provide adequate common-mode rejection at small ground-loop errors.

Figure 22. Low-Side Current Monitor

R_N are operational resistors used to isolate the ADS1100 from the noise of the digital I^2C bus. The ADS1100 is a 16-bit converter; therefore, a precise reference is essential for maximum accuracy. If absolute accuracy is not required and the 5-V power supply is sufficiently stable, the REF3130 may be omitted.

Figure 23 shows the OPA317 in a typical thermistor circuit.

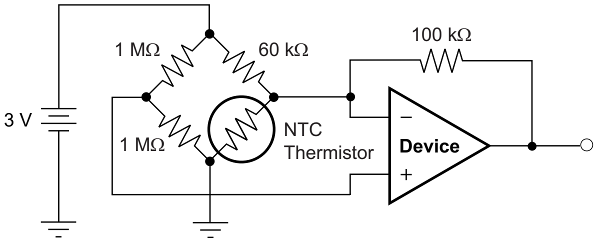


Figure 23. Thermistor Measurement

GENERAL LAYOUT GUIDELINES

Attention to good layout practice is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-µF capacitor closely across the supply pins. Apply these guidelines throughout the analog circuit to improve performance and provide benefits, such as reducing the electromagnetic interference (EMI) susceptibility.

Optimize circuit layout and mechanical conditions for lowest offset voltage and precision performance. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield op amp and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1 µV/°C or higher, depending on the materials used.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May 2013) to Revision A	Page
• Deleted *PSRR* Features bullet	1
• Changed *Quiescent Current* Features bullet	1
• Changed second sentence in Description section	1
• Changed PSSR maximum value	4

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2317ID	PREVIEW	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2317A	
OPA2317IDR	PREVIEW	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2317A	
OPA317ID	PREVIEW	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	O317A	
OPA317IDR	PREVIEW	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	O317A	
OPA4317ID	PREVIEW	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	O4317A	
OPA4317IDR	PREVIEW	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	O4317A	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

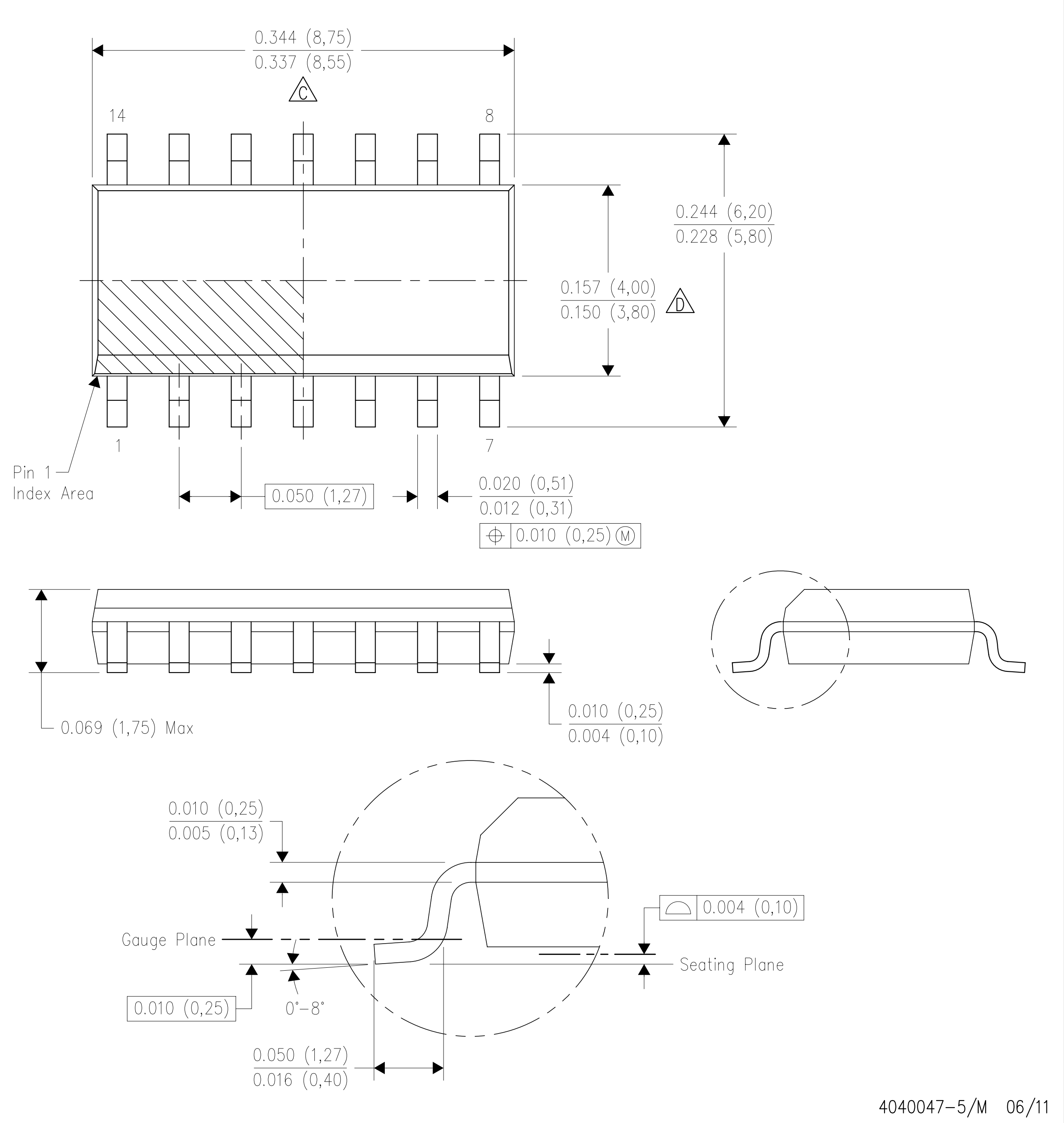
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

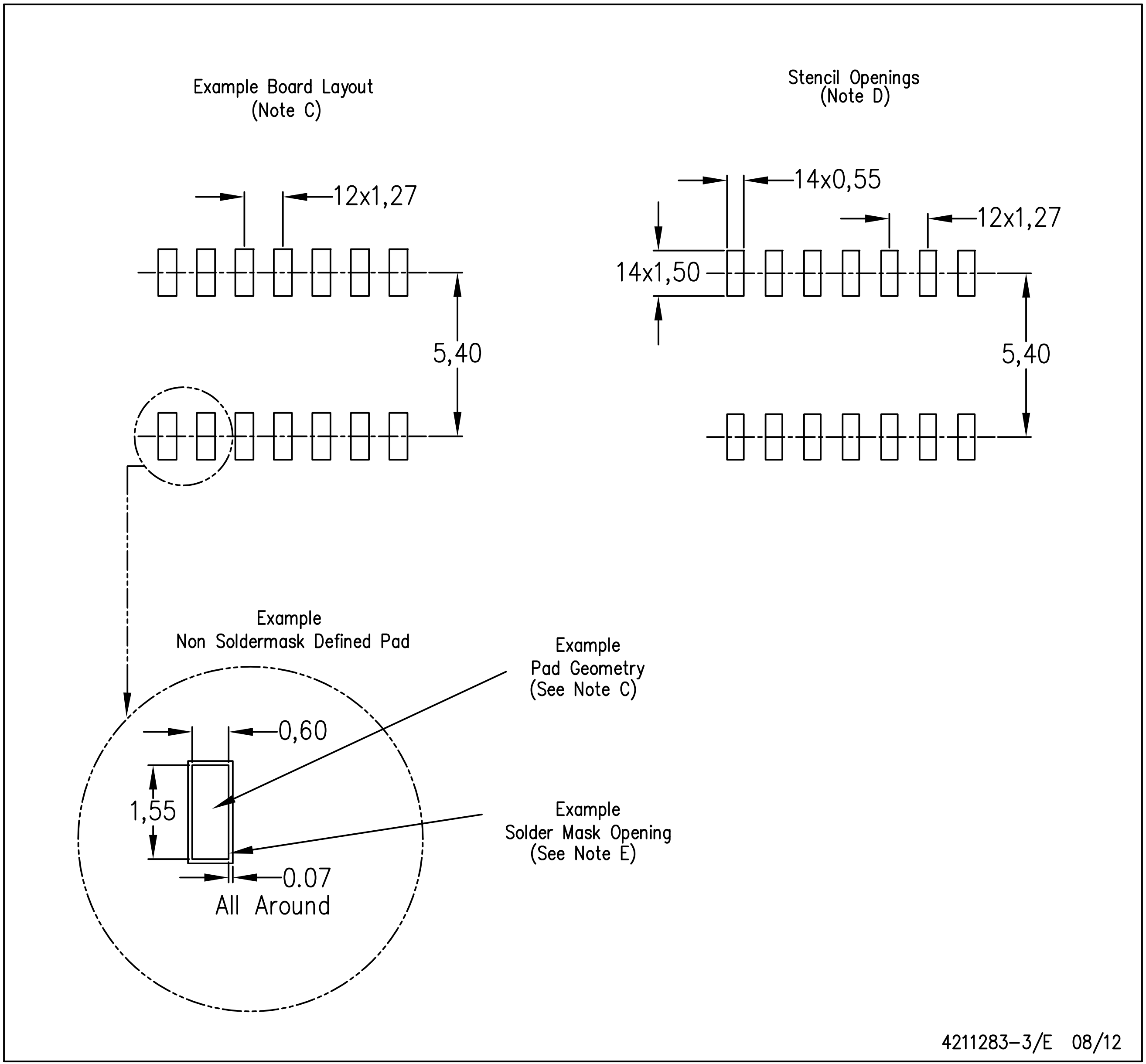
PACKAGE OPTION ADDENDUM

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



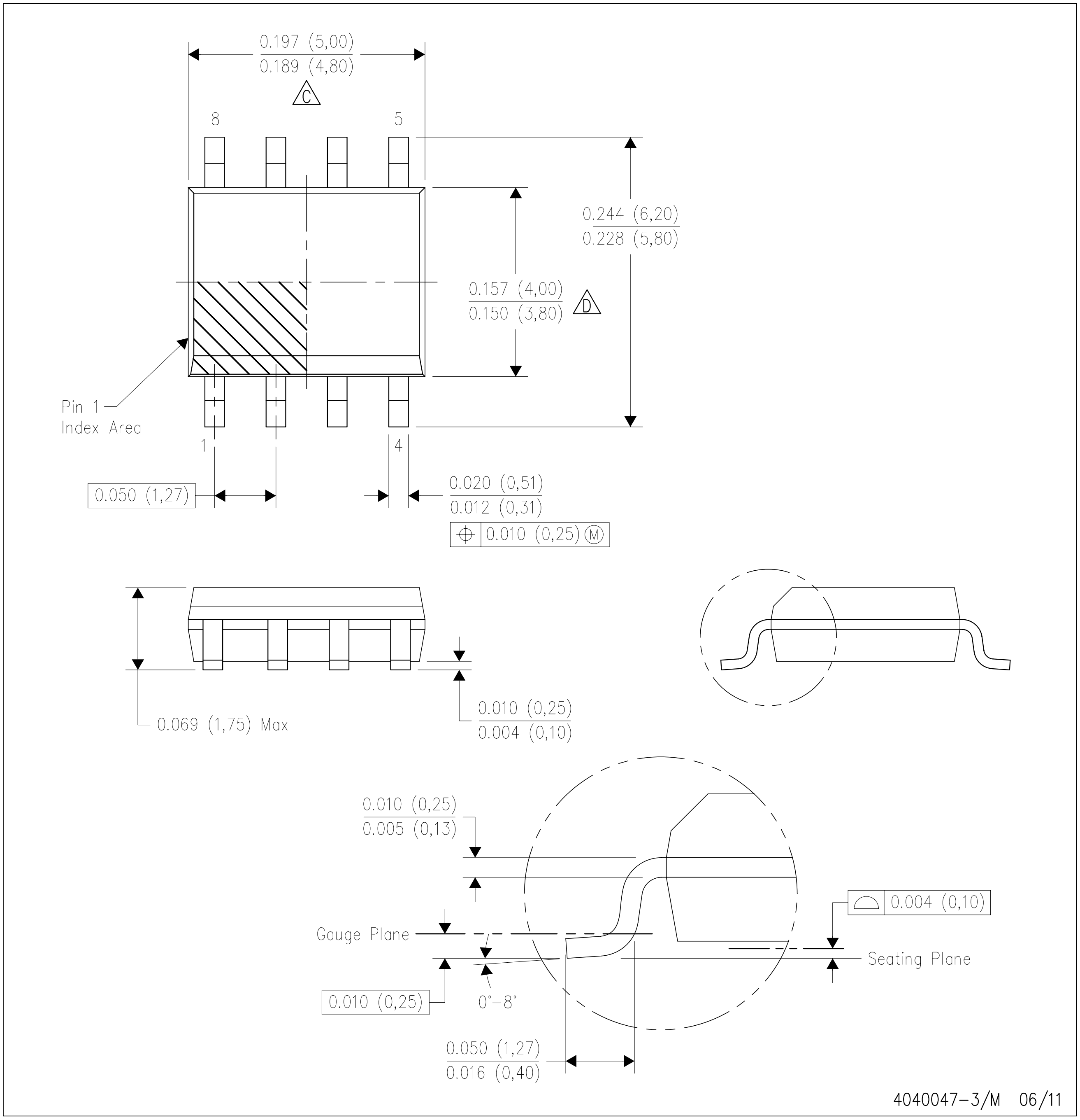
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



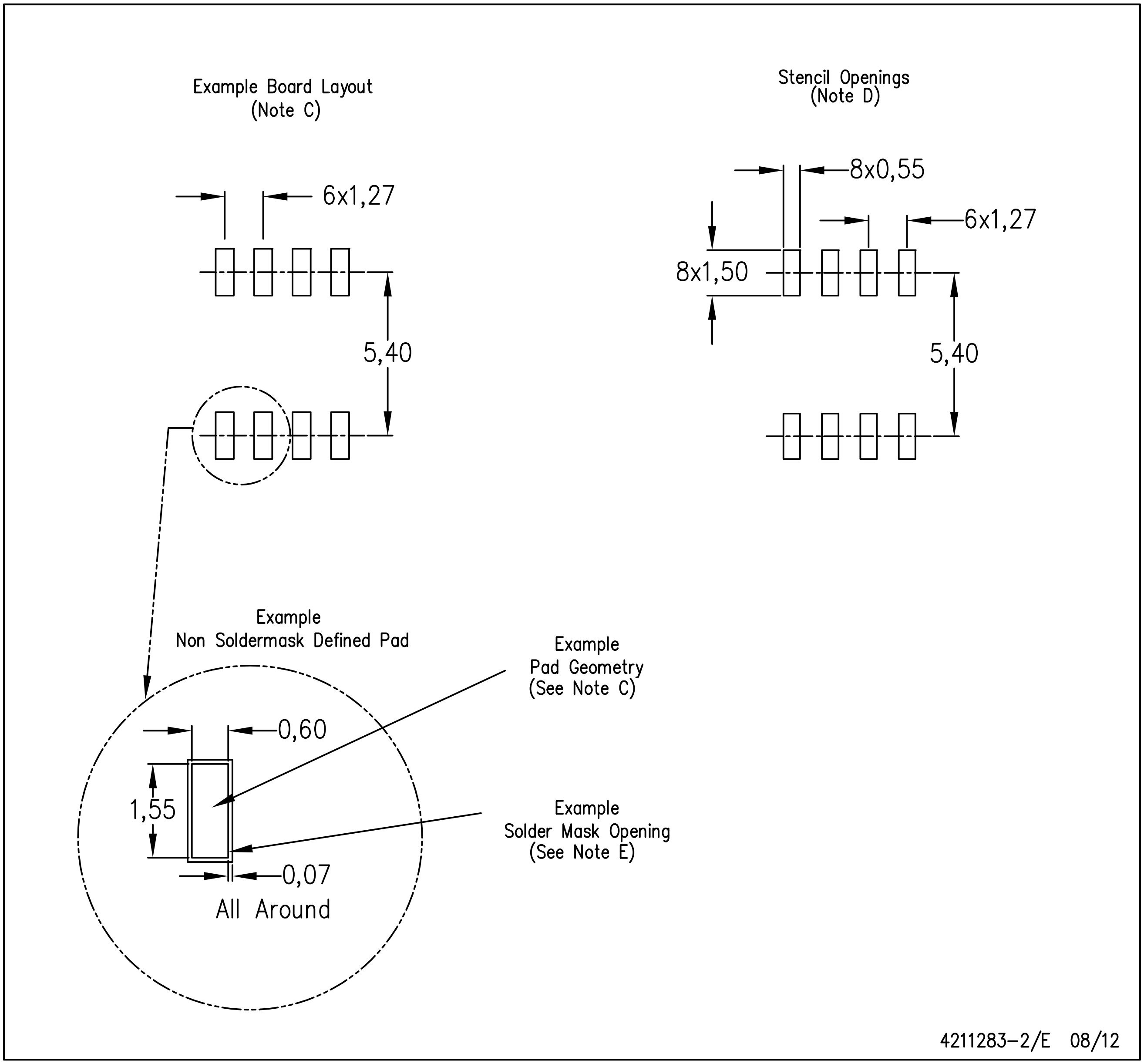
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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