



1.2A PWM High-Side Driver for Solenoids, Coils, Valves, Heaters, and Lamps

FEATURES

- **HIGH OUTPUT DRIVE: 1.2A**
- **WIDE SUPPLY RANGE: +8V to +32V**
- **COMPLETE FUNCTION:**
 PWM Output
 Adjustable Internal Oscillator: 500Hz to 100kHz
 Digitally Controlled Input
 Adjustable Delay and Duty Cycle
 Over-Current Indicator Flag
- **FULLY PROTECTED:**
 Thermal Shutdown with Indicator Flag
 Internal Current Limit
- **PACKAGE: HTSSOP-14 Surface-Mount PowerPAD™**

APPLICATIONS

- **ELECTROMECHANICAL DRIVERS:**
 Solenoids, Valves, Positioners, Actuators, Relays,
 Power Contactor Coils, Heaters, and Lamps
- **FLUID AND GAS FLOW SYSTEMS**
- **FACTORY AUTOMATION**
- **PART HANDLERS AND SORTERS**
- **PHOTOGRAPHIC PROCESSING**
- **ENVIRONMENTAL MONITORING AND HVAC**
- **THERMOELECTRIC COOLERS**
- **MOTOR SPEED CONTROLS**
- **SOLENOID PROTECTORS**
- **MEDICAL ANALYZERS**

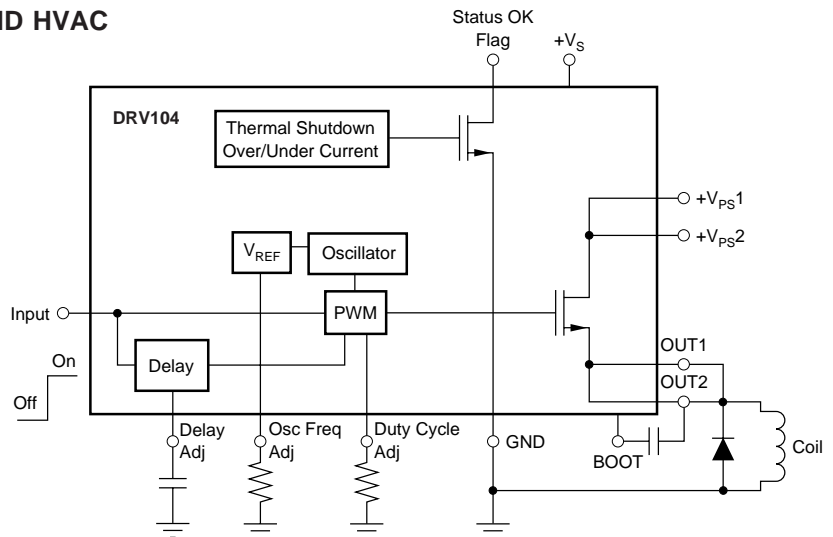
DESCRIPTION

The DRV104 is a DMOS, high-side power switch employing a pulse-width modulated (PWM) output. Its rugged design is optimized for driving electromechanical devices such as valves, solenoids, relays, actuators, and positioners. It is also ideal for driving thermal devices such as heaters, coolers, and lamps. PWM operation conserves power and reduces heat rise, resulting in higher reliability. In addition, adjustable PWM allows fine control of the power delivered to the load. Time from dc-to-PWM output and oscillator frequency are externally adjustable.

Separate supply pins for the circuit and driver transistor allow the output to operate on a different supply than the rest of the circuit.

The DRV104 can be set to provide a strong initial solenoid closure, automatically switching to a soft hold mode for power savings. The duty cycle can be controlled by a resistor, analog voltage, or a digital-to-analog (D/A) converter for versatility. The Status OK Flag pin indicates when thermal shutdown or over-current occurs.

The DRV104 is specified for -40°C to $+85^{\circ}\text{C}$ at its case. The exposed lead frame must be soldered to the circuit board.



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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage V_S , V_{PS1} , V_{PS2} ⁽²⁾	+40V
Input Voltage, Master, SYNC	-0.2V to +5.5V ⁽³⁾
PWM Adjust Input	-0.2V to +5.5V ⁽³⁾
Delay Adjust Input	-0.2V to +5.5V ⁽³⁾
Frequency Adjust Input	-0.2V to +5.5V ⁽³⁾
Status OK Flag and OUT	-0.2V to V_S ⁽⁴⁾
Boot Voltage	$V_S + 10V$
Operating Temperature Range	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Junction Temperature	+150°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) See the Bypass section for discussion about operating near the maximum supply. (3) Higher voltage may be applied if current is limited to 2mA. (4) Status OK flag will internally current limit at about 10mA.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

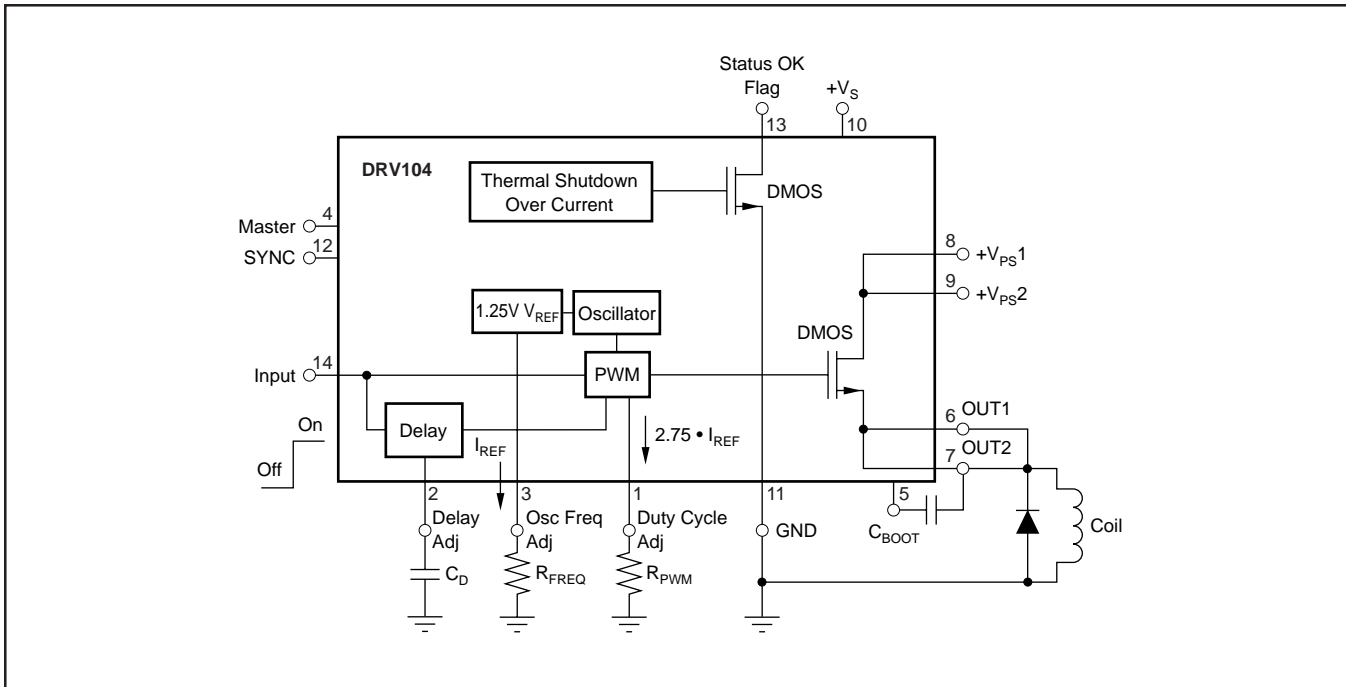
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DRV104	PowerPAD HTSSOP-14	PWP	-40°C to +85°C	DRV104	DRV104PWP	Rails, 90
"	"	"	"	"	DRV104PWPR	Tape and Reel, 2000

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this document, or see the TI web site at www.ti.com.

LOGIC BLOCK DIAGRAM



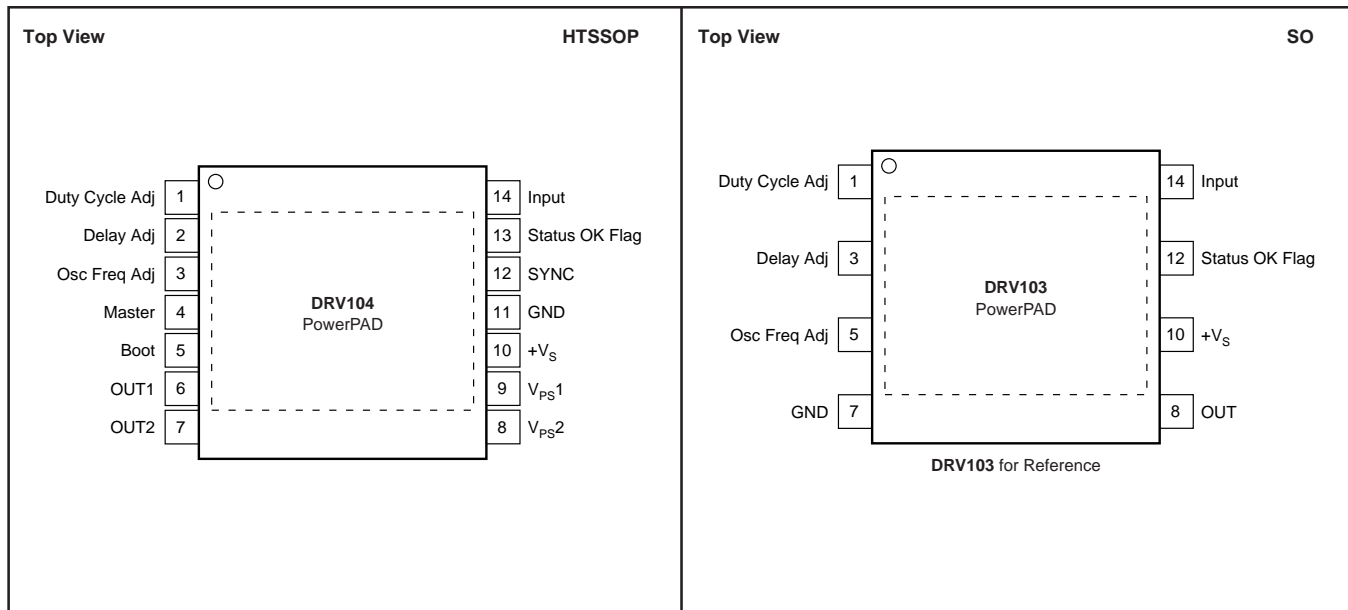
ELECTRICAL CHARACTERISTICS

At $T_C = +25^\circ\text{C}$, $V_S = V_{PS} = +24\text{V}$, Load = 100Ω , $4.99\text{k}\Omega$ Status OK flag pull-up to +5V, Boot capacitor = 470pF , Delay Adj Capacitor (C_D) = 100pF to GND, Osc Freq Adj Resistor = $191\text{k}\Omega$ to GND, Duty Cycle Adj Resistor = $147\text{k}\Omega$ to GND, and Master and SYNC open, unless otherwise noted.

PARAMETER	CONDITIONS	DRV104			UNITS
		MIN	TYP	MAX	
OUTPUT Output Saturation Voltage, Source Current Limit ⁽¹⁾⁽⁷⁾ Leakage Current	$I_O = 1\text{A}$ $I_O = 0.1\text{A}$ DMOS Output Off, $V_{PS} = V_S = 32\text{V}$	1.2	+0.45 +0.05 2.0 1	+0.65 +0.07 2.6 10	V V A μA
DELAY TO PWM ⁽³⁾ Delay Equation ⁽⁴⁾ Delay Time Minimum Delay Time ⁽⁵⁾	DC to PWM Mode $C_D = 0.1\mu\text{F}$ $C_D = 0$	Delay to PWM = $C_D \cdot 10^6$ (C_D in F \cdot 1.24) 60	80 18	100	s ms μs
DUTY CYCLE ADJUST Duty Cycle Range Duty Cycle Accuracy vs Supply Voltage Nonlinearity ⁽⁶⁾	50% Duty Cycle, 25kHz 50% Duty Cycle, $V_S = V_{PS} = 8\text{V}$ to 32V 10% to 90% Duty Cycle		10 to 90 ± 2 ± 2 1	± 5	% % % % FSR
DYNAMIC RESPONSE Output Voltage Rise Time Output Voltage Fall Time SYNC Output Rise Time SYNC Output Fall Time Oscillator Frequency Range Oscillator Frequency Accuracy	$V_O = 10\%$ to 90% of V_{PS} $V_O = 90\%$ to 10% of V_{PS} $V_{\text{SYNC}} = 10\%$ to 90% $V_{\text{SYNC}} = 10\%$ to 90% External Adjust $R_{\text{FREQ}} = 191\text{k}\Omega$		1 0.2 0.5 0.5 0.5 to 100 25	2 2 2 2	μs μs μs μs kHz kHz
STATUS OK FLAG Normal Operation Fault ⁽⁷⁾ Over-Current Flag: Set—Delay	$20\text{k}\Omega$ Pull-Up to +5V $4.99\text{k}\Omega$ Pull-Up to +5V	+4.5	+5 +0.45 5	+0.6	V V μs
INPUT ⁽²⁾ $V_{\text{INPUT Low}}$ $V_{\text{INPUT High}}$ $I_{\text{INPUT Low}}$ (output disabled) $I_{\text{INPUT High}}$ (output enabled) Propagation Delay (master mode)	$V_{\text{INPUT}} = 0\text{V}$ $V_{\text{INPUT}} = +4.5\text{V}$ On to Off and Off to On, INPUT to OUT On to Off and Off to On, INPUT to SYNC	0 +2.2	0.01 0.01 2.2 0.4	+1.2 +5.5 1 1	V V μA μA μs μs
MASTER INPUT $V_{\text{MSTR Low}}$ $V_{\text{MSTR High}}$ $I_{\text{MSTR Low}}$ (slave mode) $I_{\text{MSTR High}}$ (master mode)	$V_{\text{INPUT}} = 0\text{V}$ $V_{\text{INPUT}} = +4.5\text{V}$	0 +2.2	15 15	+1.2 +5.5 25 25	V V μA μA
SYNC INPUT $V_{\text{SYNC Low}}$ $V_{\text{SYNC High}}$ $I_{\text{MSTR Low}}$ (OUT disabled in slave mode) $I_{\text{MSTR High}}$ (OUT disabled in slave mode) Propagation Delay	$V_{\text{INPUT}} = 0\text{V}$ $V_{\text{INPUT}} = +4.5\text{V}$ On to Off and Off to On, SYNC to OUT (slave)	0 +2.2	0.01 0.01 2.2	+1.2 +5.5 1 1	V V μA μA μs
SYNC OUTPUT ⁽⁹⁾ $V_{\text{OL Sync}}$ $V_{\text{OH Sync}}$	$I_{\text{SYNC}} = 100\mu\text{A}$ (sinking) $I_{\text{SYNC}} = 100\mu\text{A}$ (sourcing)	+4.0	0.1 +4.2	0.3	V V
THERMAL SHUTDOWN Junction Temperature Shutdown Reset from Shutdown			+160 +140		$^\circ\text{C}$ $^\circ\text{C}$
POWER SUPPLY Specified Operating Voltage Operating Voltage Range Quiescent Current (V_S)	$I_O = 0$	+8	+24 0.6	+32 1	V V mA
TEMPERATURE RANGE Specified Range Operating Range Storage Range Thermal Resistance, θ_{JA} ⁽⁸⁾ HTSSOP-14 with PowerPAD		-40 -55 -65		+85 +125 +150	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}/\text{W}$

NOTES: (1) Output current resets to zero when current limit is reached. (2) Logic high enables output (normal operation). (3) Constant dc output to PWM (Pulse-Width Modulated) time. (4) Maximum delay is determined by an external capacitor. Pulling the Delay Adjust Pin low corresponds to an infinite (continuous) delay. (5) Connecting the Delay Adjust pin to +5V reduces delay time to $3\mu\text{s}$. (6) V_{IN} at pin 1 to percent of duty cycle at pins 6 and 7. (7) Flag indicates fault from over-temperature or over-current conditions. (8) $\theta_{JA} = 37.5^\circ\text{C}/\text{W}$ measured on JEDEC standard test board. $\theta_{JC} = 2.07^\circ\text{C}/\text{W}$. (9) SYNC output follows power output in master mode. Power output follows SYNC input in slave mode.

PIN CONFIGURATION

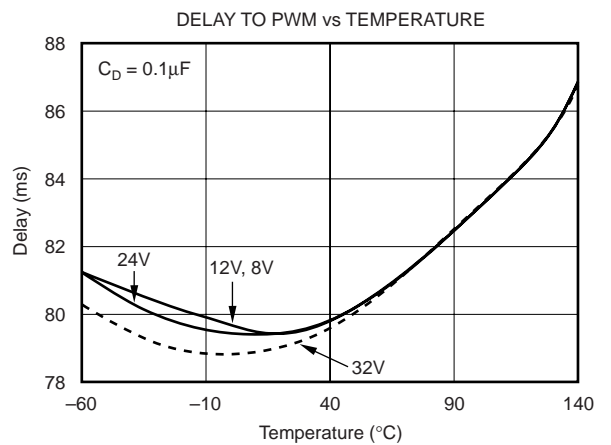
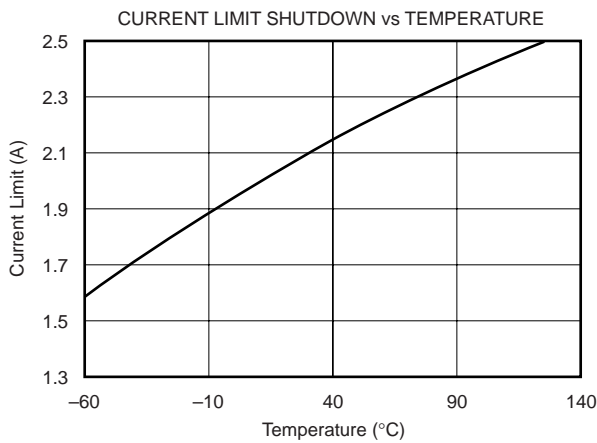
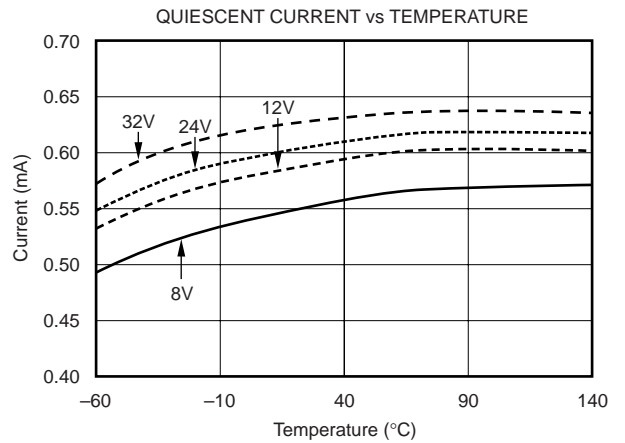
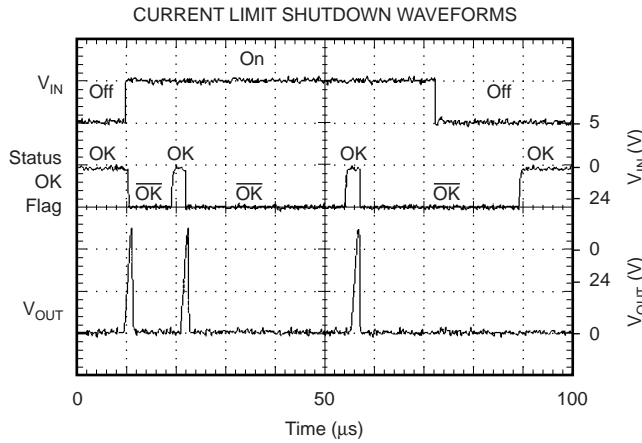
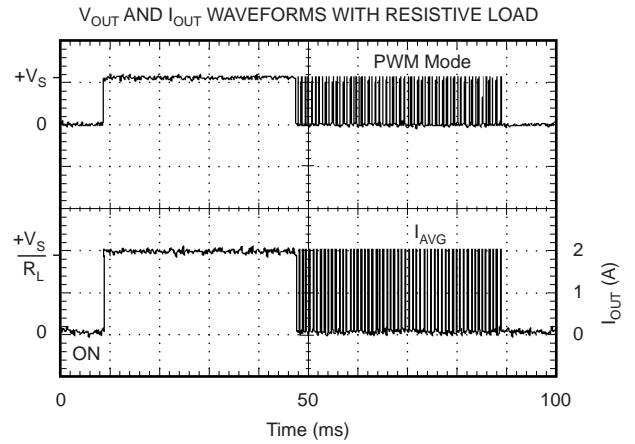
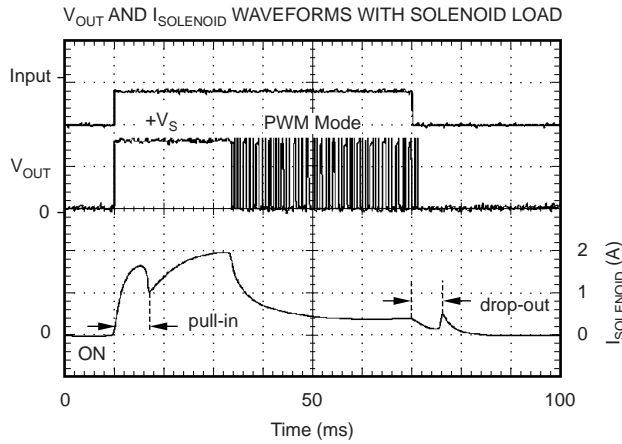


PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	Duty Cycle Adjust	Internally, this pin connects to the input of a comparator and a $(2.75 \times I_{REF})$ current source from V_S . The voltage at this node linearly sets the duty cycle. The duty cycle can be programmed with a resistor, analog voltage, or the voltage output of a D/A converter. The active voltage range is from 1.3V to 3.9V to facilitate the use of single-supply control electronics. At 3.56V, the output duty cycle is near 90%. At 1.5V, the output duty cycle is near 10%. Internally, this pin is forced to 1.24V. No connection is required when the device is in slave mode.
2	Delay Adjust	This pin sets the duration of the initial 100% duty cycle before the output goes into PWM mode. Leaving this pin floating results in a delay of approximately 18 μ s, which is internally limited by parasitic capacitance. Minimum delay may be reduced to less than 3 μ s by tying the pin to 5V. This pin connects internally to a 15 μ A current source from V_S and to a 2.6V threshold comparator. When the pin voltage is below 2.6V, the output device is 100% On. The PWM oscillator is not synchronized to the Input (pin 1), so the duration of the first pulse may be any portion of the programmed duty cycle. No connection is required when the device is in slave mode.
3	Oscillator Frequency Adjust	PWM frequency is adjustable. A resistor to ground sets the current I_{REF} and the internal PWM oscillator frequency. A range of 500Hz to 100kHz can be achieved with practical resistor values. Although oscillator frequency operation below 500Hz is possible, resistors higher than 10M Ω will be required. The pin then becomes a very high-impedance node and is, therefore, sensitive to noise pickup and PCB leakage currents. Resistor connection to this pin in slave mode sets the frequency at which current limit reset occurs.
4	Master	With no connection, this pin is driven to 5V by an internal 15 μ A current source. In this mode the device is the master and the SYNC pin becomes a 0V to 4.2V output, which is High when the power device is on. When the Master/Input is 0V, the SYNC pin is an input. In slave mode, the output follows the SYNC pin; the output is High when SYNC is High.
5	BOOT	The bootstrap capacitor between this pin and the output, supplies the charge to provide the V_{GS} necessary to turn on the power device. C_{BOOT} should be larger than 100pF. Use of a smaller C_{BOOT} may slow the output rise time, device is specified and tested with 470pF.
6, 7	OUT1, OUT2	The output is the source of a power DMOS transistor with its drain connected to V_{PS} . Its low on-resistance (0.45 Ω typ) assures low power dissipation in the DRV104. Gate drive to the power device is controlled to provide a slew-rate limited rise-and-fall time. This reduces the radiated RFI/EMI noise. A flyback diode is needed with inductive loads to conduct the load current during the off cycle. The external diode should be selected for low forward voltage and low storage time. The internal diode should not be used as a flyback diode. If devices are connected in parallel, the outputs must be connected through individual diodes. Devices are current-limit protected for shorts to ground, but not to supply.
8, 9	V_{PS1} , V_{PS2}	These are the load power-supply pins to the drain of the power device. The load supply voltage may exceed the voltage at pin 10 by 5V, but must not exceed 37V.
10	$+V_S$	This is the power-supply connection for all but the drain of the power device. The operating range is 8V to 32V.
11	GND	This pin must be connected to the system ground for the DRV104 to function. It does not carry the load current when the power DMOS device is switched on.
12	SYNC	The SYNC pin is a 0V to 4.2V copy of the output when the Master/Slave pin is High. As an output, it can supply 100 μ A with 1k Ω output resistance. At 2mA, it current limits to either 4.2V or 0V. When the Master pin is Low, it is an input and the threshold is 2V. SYNC output follows power output in master mode, and is not affected by thermal or current-limit shutdown. Power output follows SYNC input in slave mode.
13	Status OK Flag	Normally High (active Low), a Flag Low signals either an over-temperature or over-current fault. A thermal fault (thermal shutdown) occurs when the die surface reaches approximately 160°C and latches until the die cools to 140°C. This output requires a pull-up resistor and it can typically sink 2mA, sufficient to drive a low-current LED. Sink current is internally limited at 10mA, typical.
14	Input	The input is compatible with standard TTL levels. The device becomes enabled when the input voltage is driven above the typical switching threshold, 1.8V; below this level, the device is disabled. Input current is typically 1 μ A when driven High and 1 μ A when driven Low. The input should not be directly connected to the power supply (V_S) or damage will occur.

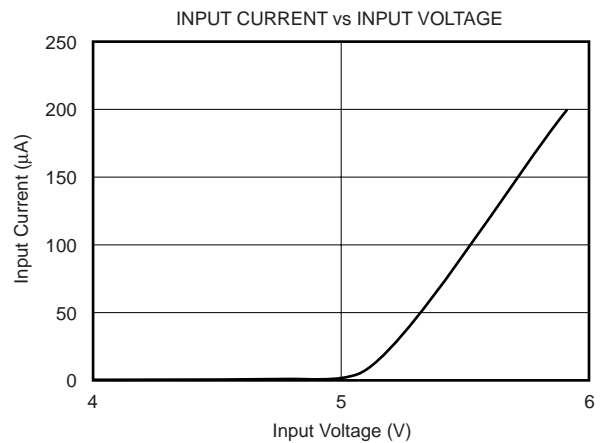
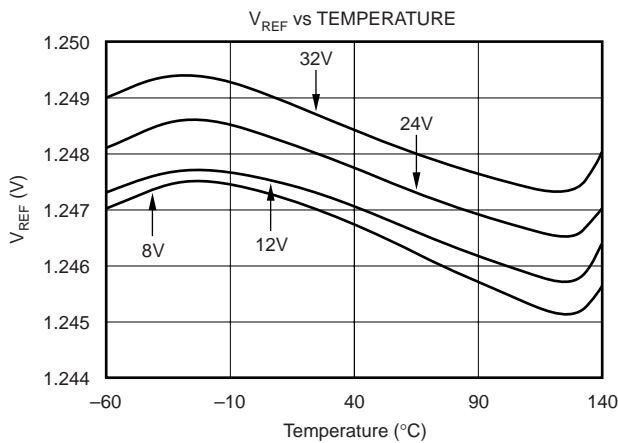
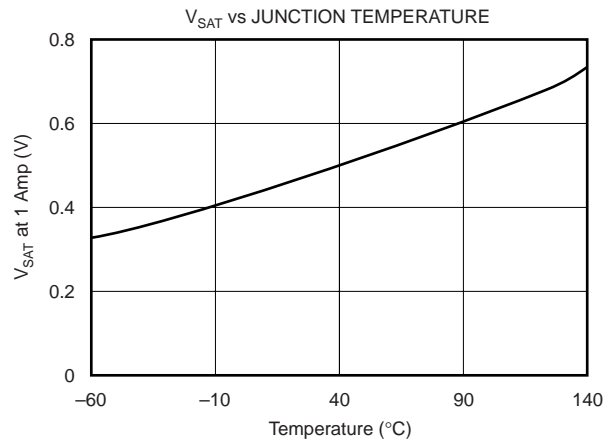
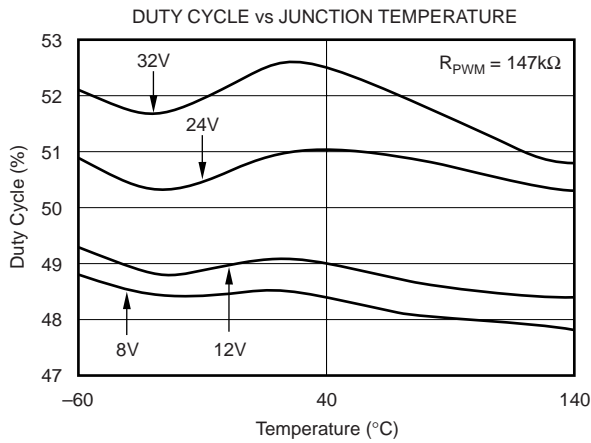
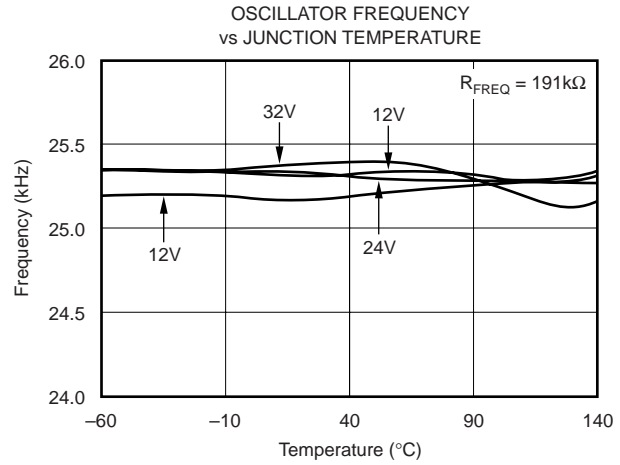
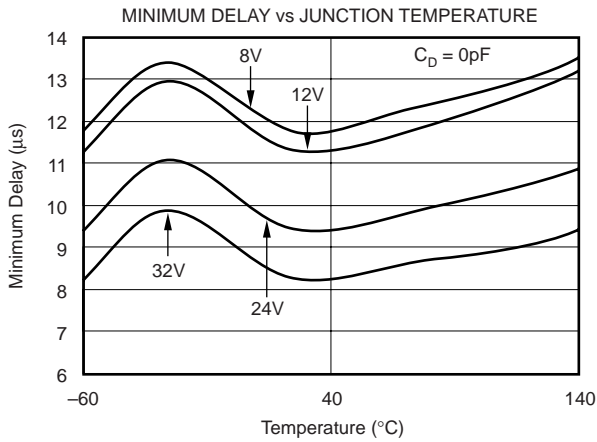
TYPICAL CHARACTERISTICS

At $T_C = +25^\circ\text{C}$ and $V_S = +24\text{V}$, unless otherwise noted.



TYPICAL CHARACTERISTICS (Cont.)

At $T_C = +25^\circ\text{C}$ and $V_S = +24\text{V}$, unless otherwise noted.



BASIC OPERATION

The DRV104 is a high-side, DMOS power switch employing a PWM output for driving electromechanical and thermal devices. Its design is optimized for two types of applications: as a 2-state driver (open/close) for loads such as solenoids and actuators; and a linear driver for valves, positioners, heaters, and lamps. Its low 0.45Ω On resistance, small size, adjustable delay to PWM mode, and adjustable duty cycle make it suitable for a wide range of applications.

Figure 1 shows the basic circuit connections to operate the DRV104. A $1\mu\text{F}$ ($10\mu\text{F}$ when driving high current loads) or larger ceramic bypass capacitor is recommended on the power-supply pin.

Control input (pin 14) is level-triggered and compatible with standard TTL levels. An input voltage between $+2.2\text{V}$ and $+5.5\text{V}$ turns the device's output On, while a voltage of 0V to $+1.2\text{V}$ shuts the DRV104's output Off. Input bias current is typically $1\mu\text{A}$. Delay Adjust (pin 2) and Duty Cycle Adjust (pin 1) allow external adjustment of the PWM output signal. The Delay Adjust pin can be left floating for minimum delay to PWM mode (typically $18\mu\text{s}$) or a capacitor can be used

to set a longer delay time. A resistor, analog voltage, or a voltage from a D/A converter can be used to control the duty cycle of the PWM output. The D/A converter must be able to sink a current of $2.75 \cdot I_{\text{REF}}$ ($I_{\text{REF}} = V_{\text{REF}}/R_{\text{FREQ}}$).

Figure 2 illustrates a typical timing diagram with the Delay Adjust pin connected to a 4.7nF capacitor, the duty cycle set to 75%, and oscillator frequency set to 1kHz . See the Adjustable and Adjustable Delay Time section for equations and further explanation. Ground (pin 11) must be connected to the system ground for the DRV104 to function. The load (relay, solenoid, valve, etc.) should be connected between the ground and the output (pins 6, 7). For an inductive load, an external flyback diode is required, as shown in Figure 1. The diode maintains continuous current flow in the inductive load during Off periods of PWM operation. For remotely located loads, the external diode is ideally located next to the DRV104. The internal ESD clamp diode between the output and ground is not intended to be used as a "flyback diode." The Status OK Flag (pin 13) provides fault status for over-current and thermal shutdown conditions. This pin is active Low with an output voltage of typically $+0.48\text{V}$ during a fault condition.

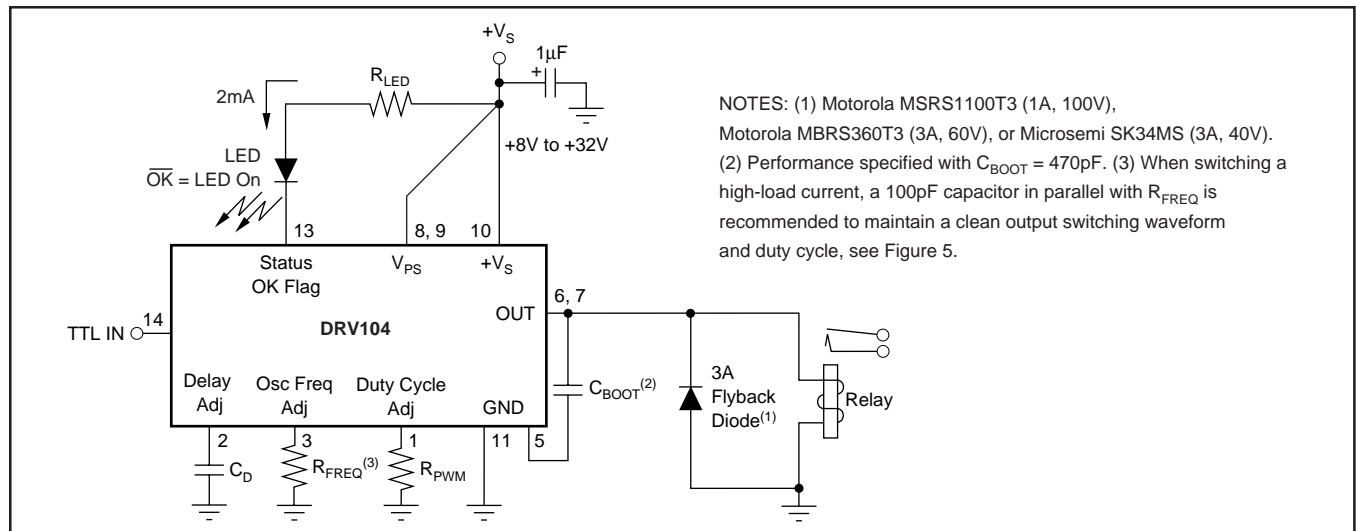


FIGURE 1. DRV104 Basic Circuit Connections.

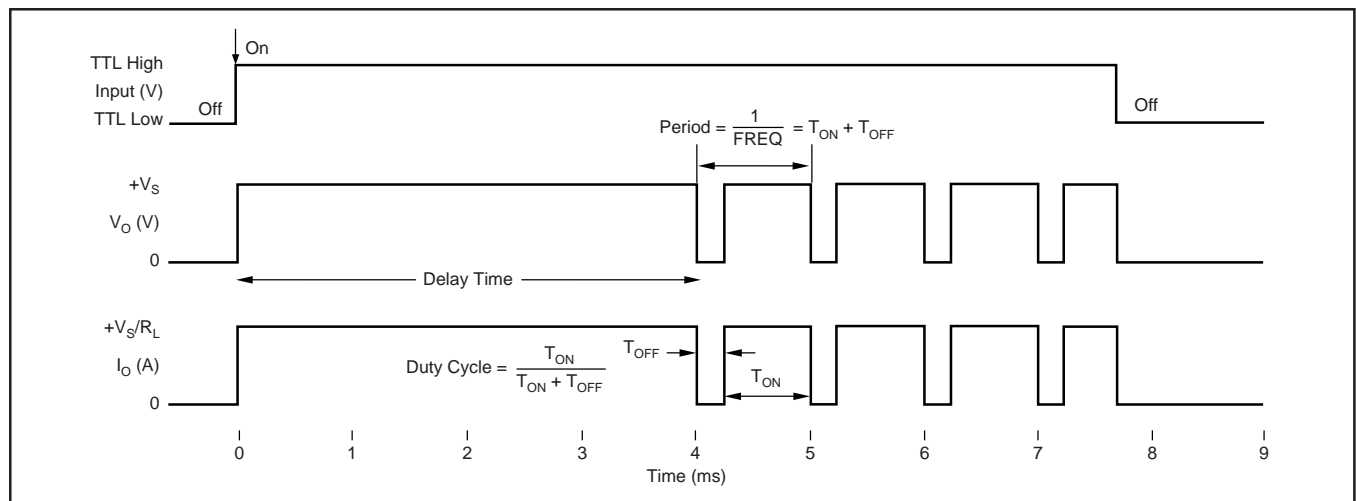


FIGURE 2. Typical Timing Diagram.

APPLICATIONS INFORMATION

POWER SUPPLY

The DRV104 operates from a single +8V to +32V supply with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. Parameters that vary significantly with operating voltage are shown in the Typical Characteristics.

ADJUSTABLE DELAY TIME (INITIAL 100% DUTY CYCLE)

A unique feature of the DRV104 is its ability to provide an initial constant DC output (100% duty cycle) and then switch to PWM mode output to save power. This function is particularly useful when driving solenoids that have a much higher pull-in current requirement than continuous-hold requirement.

The duration of this constant DC output (before PWM output begins) can be externally controlled by a capacitor connected from Delay Adjust (pin 2) to ground according to Equation 1:

$$\text{Delay Time} \approx (C_D \cdot 10^6)/1.24 \quad (1)$$

(time in seconds, C_D in Farads)

Leaving the Delay Adjust pin open results in a constant output time of approximately 18 μ s. The duration of this initial output can be reduced to less than 3 μ s by connecting the pin to 5V. Table I provides examples of delay times (constant output before PWM mode) achieved with selected capacitor values.

The internal Delay Adjust circuitry is composed of a 3 μ A current source and a 2.6V comparator, as shown in Figure 3. Thus, when the pin voltage is less than 2.6V, the output device is 100% On (DC output mode).

OSCILLATOR FREQUENCY ADJUST

The DRV104 PWM output frequency can be easily programmed over a wide range by connecting a resistor (R_{FREQ}) between Osc Freq Adj (pin 3) and ground. A range of 500Hz to 100kHz can be achieved with practical resistor values, as shown in Table II. Refer to the PWM Frequency vs R_{FREQ} plot shown in Figure 4 for additional information. Although oscillator frequency operation below 500Hz is possible, resistors higher than 10M Ω will be required. The pin becomes a very high impedance node and is therefore sensitive to noise

INITIAL CONSTANT OUTPUT DURATION	C_D
3 μ s	Pin 2 Tied to +5V
18 μ s	Pin 2 Open
81 μ s	100pF
0.81ms	1nF
8.1ms	10nF
81ms	100nF
0.81s	1 μ F
8.1s	10 μ F

TABLE I. Delay Adjust Times.

pickup and PCB leakage currents if very high resistor values are used. Refer to Figure 3 for a simplified circuit of the frequency adjust input.

The DRV104's adjustable PWM output frequency allows it to be optimized for driving virtually any type of load.

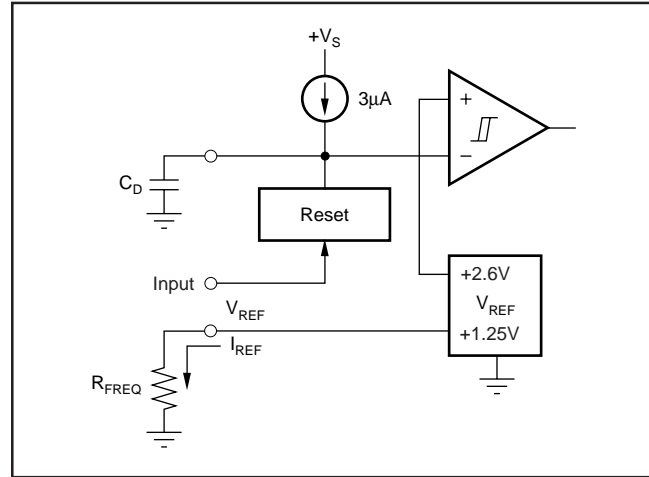


FIGURE 3. Simplified Delay Adjust and Frequency Adjust Inputs.

OSCILLATOR FREQUENCY (Hz)	R_{FREQ} (nearest 1% values) (Ω)
100k	47.5k
50k	100k
25k	191k
10k	499k
5k	976M
500	10M

TABLE II. Oscillator Frequency Resistance.

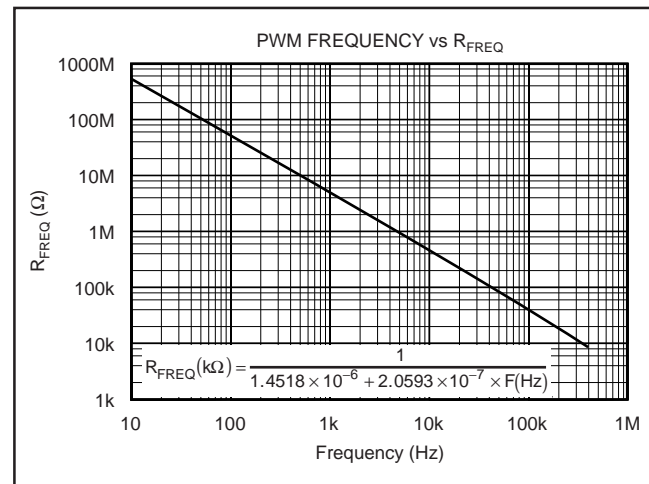


FIGURE 4. Using a Resistor to Program Oscillator Frequency.

When switching a high-load current, 100pF capacitors in parallel with R_{FREQ} are recommended to maintain a clean output switching waveform and duty cycle, see Figure 5.

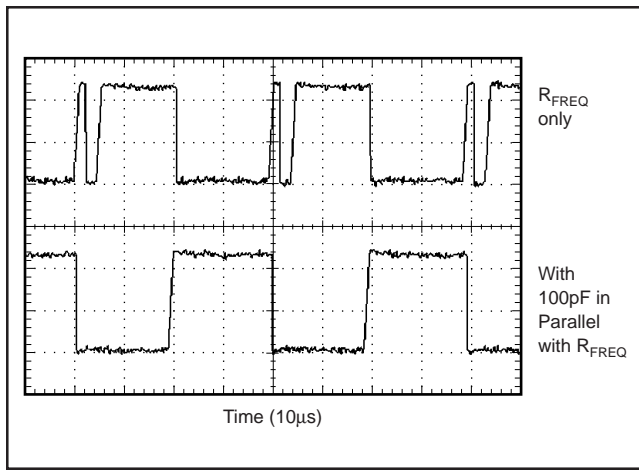


FIGURE 5. Output Waveform at High Load Current.

ADJUSTABLE DUTY CYCLE (PWM MODE)

The DRV104's externally adjustable duty cycle provides an accurate means of controlling power delivered to a load. Duty cycle can be set over a range of 10% to 90% with an external resistor, analog voltage, or the voltage output of a D/A converter. A low duty cycle results in reduced power dissipation in the load. This keeps the DRV104 and the load cooler, resulting in increased reliability for both devices.

Resistor Controlled Duty Cycle

Duty cycle is easily programmed by connecting a resistor ($R_{P_{PWM}}$) between Duty Cycle Adjust (pin 1) and ground. High resistor values correspond to high duty cycles. At 100kHz, the range of adjustable duty cycle is limited to 10% to 70%. Table III provides resistor values for typical duty cycles. Resistor values for additional duty cycles can be obtained from Figure 6.

DUTY CYCLE (%)	$R_{P_{PWM}}$ (Ω) (Nearest 1% Values)		
	5kHz	25kHz	100kHz
10	412k	84.5k	25.5k
20	487k	97.6k	28.7k
30	562k	113k	31.6k
40	649k	130k	35.7k
50	715k	147k	39.2k
60	787k	162k	43.2k
70	887k	174k	44.9k
80	953k	191k	—
90	1050k	205k	—

TABLE III. Duty Cycle Adjust Resistance.

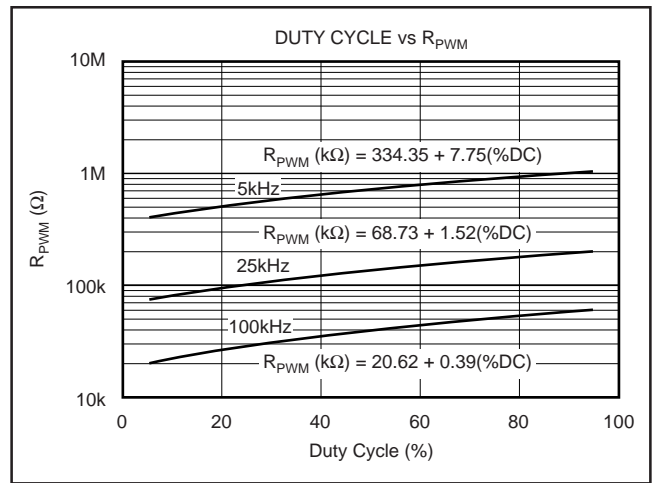


FIGURE 6. Using a Resistor to Program Duty Cycle.

Voltage Controlled Duty Cycle

The duty cycle can also be programmed by analog voltage $V_{P_{PWM}}$. With $V_{P_{PWM}} \approx 3.59V$, the duty cycle is about 90%. Decreasing this voltage results in decreased duty cycles. Table IV provides $V_{P_{PWM}}$ values for typical duty cycles. Figure 7 shows the relationship of duty cycle versus $V_{P_{PWM}}$ and its linearity.

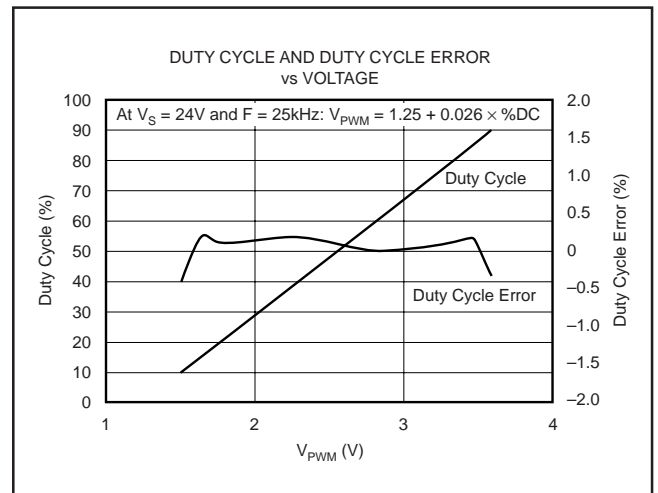


FIGURE 7. Using a Voltage to Program Duty Cycle.

DUTY CYCLE (%)	$V_{P_{PWM}}$ (V)
10	1.501
20	1.773
40	2.296
60	2.813
80	3.337
90	3.589

TABLE IV. Duty Cycle Adjust Voltage.

The Duty Cycle Adjust pin is internally driven by an oscillator frequency dependent current source and connects to the input of a comparator, as shown in Figure 8. The DRV104's PWM adjustment is inherently monotonic; that is, a decreased voltage (or resistor value) always produces an decreased duty cycle.

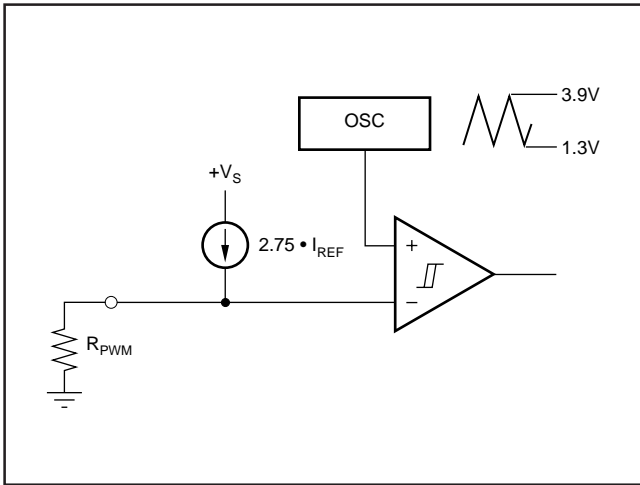


FIGURE 8. Simplified Duty Cycle Adjust Input.

STATUS OK FLAG

The Status OK Flag (pin 13) provides a fault indication for over-current and thermal shutdown conditions. During a fault condition, the Status OK Flag output is driven Low (pin voltage typically drops to 0.45V). A pull-up resistor, as shown in Figure 9, is required to interface with standard logic. Figure 9 also gives an example of a non-latching fault monitoring circuit, while Figure 10 provides a latching version. The Status OK Flag pin can sink up to 10mA, sufficient to drive external logic circuitry, a reed relay, or an LED (as shown in Figure 11) to indicate when a fault has occurred. In addition, the Status OK Flag pin can be used to turn off other DRV104s in a system for chain fault protection.

Over-Current Fault

An over-current fault occurs when the PWM peak output current is greater than typically 2.0A. The Status OK flag is not latched. Since current during PWM mode is switched on and off, the Status OK flag output will be modulated with PWM timing (see the Status OK flag waveforms in the Typical Characteristics).

Avoid adding capacitance to pins 6, 7 (OUT) because this can cause momentary current limiting.

Over-Temperature Fault

A thermal fault occurs when the die reaches approximately 160°C, producing an effect similar to pulling the input low. Internal shutdown circuitry disables the output. The Status OK Flag is latched in the Low state (fault condition) until the die has cooled to approximately 140°C.

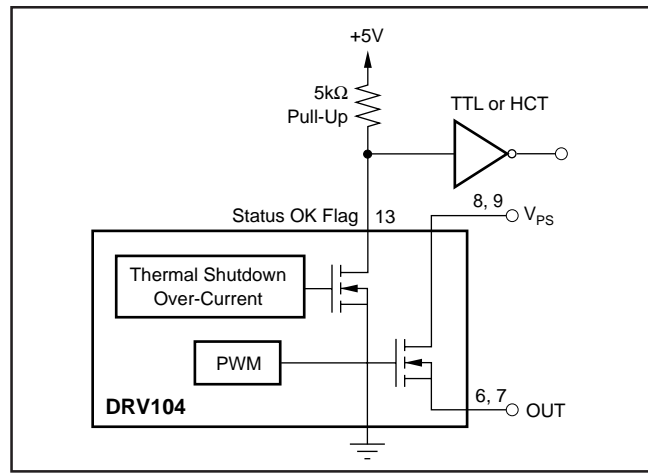
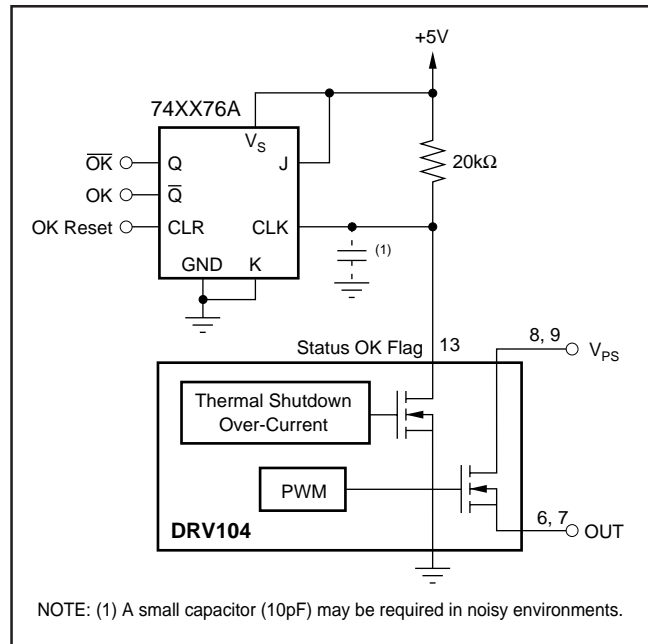


FIGURE 9. Non-Latching Fault Monitoring Circuit.



NOTE: (1) A small capacitor (10pF) may be required in noisy environments.

FIGURE 10. Latching Fault Monitoring Circuit.

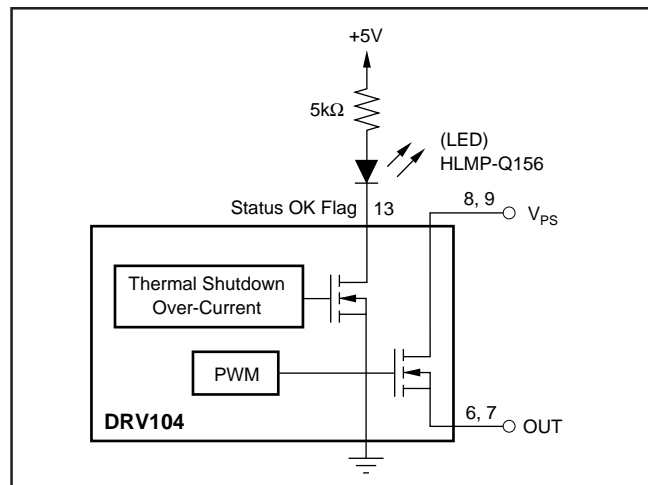


FIGURE 11. Using an LED to Indicate a Fault Condition.

PACKAGE MOUNTING

Figure 12 provides recommended printed circuit board (PCB) layouts for the PowerPAD HTSSOP-14 package. The metal pad of the PowerPAD HTSSOP-14 package is electrically isolated from other pins and ideally should be connected to a ground. For reliable operation, the PowerPAD must be directly soldered to a circuit board, as shown in Figure 13. Increasing the heat-sink copper area improves heat dissipation. Figure 14 shows typical junction-to-ambient thermal resistance as a function of the PCB copper area.

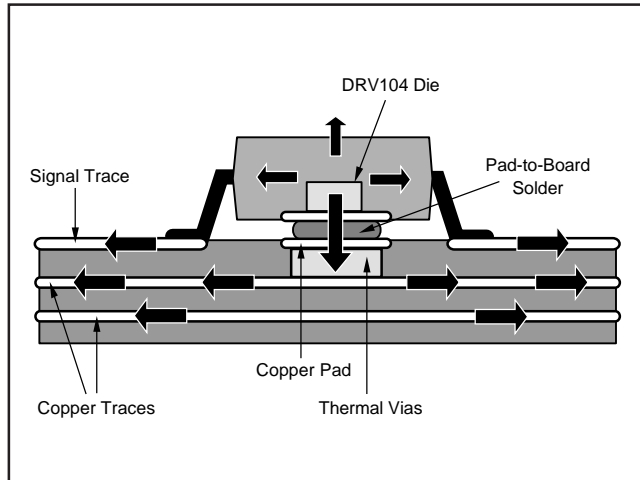


FIGURE 13. PowerPAD Heat Transfer.

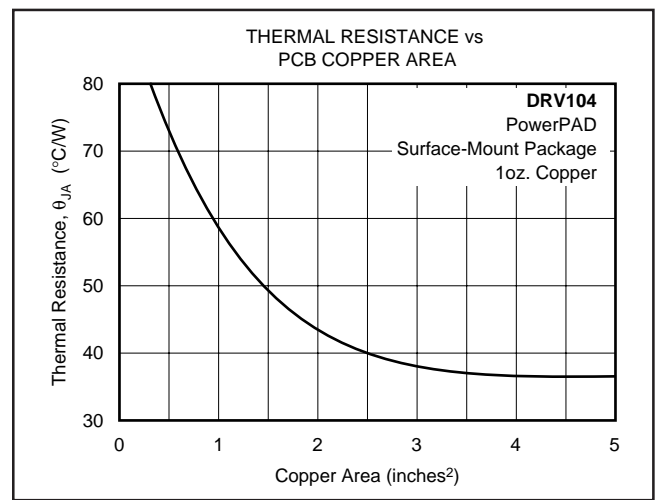


FIGURE 14. Heat-Sink Thermal Resistance vs PCB Copper Area.

POWER DISSIPATION

The DRV104 power dissipation depends on power supply, signal, and load conditions. Power dissipation (P_D) is equal to the product of output current times the voltage across the conducting DMOS transistor times the duty cycle. Using the lowest possible duty cycle necessary to assure the required hold force can minimize power dissipation in both the load and in the DRV104. At 1A, the output DMOS transistor on-resistance is 0.45Ω , increasing to 0.65Ω at current limit.

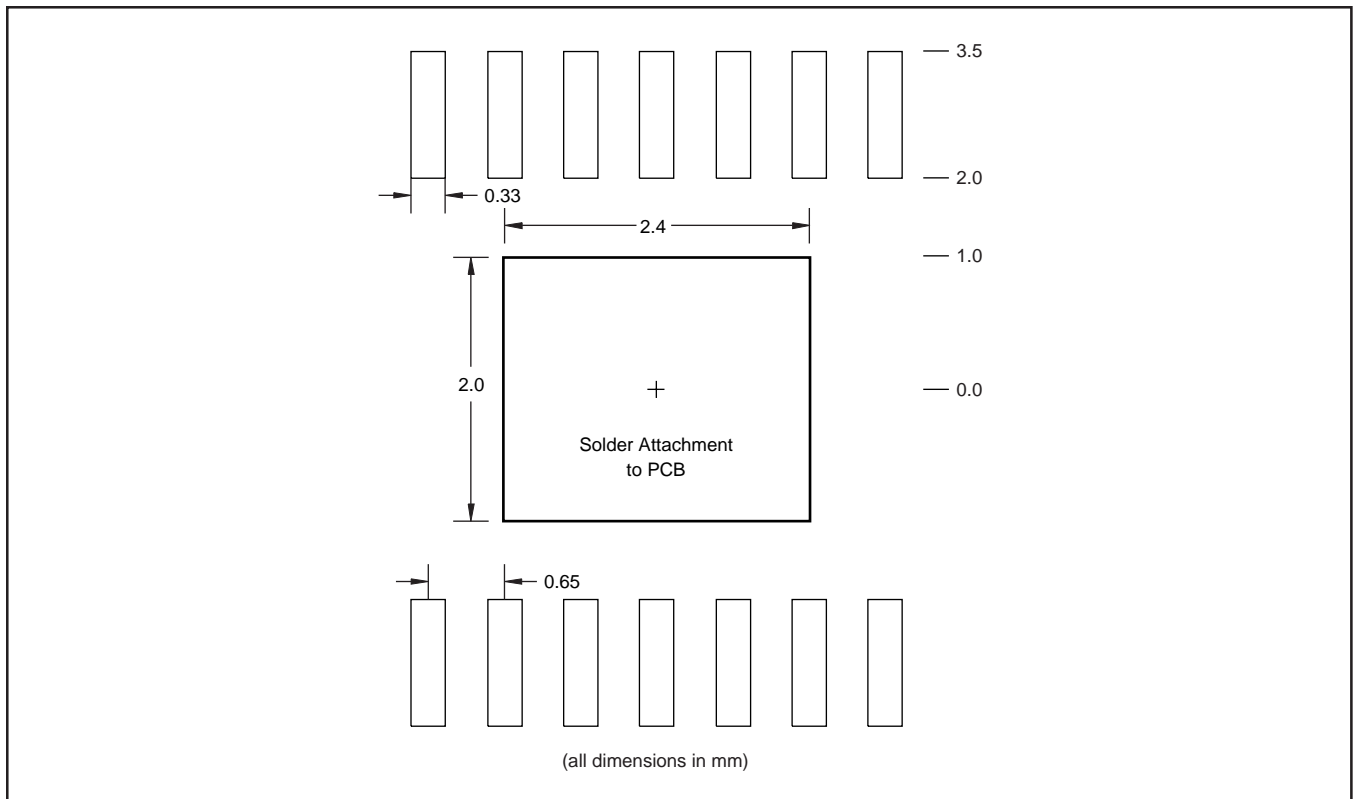


FIGURE 12. Recommended PCB Layout.

At very high oscillator frequencies, the energy in the DRV104's linear rise and fall times can become significant and cause an increase in P_D .

THERMAL PROTECTION

Power dissipated in the DRV104 causes its internal junction temperature to rise. The DRV104 has an on-chip thermal shutdown circuitry that protects the IC from damage. The thermal protection circuitry disables the output when the junction temperature reaches approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is again enabled. Depending on load and signal conditions, the thermal protection circuit may cycle on and off. This limits the dissipation of the driver but may have an undesirable effect on the load.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to a maximum of +125°C. To estimate the margin of safety in a complete design (including heat-sink), increase the ambient temperature until the thermal protection is triggered. Use worst-case load and signal conditions. For good reliability, thermal protection should trigger more than 35°C above the maximum expected ambient condition of your application. This produces a junction temperature of 125°C at the maximum expected ambient condition.

The internal protection circuitry of the DRV104 is designed to protect against overload conditions. It is not intended to replace proper heat sinking. Continuously running the DRV104 into thermal shutdown will degrade device reliability.

HEAT SINKING

Most applications do not require a heat-sink to assure that the maximum operating junction temperature (125°C) is not exceeded. However, junction temperature should be kept as low as possible for increased reliability. Junction temperature can be determined according to the following equations:

$$T_J = T_A + P_D \theta_{JA} \quad (3)$$

$$\theta_{JA} = \theta_{JC} + \theta_{CH} + \theta_{HA} \quad (4)$$

where:

T_J = Junction Temperature (°C)

T_A = Ambient Temperature (°C)

P_D = Power Dissipated (W)

θ_{JC} = Junction-to-Case Thermal Resistance (°C/W)

θ_{CH} = Case-to-Heat Sink Thermal Resistance (°C/W)

θ_{HA} = Heat Sink-to-Ambient Thermal Resistance (°C/W)

θ_{JA} = Junction-to-Air Thermal Resistance (°C/W)

Using a heat sink significantly increases the maximum allowable power dissipation at a given ambient temperature.

The answer to the question of selecting a heat-sink lies in determining the power dissipated by the DRV104. For DC output into a purely resistive load, power dissipation is simply the load current times the voltage developed across the conducting output transistor times the duty cycle. Other loads are not as simple. (For further information on calculating power dissipation, refer to Application Bulletin SBFA002, available at www.ti.com.) Once power dissipation for an application is known, the proper heat-sink can be selected.

Heat-Sink Selection Example

A PowerPAD HTSSOP-14 package dissipates 2W. The maximum expected ambient temperature is 35°C. Find the proper heat-sink to keep the junction temperature below 125°C.

Combining Equations 1 and 2 gives:

$$T_J = T_A + P_D(\theta_{JC} + \theta_{CH} + \theta_{HA}) \quad (5)$$

T_J , T_A , and P_D are given. θ_{JC} is provided in the specification table: 2.07°C/W. θ_{CH} depends on heat sink size, area, and material used. Semiconductor package type and mounting can also affect θ_{CH} . A typical θ_{CH} for a soldered-in-place PowerPAD HTSSOP-14 package is 2°C/W. Now, solving for θ_{HA} :

$$\theta_{HA} = \frac{T_J - T_A}{P_D} - (\theta_{JC} + \theta_{CH})$$

$$\theta_{HA} = \frac{125^\circ\text{C} - 35^\circ\text{C}}{2\text{W}} - (2.07^\circ\text{C}/\text{W} + 2^\circ\text{C}/\text{W}) \quad (6)$$

$$\theta_{HA} = 40.9^\circ\text{C}/\text{W}$$

To maintain junction temperature below 125°C, the heat-sink selected must have a θ_{HA} less than 40.9°C/W. In other words, the heat-sink temperature rise above ambient temperature must be less than 81.8°C (40.9°C/W • 2W).

Another variable to consider is natural convection versus forced convection air flow. Forced-air cooling by a small fan can lower θ_{CA} ($\theta_{CH} + \theta_{HA}$) dramatically.

As mentioned above, once a heat-sink has been selected, the complete design should be tested under worst-case load and signal conditions to ensure proper thermal protection.

RFI/EMI

Any switching system can generate noise and interference by radiation or conduction. The DRV104 is designed with controlled slew rate current switching to reduce these effects. By slowing the rise time of the output to 1µs, much lower switching noise is generated.

Radiation from the DRV104-to-load wiring (the antenna effect) can be minimized by using twisted pair cable or by shielding. Good PCB ground planes are recommended for low noise and good heat dissipation. Refer to the Bypassing section for notes on placement of the flyback diode.

BYPASSING

A 1 μ F ceramic bypass capacitor is adequate for uniform duty cycle control when switching loads of less than 0.5A. Larger bypass capacitors are required when switching high-current loads. A 10 μ F ceramic capacitor is recommended for heavy-duty (1.2A) applications. It may also be desirable to run the DRV104 and load driver on separate power supplies at high-load currents. Bypassing is especially critical near the absolute maximum supply voltage of 32V. In the event of a current overload, the DRV104 current limit responds in microseconds, dropping the load current to zero. With inadequate bypassing, energy stored in the supply line inductance can lift the supply sufficiently to exceed voltage breakdown with catastrophic results.

Place the flyback diode at the DRV104 end when driving long (inductive) cables to a remotely located load. This minimizes RFI/EMI and helps protect the output DMOS transistor from breakdown caused by di/dt transients. Fast rectifier diodes such as epitaxial silicon or Schottky types are recommended for use as flyback diodes.

APPLICATIONS CIRCUITS

SINGLE AND MULTICHANNEL

The DRV104 can be used in a variety of ways with resistive and inductive loads. As a single-channel driver, it can be placed on one PC board or inside a solenoid, relay, actuator, valve, motor, heater, thermoelectric cooler, or lamp housing. In high-density systems, multichannel power drivers may be packed close together on a PC board. For these switching applications, it is important to provide power supply bypassing as close to the driver IC as possible to avoid cross-coupling of spikes from one circuit to another. Also, in some applications, it may be necessary to keep beat frequencies (sum and difference between DRV oscillators or between DRV oscillators and system clock frequencies) from interfering with low-level analog circuits that are located relatively near to the power drivers. Paralleling device outputs is not recommended as unequal load sharing and device damage will result.

BEAT FREQUENCIES IN NON-SYNCHRONIZED MULTICHANNEL SYSTEMS

In many multichannel systems, beat frequencies are of no consequence where each DRV uses its own internal oscillator.

Beat frequencies can be intentionally set up to be outside the measurement base-band to avoid interference in sensitive analog circuits located nearby. For example, with two

DRV104s, a beat frequency of 22.5kHz can be established by setting one internal oscillator to a center of 62.5kHz and the other to 40kHz. Considering the specification of $\pm 20\%$ frequency accuracy, the beat could range from 2kHz (48kHz and 50kHz) to 43kHz (75kHz and 32kHz). By limiting the analog measurement bandwidth to 100Hz, for example, interference can be avoided.

BEAT FREQUENCY ELIMINATION—OPTIONAL SYNCHRONIZATION

The benefit of synchronization in multichannel systems is that measurement interference can be avoided in low-level analog circuits, particularly when physically close to the DRVs. Specifically, synchronization will accomplish the following:

1. Eliminate beat frequencies between DRVs or DRVs and the system clock.
2. Predict quiet or non-switching times.

Synchronization of DRV104s is possible by using one oscillator frequency for all DRVs. See Figure 15 for an example of one DRV internal oscillator as the master and the others as slaves. Also, one external clock can be used as the master and all the others as slaves.

PEAK SUPPLY CURRENT ELIMINATION—OPTIONAL SWITCHING SKEW

In many systems, particularly where only a few channels are used or low magnitude load currents are present, it is unnecessary to skew the switching times.

In some multichannel systems, where just PWM is used, without initial dc time delay, simultaneous switching of edges can cause large peak currents to be drawn from the main power supply. This is similar to that which occurs when multiple switching power supplies draw current from one power source.

Peak currents can be reduced by synchronizing oscillators and skewing switching edges. Synchronization has the added benefit of eliminating beat frequencies, as discussed above.

Skewing can be accomplished by using a polyphase clock approach, which intentionally delays the time that each DRV switches on PWM edges.

The DRV104 is useful for a variety of relay driver applications (see Figures 16 and 17), as well as valve drivers (see Figures 18 and 19).

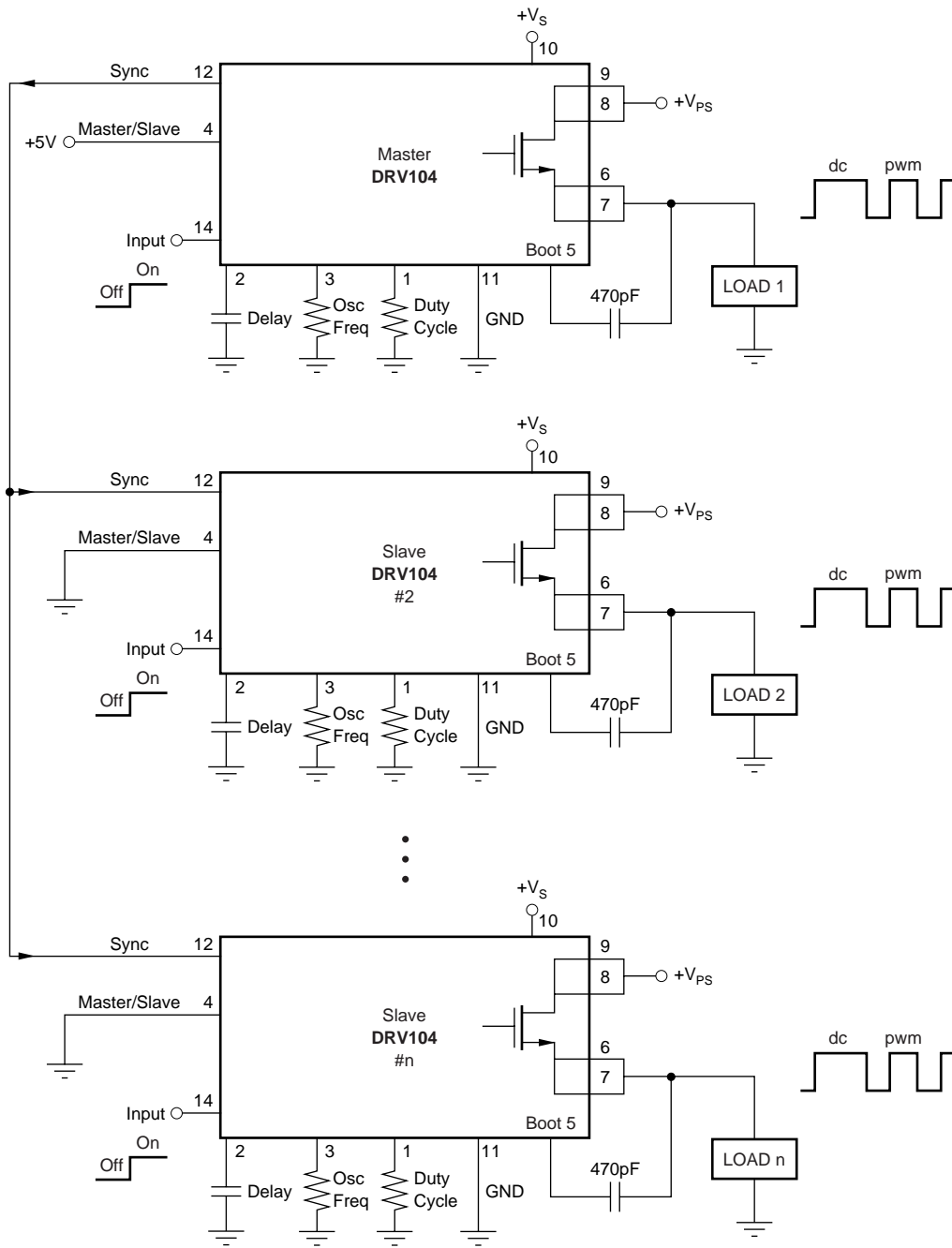


FIGURE 15. Multichannel DRV104s, Synchronized with One as the Master and the Others as Slaves.

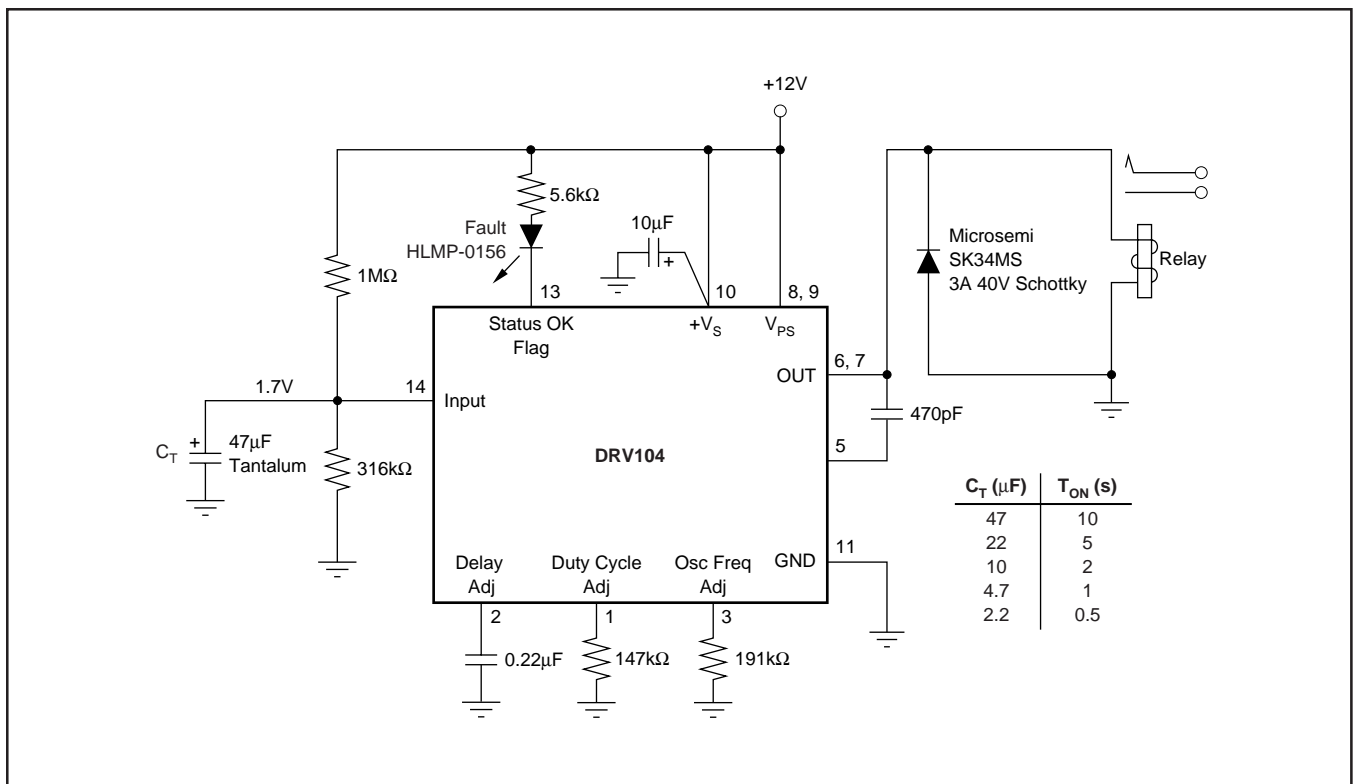


FIGURE 16. Time-Delay Relay Driver.

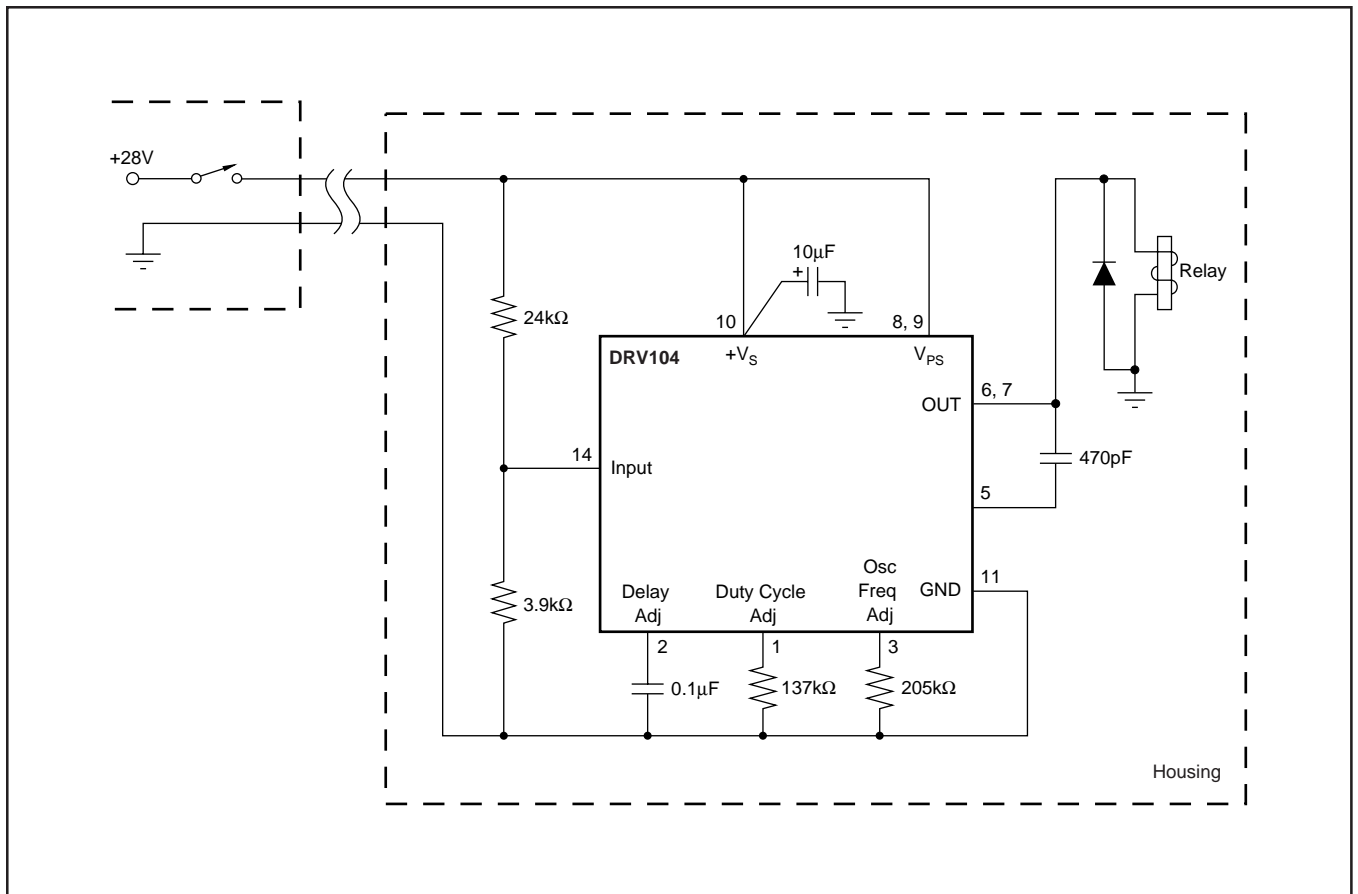


FIGURE 17. Remotely-Operated Solenoid Valve or Relay.

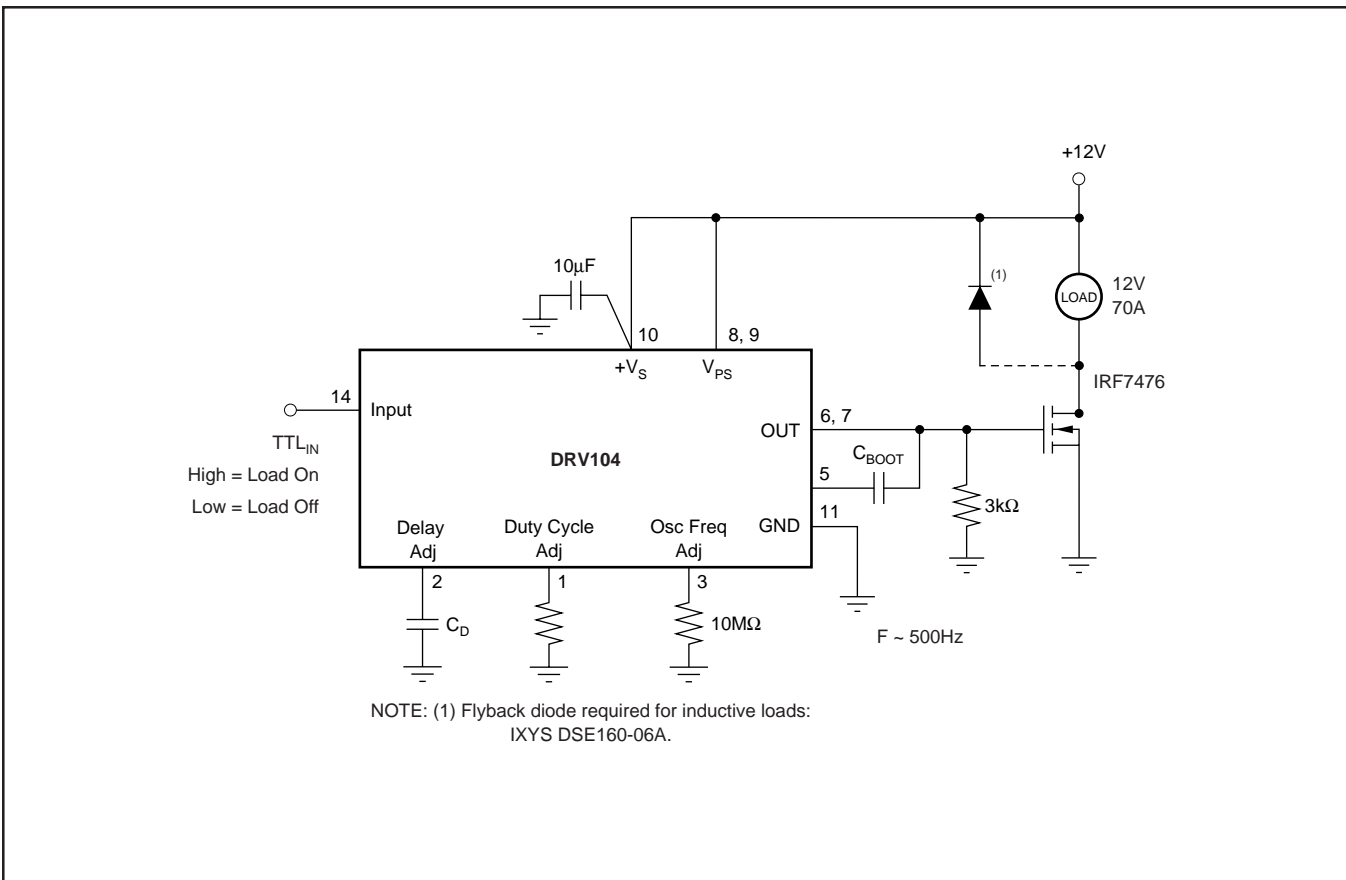


FIGURE 18. High-Power, Low-Side Driver.

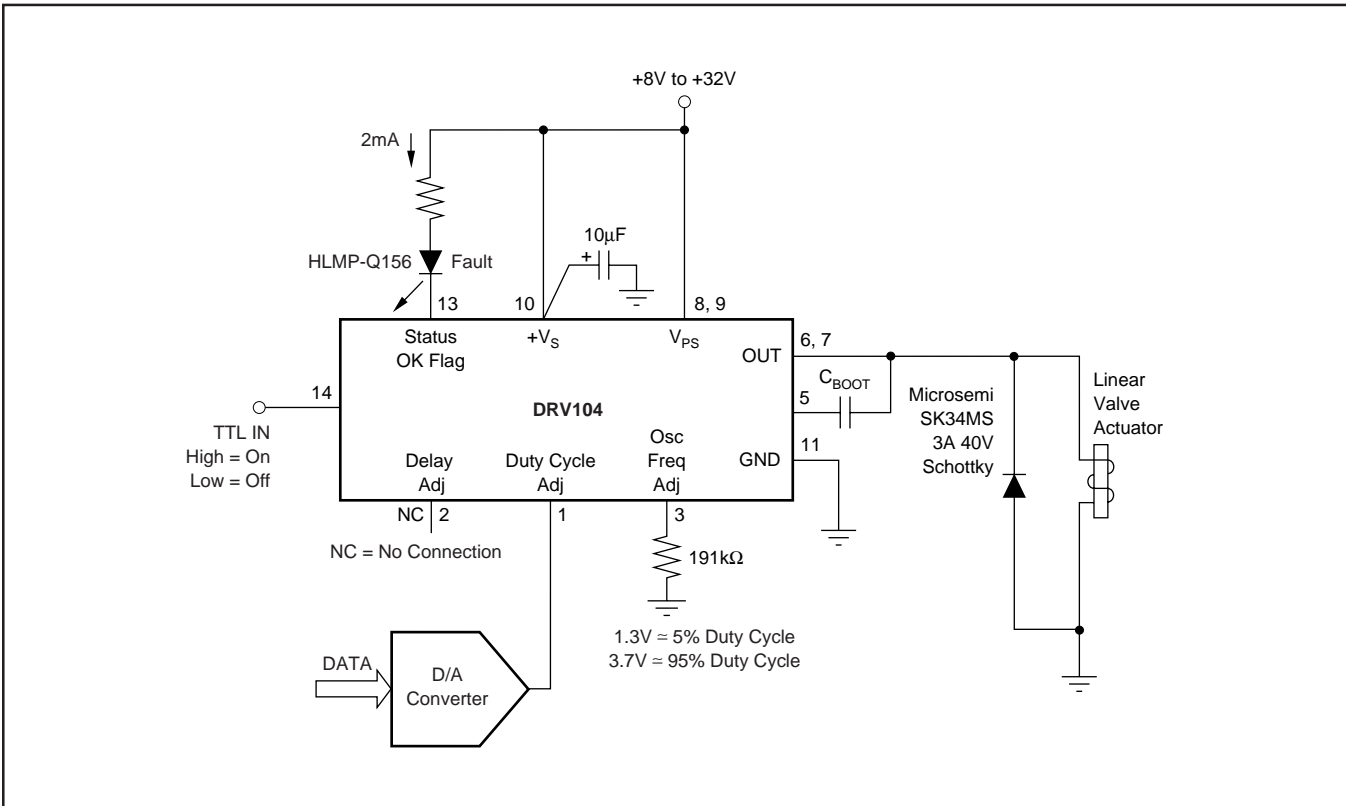


FIGURE 19. Linear Valve Driver.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DRV104PWP	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV104	Samples
DRV104PWP4	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV104	Samples
DRV104PWPR	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV104	Samples
DRV104PWPRG4	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV104	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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PWP (R-PDSO-G14)

PowerPAD™ PLASTIC SMALL OUTLINE



4073225-2/1 05/11

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

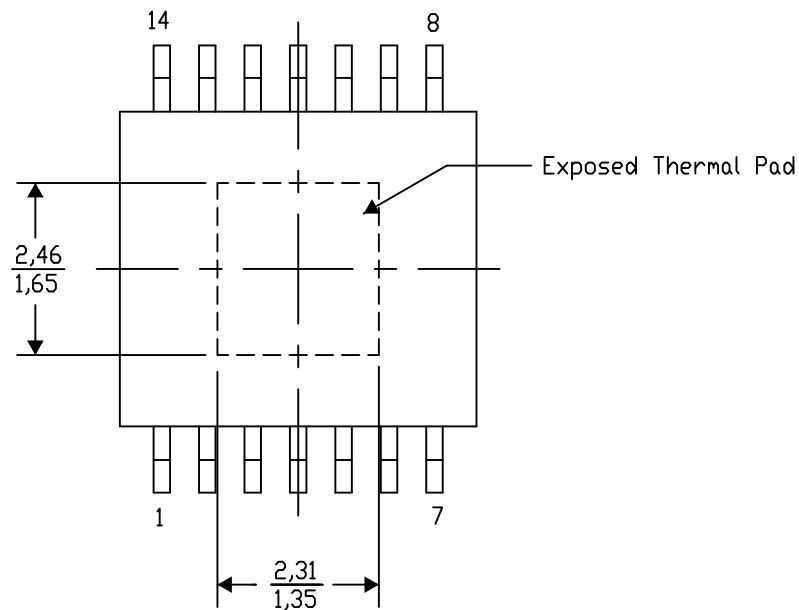
PWP (R-PDSO-G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

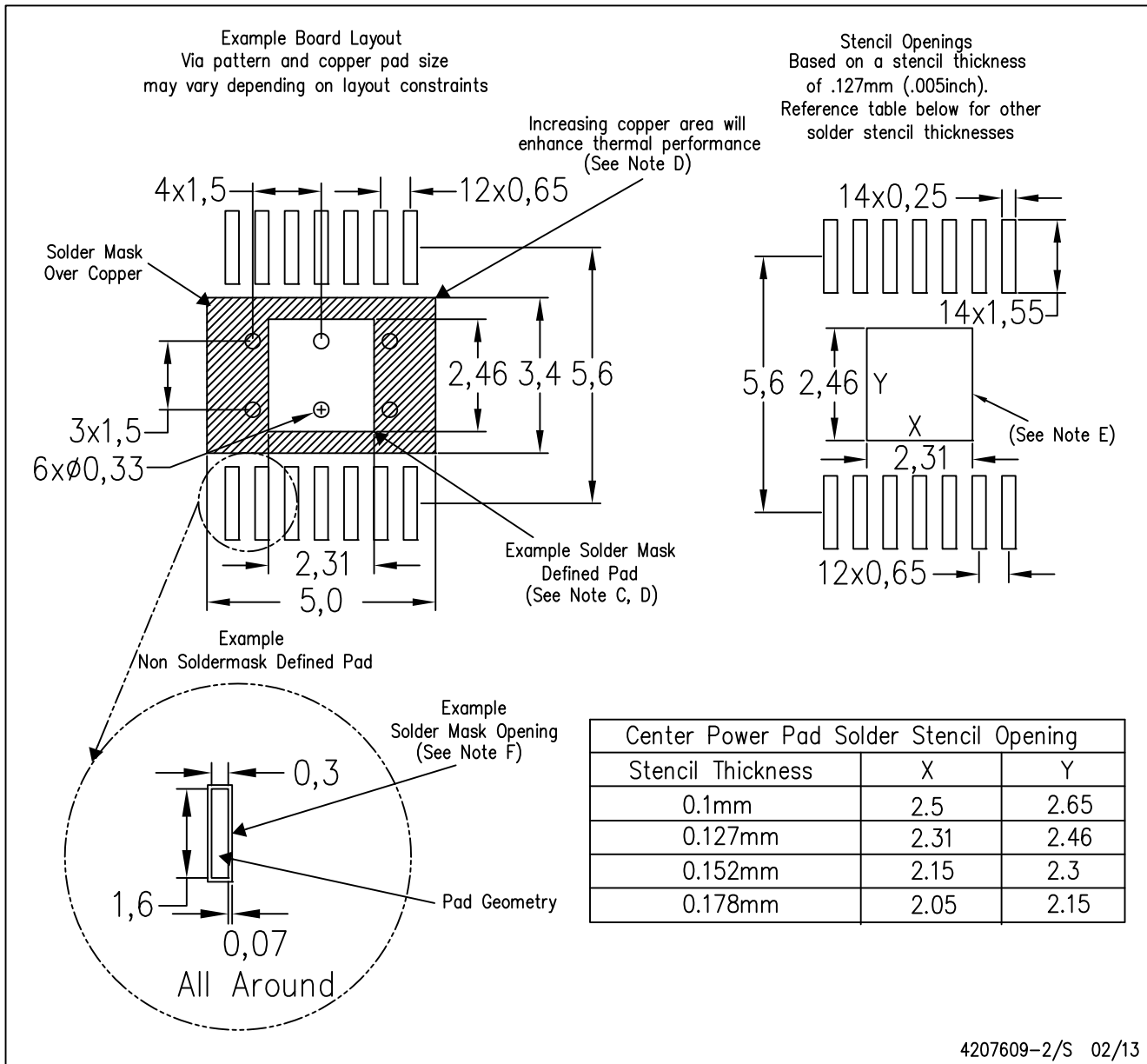
4206332-2/AE 04/13

NOTE: A. All linear dimensions are in millimeters

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PWP (R-PDSO-G14)

PowerPAD™ PLASTIC SMALL OUTLINE



4207609-2/S 02/13

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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