

LOW-NOISE, HIGH PSRR, RF 200-mA LOW-DROPOUT LINEAR REGULATORS

Check for Samples: [TPS730xx](#)

FEATURES

- 200-mA RF Low-Dropout Regulator With Enable
- Available in Fixed Voltages from 1.8V to 3.3V and Adjustable (1.22V to 5.5V)
- High PSRR (68dB at 100Hz)
- Ultralow-Noise ($33\mu\text{V}_{\text{RMS}}$, TPS73018)
- Fast Start-Up Time (50 μs)
- Stable With a 2.2 μF Ceramic Capacitor
- Excellent Load/Line Transient Response
- Very Low Dropout Voltage (120mV at 200mA)
- 5- and 6-Pin SOT23 (DBV), and Wafer Chip Scale (YZQ) Packages

APPLICATIONS

- RF: VCOs, Receivers, ADCs
- Audio
- Cellular and Cordless Telephones
- Bluetooth[®], Wireless LAN
- Handheld Organizers, PDAs

DESCRIPTION

The TPS730xx family of low-dropout (LDO) low-power linear voltage regulators features high power-supply rejection ratio (PSRR), ultralow-noise, fast start-up, and excellent line and load transient responses a small SOT23 package. NanoStar™ packaging gives an ultrasmall footprint as well as an ultralow profile and package weight, making it ideal for portable applications such as handsets and PDAs. Each device in the family is stable, with a small 2.2 μF ceramic capacitor on the output. The TPS730xx family uses an advanced, proprietary BiCMOS fabrication process to yield low dropout voltages (e.g., 120mV at 200mA, TPS73030). Each device achieves fast start-up times (approximately 50 μs with a 0.001 μF bypass capacitor) while consuming low quiescent current (170 μA typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 μA . The TPS73018 exhibits approximately 33 μV_{RMS} of output voltage noise at 1.8V output with a 0.01 μF bypass capacitor. Applications with analog components that are noise-sensitive, such as portable RF electronics, benefit from the high PSRR and low-noise features as well as the fast response time.

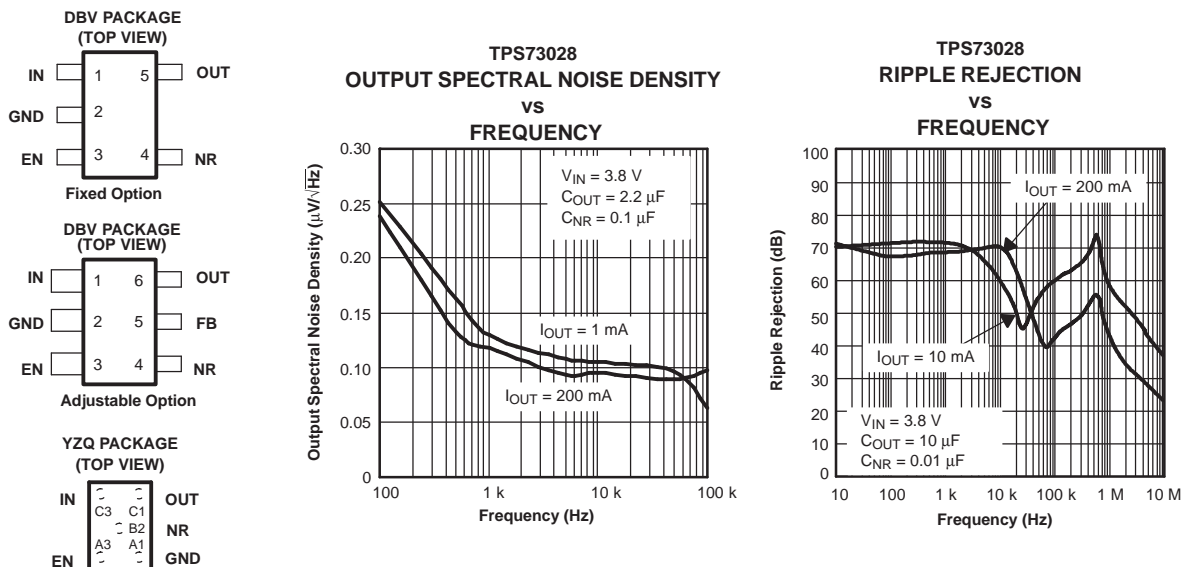


Figure 1.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar is a trademark of Texas Instruments.
 Bluetooth is a registered trademark of Bluetooth Sig, Inc.
 All other trademarks are the property of their respective owners.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

PRODUCT	V _{OUT}
TPS730xx yy yz	XX is nominal output voltage (for example, 28 = 2.8V, 01 = Adjustable). YYY is package designator. Z is package quantity.

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

Over operating temperature range (unless otherwise noted).⁽¹⁾

	UNIT
V _{IN} range	–0.3V to +6V
V _{EN} range	–0.3V to +6V
V _{OUT} range	–0.3V to V _{IN} + 0.3V
Peak output current	Internally limited
ESD rating, HBM	2kV
ESD rating, CDM	500V
Continuous total power dissipation	See Dissipation Ratings Table
Junction temperature range	–40°C to +150°C
Storage temperature range, T _{stg}	–65°C to +150°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS TABLE

BOARD	PACKAGE	R _{θJC}	R _{θJA}	DERATING FACTOR ABOVE T _A = +25°C	T _A ≤ +25°C POWER RATING	T _A = +70°C POWER RATING	T _A = +85°C POWER RATING
Low-K ⁽¹⁾	DBV	65°C/W	255°C/W	3.9mW/°C	390mW	215mW	155mW
High-K ⁽²⁾	DBV	65°C/W	180°C/W	5.6mW/°C	560mW	310mW	225mW
Low-K ⁽¹⁾	YZQ	27°C/W	255°C/W	3.9mW/°C	390mW	215mW	155mW
High-K ⁽²⁾	YZQ	27°C/W	190°C/W	5.3mW/°C	530mW	296mW	216mW

- (1) The JEDEC low-K (1s) board design used to derive this data was a 3-inch × 3-inch, two layer board with 2 ounce copper traces on top of the board.
- (2) The JEDEC high-K (2s2p) board design used to derive this data was a 3-inch × 3-inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

ELECTRICAL CHARACTERISTICS

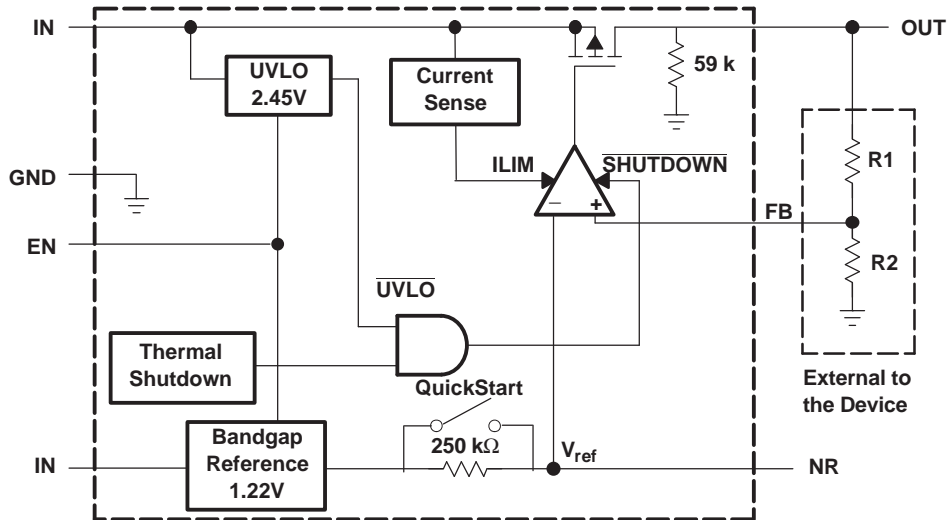
Over recommended operating temperature range T_J = –40 to +125°C, V_{EN} = V_{IN}, V_{IN} = V_{OUT(nom)} + 1 V⁽¹⁾, I_{OUT} = 1mA, C_{OUT} = 10μF, C_{NR} = 0.01μF (unless otherwise noted). Typical values are at +25°C.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IN} Input voltage ⁽¹⁾		2.7		5.5	V
I _{OUT} Continuous output current		0		200	mA
V _{FB} Internal reference (TPS73001)		1.201	1.225	1.250	V
Output voltage range (TPS73001)		V _{FB}		5.5 – V _{DO}	V
Output voltage accuracy	0μA ≤ I _{OUT} ≤ 200mA, 2.75V ≤ V _{IN} < 5.5V	–2%	V _{OUT(nom)}	+2%	V
Line regulation (ΔV _{OUT} %/ΔV _{IN}) ⁽¹⁾	V _{OUT} + 1V ≤ V _{IN} ≤ 5.5V		0.05		%/V
Load regulation (ΔV _{OUT} %/ΔI _{OUT})	0μA ≤ I _{OUT} ≤ 200mA, T _J = +25°C		5		mV
Dropout voltage ⁽²⁾ (V _{IN} = V _{OUT(nom)} – 0.1V)	I _{OUT} = 200mA		120	210	mV
Output current limit	V _{OUT} = 0V	285		600	mA
GND pin current	0μA ≤ I _{OUT} ≤ 200mA		170	250	μA
Shutdown current ⁽³⁾	V _{EN} = 0V, 2.7V ≤ V _{IN} ≤ 5.5V		0.07	1	μA
FB pin current	V _{FB} = 1.8V			1	μA
Power-supply ripple rejection	TPS73028 f = 100Hz, T _J = +25°C, I _{OUT} = 200mA		68		dB
Output noise voltage (TPS73018)	BW = 200Hz to 100kHz, I _{OUT} = 200mA C _{NR} = 0.01μF		33		μV _{RMS}
Time, start-up (TPS73018)	R _L = 14Ω, C _{OUT} = 1μF C _{NR} = 0.001μF		50		μs
High level enable input voltage	2.7V ≤ V _{IN} ≤ 5.5V	1.7		V _{IN}	V
Low level enable input voltage	2.7V ≤ V _{IN} ≤ 5.5V	0		0.7	V
EN pin current	V _{EN} = 0	–1		1	μA
UVLO threshold	V _{CC} rising	2.25		2.65	V
UVLO hysteresis			100		mV

- (1) Minimum V_{IN} is 2.7V or V_{OUT} + V_{DO}, whichever is greater.
- (2) Dropout is not measured for the TPS73018 and TPS73025 since minimum V_{IN} = 2.7V.
- (3) For adjustable versions, this applies only after V_{IN} is applied; then V_{EN} transitions high to low.

FUNCTIONAL BLOCK DIAGRAMS

ADJUSTABLE VERSION



FIXED VERSION

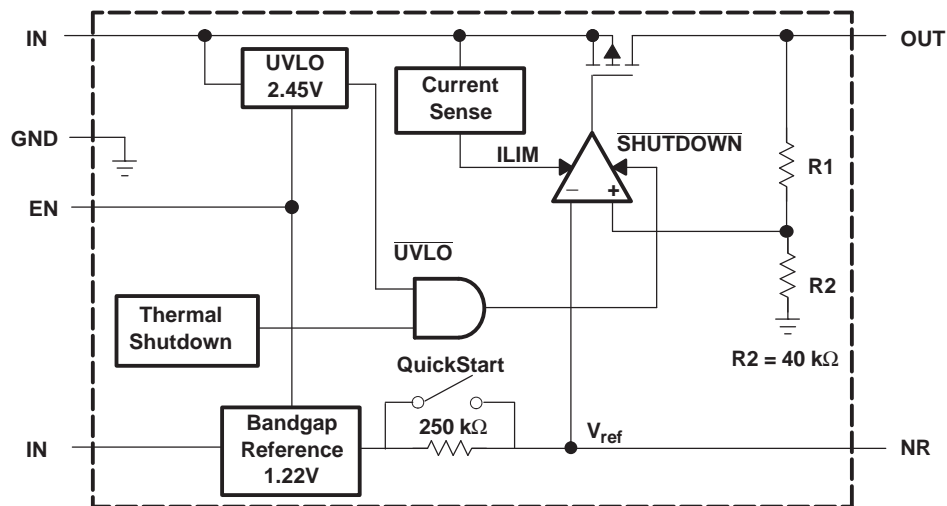


Table 1. Terminal Functions

TERMINAL				DESCRIPTION
NAME	SOT23 ADJ	SOT23 FIXED	WCSP FIXED	
NR	4	4	B2	Connecting an external capacitor to this pin bypasses noise generated by the internal bandgap. This improves power-supply rejection and reduces output noise.
EN	3	3	A3	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
FB	5	N/A	N/A	This terminal is the feedback input voltage for the adjustable device.
GND	2	2	A1	Regulator ground
IN	1	1	C3	Input to the device.
OUT	6	5	C1	Output of the regulator.

TYPICAL CHARACTERISTICS (SOT23 PACKAGE)

TPS73028
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

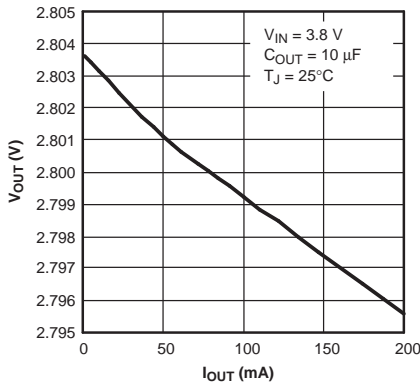


Figure 2.

TPS73028
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

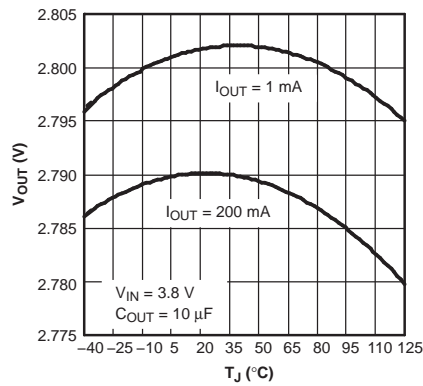


Figure 3.

TPS73028
GROUND CURRENT
vs
JUNCTION TEMPERATURE

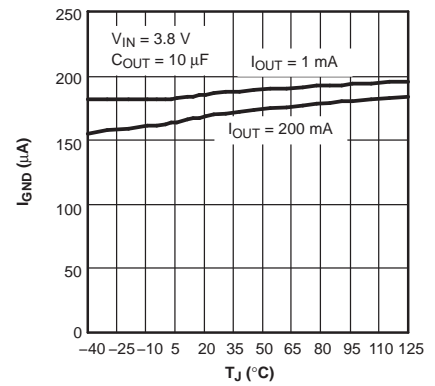


Figure 4.

TPS73028 OUTPUT SPECTRAL
NOISE DENSITY
vs
FREQUENCY

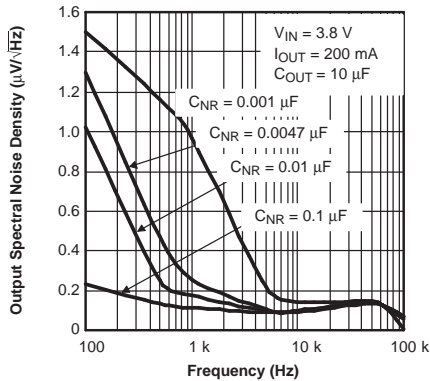


Figure 5.

ROOT MEAN SQUARE OUTPUT
NOISE
vs
CNR

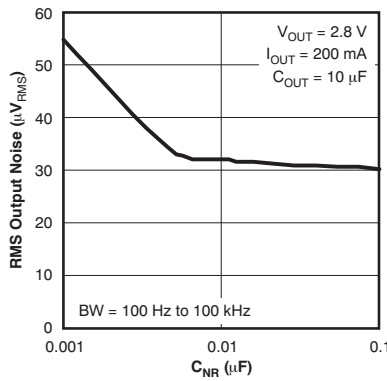


Figure 6.

TPS73028
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE

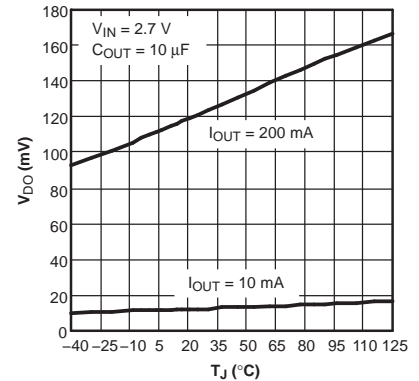


Figure 7.

TPS73028
RIPPLE REJECTION
vs
FREQUENCY

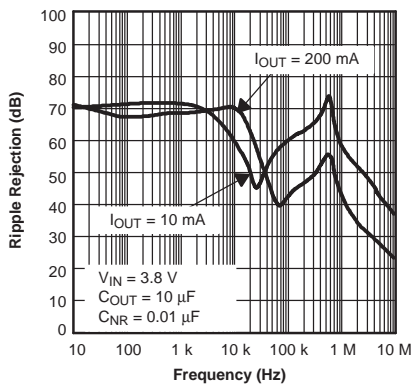


Figure 8.

TPS73028 OUTPUT VOLTAGE,
ENABLE VOLTAGE
vs
TIME (START-UP)

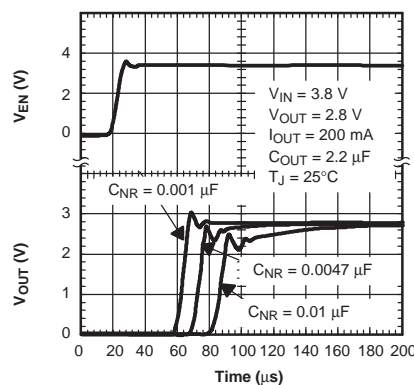


Figure 9.

TPS73028
LINE TRANSIENT RESPONSE

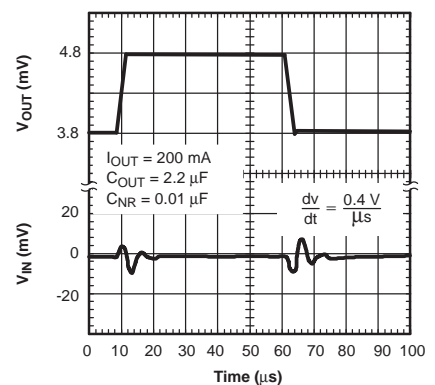


Figure 10.

TYPICAL CHARACTERISTICS (SOT23 PACKAGE) (continued)

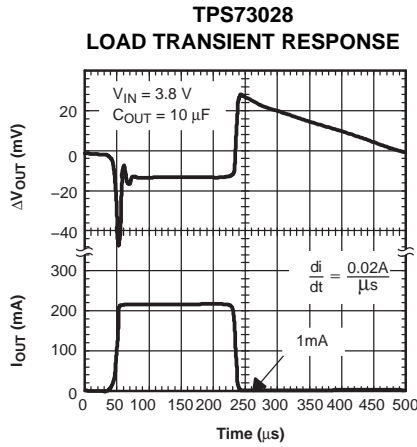


Figure 11.

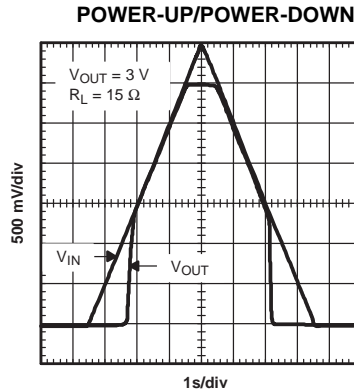


Figure 12.

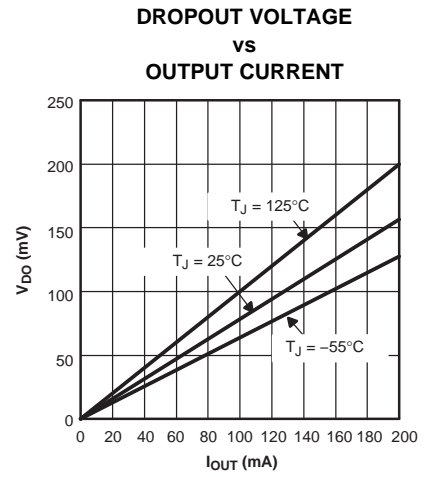


Figure 13.

TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)
vs
OUTPUT CURRENT

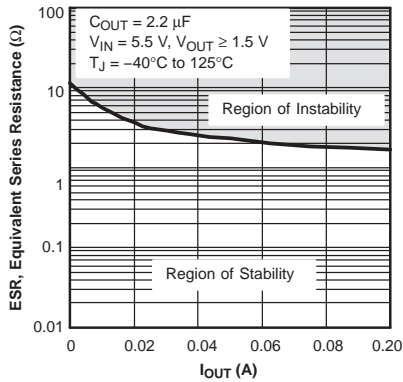


Figure 14.

TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)
vs
OUTPUT CURRENT

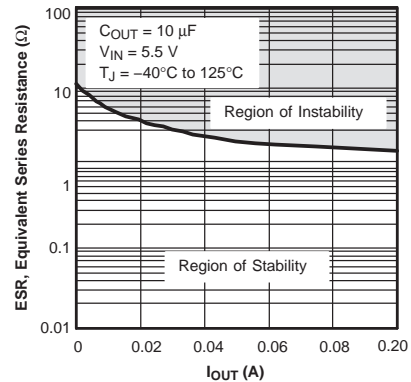


Figure 15.

APPLICATION INFORMATION

The TPS730xx family of low-dropout (LDO) regulators has been optimized for use in noise-sensitive battery-operated equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (170 μ A typically), and enable-input to reduce supply currents to less than 1 μ A when the regulator is turned off.

A typical application circuit is shown in [Figure 16](#).

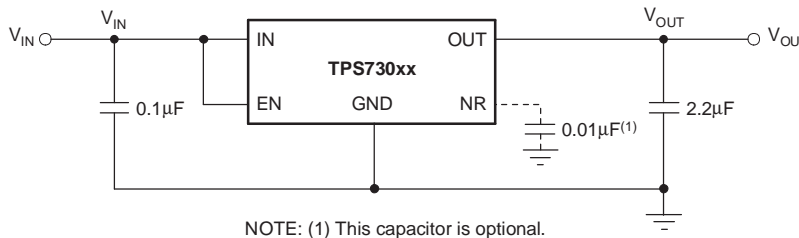


Figure 16. Typical Application Circuit

External Capacitor Requirements

A 0.1 μ F or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS730xx, is required for stability and improves transient response, noise rejection, and ripple rejection. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated or the device is located several inches from the power source.

Like most low dropout regulators, the TPS730xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 2.2 μ F. Any 2.2 μ F or larger ceramic capacitor is suitable, provided the capacitance does not vary significantly over temperature. If load current is not expected to exceed 100mA, a 1.0 μ F ceramic capacitor can be used.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS730xx has an NR pin which is connected to the voltage reference through a 250k Ω internal resistor. The 250k Ω internal resistor, in conjunction with an external bypass capacitor connected to the NR pin, creates a low pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the NR pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current. The bypass capacitor should be no more than 0.1 μ F to ensure that it is fully charged during the quickstart time provided by the internal switch shown in the [Functional Block Diagrams](#).

As an example, the TPS73018 exhibits only 33 μ V_{RMS} of output voltage noise using a 0.01 μ F ceramic bypass capacitor and a 2.2 μ F ceramic output capacitor. Note that the output starts up slower as the bypass capacitance increases due to the RC time constant at the NR pin that is created by the internal 250k Ω resistor and external capacitor.

Board Layout Recommendation to Improve PSRR and Noise Performance

To improve ac measurements like PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT} , with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of +125°C; the maximum junction temperature should be restricted to +125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(max)}$.

The maximum power dissipation limit is determined using [Equation 1](#):

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

Where:

- T_{Jmax} is the maximum allowable junction temperature.
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the [Dissipation Ratings Table](#)).
- T_A is the ambient temperature.

(1)

The regulator dissipation is calculated using [Equation 2](#):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

(2)

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

Programming the TPS73001 Adjustable LDO Regulator

The output voltage of the TPS73001 adjustable regulator is programmed using an external resistor divider as shown in [Figure 17](#). The output voltage is calculated using [Equation 3](#):

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2} \right)$$

Where:

- $V_{REF} = 1.225V$ typ (the internal reference voltage)

(3)

Resistors R_1 and R_2 should be chosen for approximately 50 μA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistor values should be avoided as leakage current into/out of FB across R_1/R_2 creates an offset voltage that artificially increases/decreases the feedback voltage and thus erroneously decreases/increases V_{OUT} . The recommended design procedure is to choose $R_2 = 30.1k\Omega$ to set the divider current at 50 μA , $C_1 = 15pF$ for stability, and then calculate R_1 using [Equation 4](#):

$$R_1 = \left[\frac{V_{OUT}}{V_{REF}} - 1 \right] \times R_2$$

(4)

In order to improve the stability of the adjustable version, it is suggested that a small compensation capacitor be placed between OUT and FB. For voltages < 1.8V, the value of this capacitor should be 100pF. For voltages > 1.8V, the approximate value of this capacitor can be calculated as shown in [Equation 5](#):

$$C_1 = \frac{(3 \times 10^{-7}) \times (R_1 + R_2)}{(R_1 \times R_2)}$$

(5)

The suggested value of this capacitor for several resistor ratios is shown in the table below. If this capacitor is not used (such as in a unity-gain configuration) or if an output voltage < 1.8V is chosen, then the minimum recommended output capacitor is 4.7 μF instead of 2.2 μF .

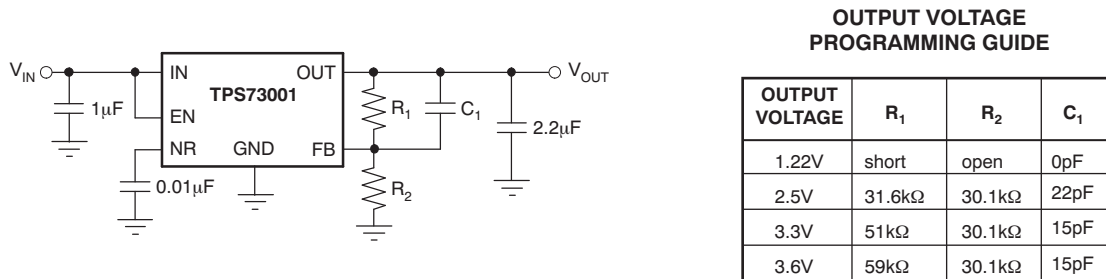


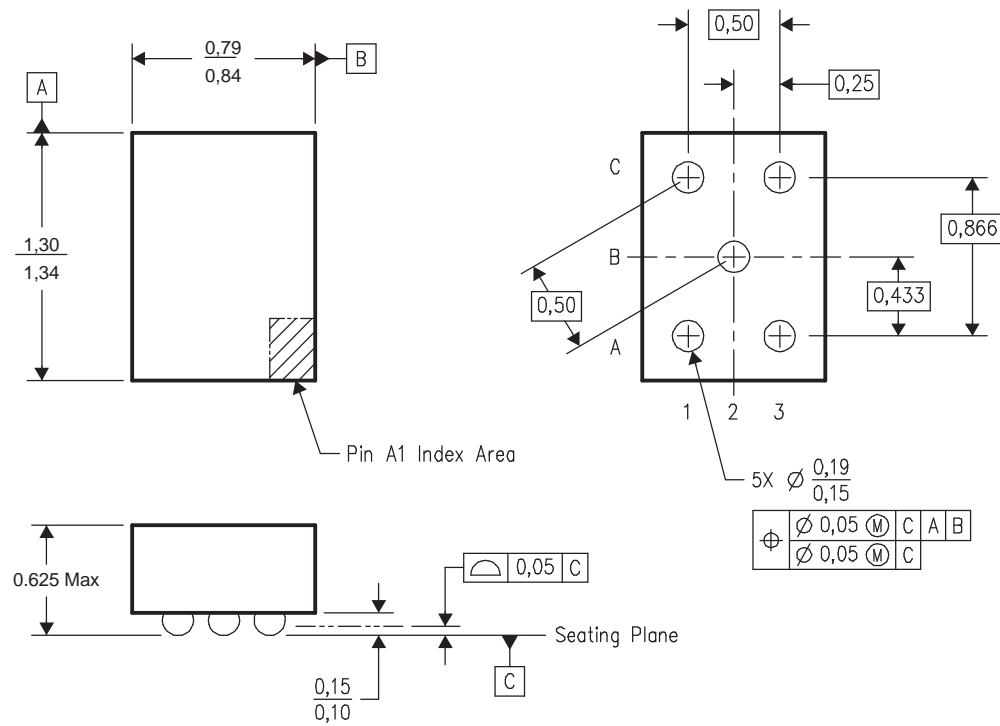
Figure 17. TPS73001 Adjustable LDO Regulator Programming

Regulator Protection

The TPS730xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS730xx features internal current limiting and thermal protection. During normal operation, the TPS730xx limits output current to approximately 400mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package or the absolute maximum voltage ratings of the device. If the temperature of the device exceeds approximately +165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately +140°C, regulator operation resumes.

TPS730xxYZQ NanoStar™ Wafer Chip Scale Information



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. NanoStar™ package configuration.
 D. This package is tin-lead (SnPb); consult the factory for availability of lead-free material.

NanoStar is a trademark of Texas Instruments.

Figure 18. NanoStar™ Wafer Chip Scale Package

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (October, 2007) to Revision I	Page
• Corrected units in y-axis of Figure 6	5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS73001DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGVI	Samples
TPS73001DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGVI	Samples
TPS73001DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGVI	Samples
TPS73001DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGVI	Samples
TPS73018DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHHI	Samples
TPS73018DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHHI	Samples
TPS73018DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHHI	Samples
TPS73018DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHHI	Samples
TPS73018YZQR	OBSOLETE	DSBGA	YZQ	5		TBD	Call TI	Call TI	-40 to 85	E3	
TPS73018YZQT	ACTIVE	DSBGA	YZQ	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	E3	Samples
TPS73025DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGWI	Samples
TPS73025DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGWI	Samples
TPS73025DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGWI	Samples
TPS73025DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGWI	Samples
TPS73025YZQR	ACTIVE	DSBGA	YZQ	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	E4	Samples
TPS73025YZQT	ACTIVE	DSBGA	YZQ	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	E4	Samples
TPS730285DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHII	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS730285DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHII	Samples
TPS730285DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHII	Samples
TPS730285DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHII	Samples
TPS730285YZQR	ACTIVE	DSBGA	YZQ	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	E5	Samples
TPS730285YZQT	ACTIVE	DSBGA	YZQ	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	E5	Samples
TPS73028DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGXI	Samples
TPS73028DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGXI	Samples
TPS73028DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGXI	Samples
TPS73028DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGXI	Samples
TPS73028YZQR	ACTIVE	DSBGA	YZQ	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	E2	Samples
TPS73028YZQT	ACTIVE	DSBGA	YZQ	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	E2	Samples
TPS73030DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGYI	Samples
TPS73030DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGYI	Samples
TPS73030DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGYI	Samples
TPS73030DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGYI	Samples
TPS73030YZQR	OBSOLETE	DSBGA	YZQ	5		TBD	Call TI	Call TI	-40 to 85		
TPS73030YZQT	OBSOLETE	DSBGA	YZQ	5		TBD	Call TI	Call TI	-40 to 85		
TPS73033DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHUI	Samples
TPS73033DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHUI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS73033DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHUI	Samples
TPS73033DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHUI	Samples
TPS73047DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PETI	Samples
TPS73047DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PETI	Samples
TPS73047DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PETI	Samples
TPS73047DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PETI	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

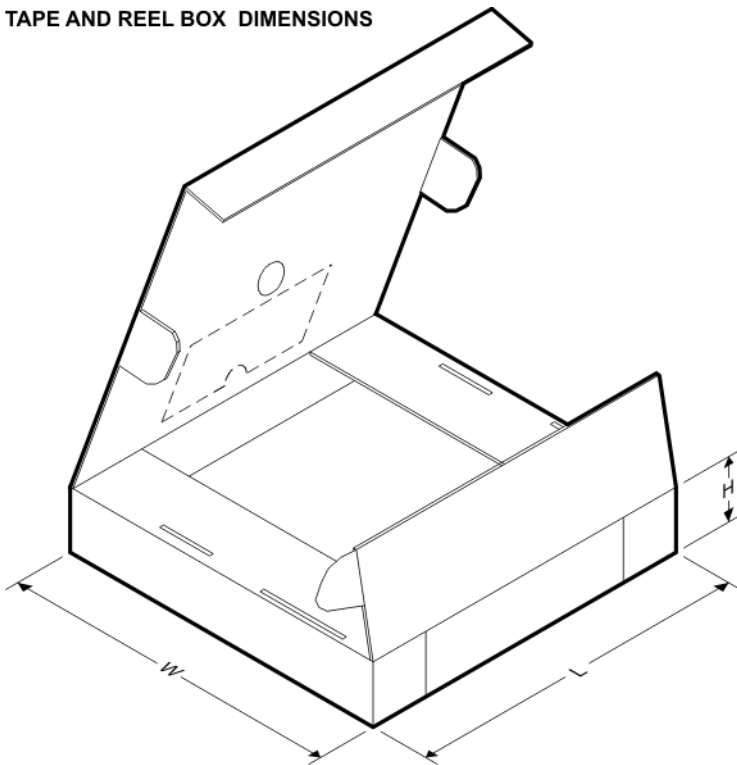
TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73001DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73001DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73001DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73018DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73018DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73018YZQT	DSBGA	YZQ	5	250	178.0	8.4	0.98	1.46	0.69	4.0	8.0	Q1
TPS73025DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73025DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73025YZQR	DSBGA	YZQ	5	3000	178.0	8.4	0.98	1.46	0.69	4.0	8.0	Q1
TPS73025YZQT	DSBGA	YZQ	5	250	178.0	8.4	0.98	1.46	0.69	4.0	8.0	Q1
TPS730285DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS730285DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS730285YZQR	DSBGA	YZQ	5	3000	178.0	8.4	0.98	1.46	0.69	4.0	8.0	Q1
TPS730285YZQT	DSBGA	YZQ	5	250	178.0	8.4	0.98	1.46	0.69	4.0	8.0	Q1
TPS73028DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73028DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73028YZQR	DSBGA	YZQ	5	3000	178.0	8.4	0.98	1.46	0.69	4.0	8.0	Q1
TPS73028YZQT	DSBGA	YZQ	5	250	178.0	8.4	0.98	1.46	0.69	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73030DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73030DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73033DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73033DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73047DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73047DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73001DBVR	SOT-23	DBV	6	3000	203.0	203.0	35.0
TPS73001DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS73001DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS73018DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73018DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73018YZQT	DSBGA	YZQ	5	250	217.0	193.0	35.0
TPS73025DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73025DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73025YZQR	DSBGA	YZQ	5	3000	217.0	193.0	35.0
TPS73025YZQT	DSBGA	YZQ	5	250	217.0	193.0	35.0
TPS730285DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS730285DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS730285YZQR	DSBGA	YZQ	5	3000	217.0	193.0	35.0
TPS730285YZQT	DSBGA	YZQ	5	250	217.0	193.0	35.0
TPS73028DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73028DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73028YZQR	DSBGA	YZQ	5	3000	217.0	193.0	35.0
TPS73028YZQT	DSBGA	YZQ	5	250	217.0	193.0	35.0
TPS73030DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73030DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73033DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73033DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73047DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
TPS73047DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0

DBV (R-PDSO-G5)

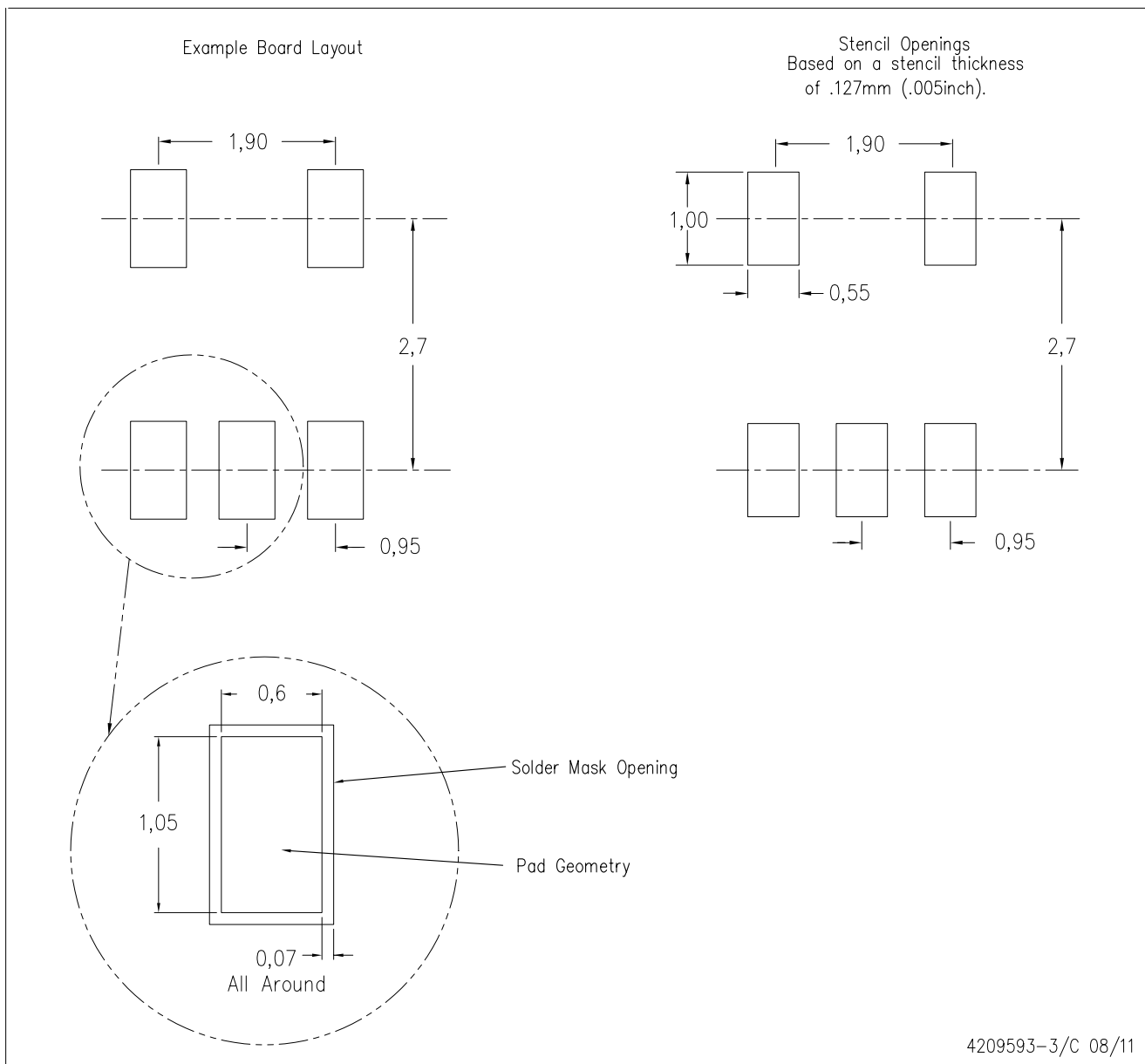
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

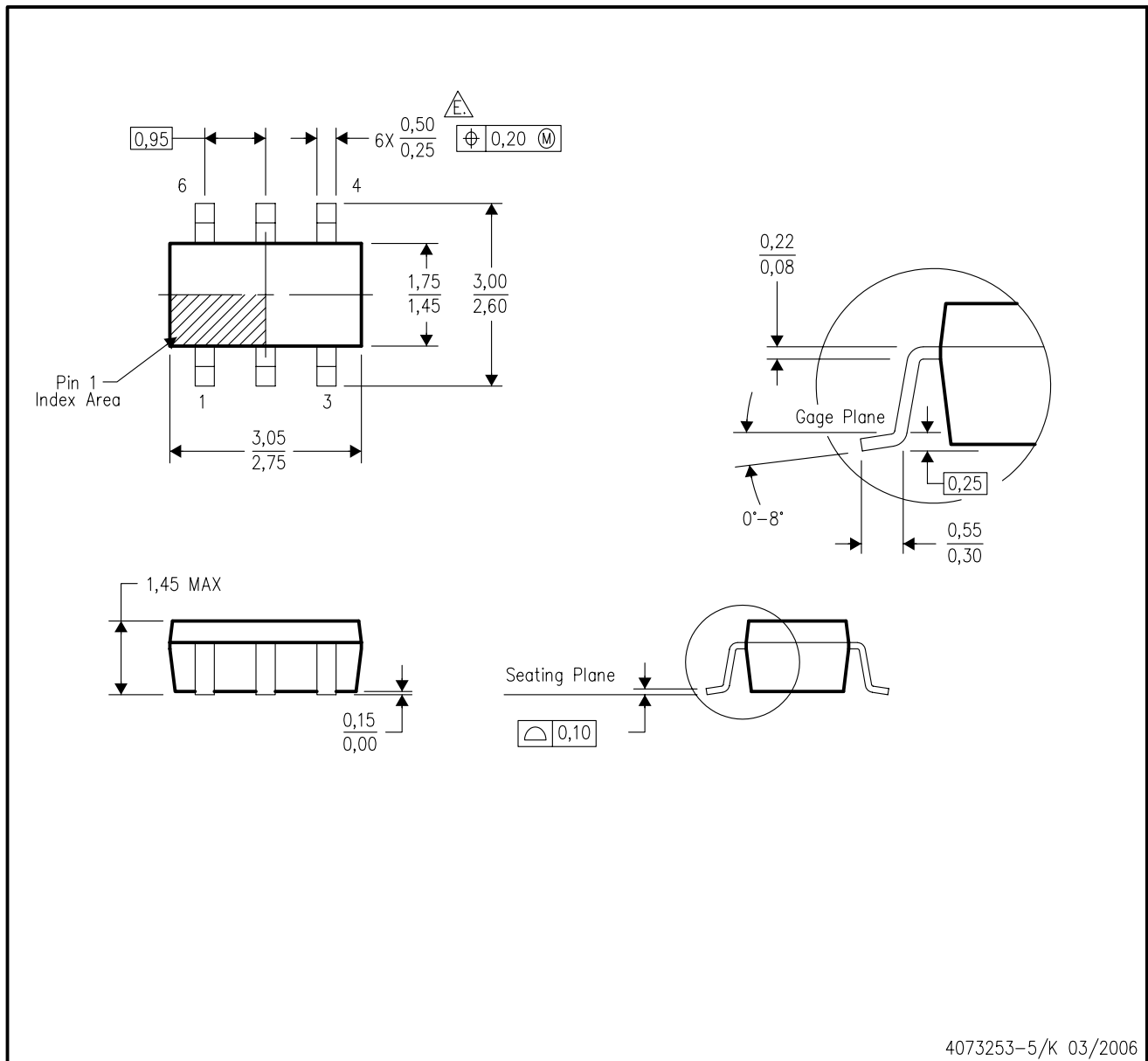
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- \triangle Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6)

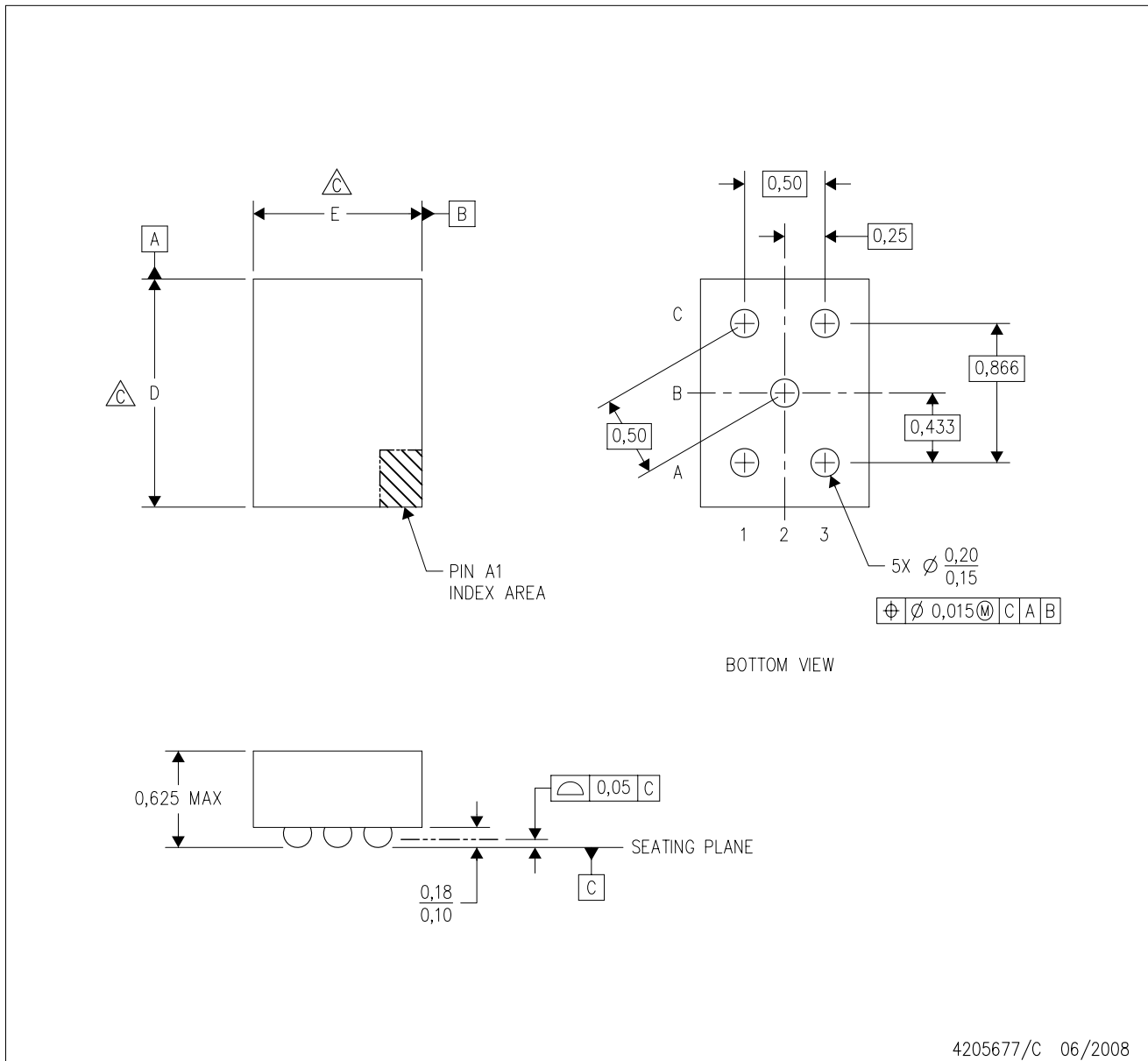
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

YZQ (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



- Notes:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - △ Devices in this YZQ package can have dimension D ranging from 1.17 to 1.67 mm and dimension E ranging from 0.80 to 1.30 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
 - D. NanoFree™ package configuration.
 - E. This package contains lead-free balls. Refer to the 5 YEQ package (drawing 4205338) for tin-lead (SnPb) balls.

NanoFree is a trademark of Texas Instruments.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com