# LOW-QUIESCENT-CURRENT PROGRAMMABLE-DELAY SUPERVISORY CIRCUIT

**Check for Samples: TPS3808-Q1**

## FEATURES

- **Qualified for Automotive Applications**
- **Power-On Reset Generator With Adjustable Delay Time: 1.25 ms to 10 s**
- **Very Low Quiescent Current: 2.4 µA Typ**
- **High Threshold Accuracy: 0.5% Typ**
- **Fixed Threshold Voltages for Standard Voltage Rails From 1.2 V to 5 V and Adjustable Voltage Down to 0.4 V Are Available**
- **Manual Reset ($\overline{MR}$) Input**
- **Open-Drain $\overline{RESET}$ Output**
- **Temperature Range: –40°C to 125°C**
- **Small SOT-23 Package**

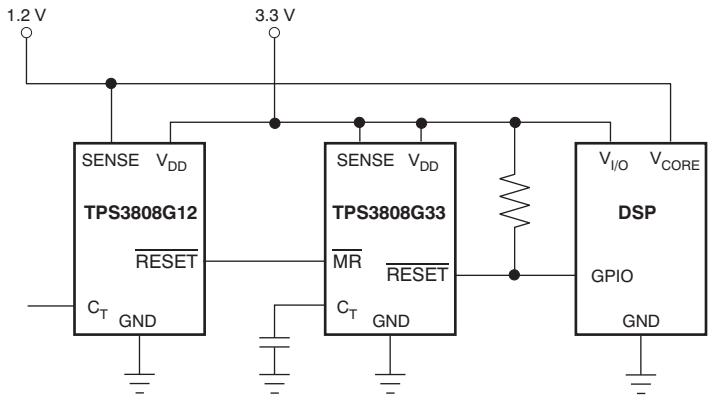
## APPLICATIONS

- **DSP or Microcontroller Applications**
- **Notebook/Desktop Computers**
- **PDAs/Hand-Held Products**
- **Portable/Battery-Powered Products**
- **FPGA/ASIC Applications**

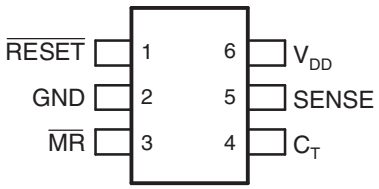
## DESCRIPTION

The TPS3808 microprocessor supervisory circuits monitor system voltages from 0.4 V to 5 V, asserting an open-drain $\overline{RESET}$ signal when the SENSE voltage drops below a preset threshold or when the manual reset ($\overline{MR}$) pin drops to a logic low. The $\overline{RESET}$ output remains low for the user-adjustable delay time after the SENSE voltage and $\overline{MR}$ return above their thresholds.

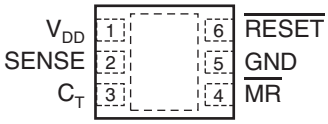
The TPS3808 uses a precision reference to achieve 0.5% threshold accuracy for $V_{IT} \leq 3.3$ V. The reset delay time can be set to 20 ms by disconnecting the $C_T$ pin, 300 ms by connecting the $C_T$ pin to $V_{DD}$ using a resistor, or can be user adjusted between 1.25 ms and 10 s by connecting the $C_T$ pin to an external capacitor. The TPS3808 has a very low typical quiescent current of 2.4 µA, so it is well suited to battery-powered applications. It is available in a small SOT-23 package and is fully specified over a temperature range of –40°C to 125°C ($T_J$).




**DBV (SOT-23) PACKAGE**
**(TOP VIEW)**




**DRV PACKAGE**
**(TOP VIEW)**



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION(1)

| $T_J$ | NOMINAL SUPPLY VOLTAGE | THRESHOLD VOLTAGE ($V_{IT}$) | PACKAGE(2) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|---|---|
| –40°C to 125°C | Adjustable | 0.405 V | SON – DRV | Reel of 3000 | TPS3808G01QDRVRQ1 | PSJQ |
| | | | SOT-23 – DBV | Reel of 3000 | TPS3808G01QDBVRQ1 | BAZ |
| | 1.25 V | 1.16 V | SOT-23 – DBV | Reel of 3000 | TPS3808G125QDBVRQ1 | QWZ |
| | 1.2 V | 1.12 V | | | TPS3808G12QDBVRQ1 | CEM |
| | 1.5 V | 1.4 V | | | TPS3808G15QDBVRQ1 | OFR |
| | 1.8 V | 1.67 V | | | TPS3808G18QDBVRQ1 | OBZ |
| | 3 V | 2.79 V | | | TPS3808G30QDBVRQ1 | AVP |
| | 3.3 V | 3.07 V | | | TPS3808G33QDBVRQ1 | AVQ |
| | 5 V | 4.65 V | | | TPS3808G50QDBVRQ1 | CEL |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

## ABSOLUTE MAXIMUM RATINGS

over operating junction temperature range (unless otherwise noted)(1)

| | | | | |
|---|---|---|---|---|
| $V_{DD}$ | Input voltage range | | | –0.3 V to 7 V |
| $V_{CT}$ | $C_T$ voltage range | | | –0.3 V to ($V_{DD}$ + 0.3) V |
| $V_{MR}$, $V_{RESET}$, $V_{SENSE}$ | $\overline{MR}$, $\overline{RESET}$, SENSE voltage ranges | | | –0.3 V to 7 V |
| $I_{RESET}$ | $\overline{RESET}$ pin current | | | 5 mA |
| $T_J$ | Operating junction temperature range(2) | | | –40°C to 150°C |
| $T_{stg}$ | Storage temperature range | | | –65°C to 150°C |
| ESD | Electrostatic discharge rating | Human-Body Model (HBM) | | 2 kV |
| | | Charged-Device Model (CDM) | TPS3808GXX | 500 V |
| | | | TPS3808G125QDBVRQ1 | 1000 V |
| | | Machine Model (MM), TPS3808G01QDRVRQ1,TPS3808G125QDBVRQ1 | | 50 V |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the *Electric Characteristics* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Due to the low dissipated power in this device, it is assumed that $T_J = T_A$.

## ELECTRICAL CHARACTERISTICS

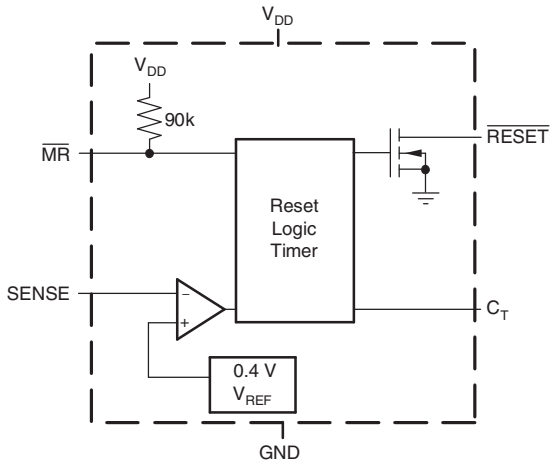
1.8 V ≤ $V_{DD}$ ≤ 6.5 V, $R_{LRESET}$ = 100 kΩ, $C_{LRESET}$ = 50 pF, over operating temperature range ($T_J$ = –40°C to 125°C) (unless otherwise noted), typical values at $T_J$ = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{DD}$ | Input supply range | | | 1.8 | | 6.5 | V |
| $I_{DD}$ | Supply current (into $V_{DD}$ pin) | $V_{DD}$ = 3.3 V, $\overline{RESET}$ not asserted, $\overline{MR}$, $\overline{RESET}$, $C_T$ open | | | 2.4 | 5 | µA |
| | | $V_{DD}$ = 6.5 V, $\overline{RESET}$ not asserted, $\overline{MR}$, $\overline{RESET}$, $C_T$ open | | | 2.7 | 6 | |
| $V_{OL}$ | Low-level output voltage | 1.3 V ≤ $V_{DD}$ < 1.8 V, $I_{OL}$ = 0.4 mA | | | | 0.3 | V |
| | | 1.8 V ≤ $V_{DD}$ ≤ 6.5 V, $I_{OL}$ = 1 mA | | | | 0.4 | |
| | Power-up reset voltage(1) | $V_{OL}$ (max) = 0.2 V, I $\overline{RESET}$ = 15 µA | | | | 0.8 | V |
| $V_{IT}$ | Negative-going input threshold accuracy | TPS3808G01 | | –2 | ±1 | +2 | % |
| | | $V_{IT}$ ≤ 3.3 V | | –1.5 | ±0.5 | +1.5 | |
| | | 3.3 V < $V_{IT}$ ≤ 5 V | | –2 | ±1 | +2 | |
| | | $V_{IT}$ ≤ 3.3 V | –40°C < $T_J$ < 85°C | –1.25 | ±0.5 | +1.25 | |
| | | 3.3 V < $V_{IT}$ ≤ 5 V | | –1.5 | ±0.5 | +1.5 | |
| $V_{HYS}$ | Hysteresis on $V_{IT}$ pin | TPS3808G01 | | | 1.5 | 3 | %$V_{IT}$ |
| | | –40°C < $T_J$ < 85°C | | | 1 | 2 | |
| | | | | | 1 | 2.5 | |
| $R_{\overline{MR}}$ | $\overline{MR}$ internal pullup resistance | $V_{SENSE}$ = $V_{IT}$ | | 70 | 90 | | kΩ |
| $I_{SENSE}$ | Input current at SENSE pin | TPS3808G01 | | –25 | | 25 | nA |
| | | $V_{SENSE}$ = 6.5 V | | | 1.7 | | µA |
| $I_{OH}$ | $\overline{RESET}$ leakage current | V $\overline{RESET}$ = 6.5 V, $\overline{RESET}$ not asserted | | | | 300 | nA |
| $C_{IN}$ | Input capacitance, any pin | $C_T$ pin | $V_{IN}$ = 0 V to $V_{DD}$ | | 5 | | pF |
| | | Other pins | $V_{IN}$ = 0 V to 6.5 V | | 5 | | |
| $V_{IL}$ | $\overline{MR}$ logic low input | | | 0 | | 0.3 $V_{DD}$ | V |
| $V_{IH}$ | $\overline{MR}$ logic high input | | | 0.7 $V_{DD}$ | | $V_{DD}$ | V |
| $t_w$ | Maximum transient duration | SENSE | $V_{IH}$ = 1.05 $V_{IT}$, $V_{IL}$ = 0.95 $V_{IT}$ | | 20 | | µs |
| | | $\overline{MR}$ | $V_{IH}$ = 0.7 $V_{DD}$, $V_{IL}$ = 0.3 $V_{DD}$ | | 0.001 | | |
| $t_d$ | $\overline{RESET}$ delay time | $C_T$ = Open | See timing diagram | 12 | 20 | 28 | ms |
| | | $C_T$ = $V_{DD}$ | | 180 | 300 | 420 | |
| | | $C_T$ = 100 pF | | 0.75 | 1.25 | 1.75 | |
| | | $C_T$ = 180 nF | | 0.7 | 1.2 | 1.7 | s |
| $t_{pHL}$ | Propagation delay | $\overline{MR}$ to $\overline{RESET}$ | $V_{IH}$ = 0.7 $V_{DD}$, $V_{IL}$ = 0.3 $V_{DD}$ | | 150 | | ns |
| | High-level to low-level $\overline{RESET}$ delay | SENSE to $\overline{RESET}$ | $V_{IH}$ = 1.05 $V_{IT}$, $V_{IL}$ = 0.95 $V_{IT}$ | | 20 | | µs |
| $\theta_{JA}$ | Thermal resistance, junction to ambient | | | | 290 | | °C/W |

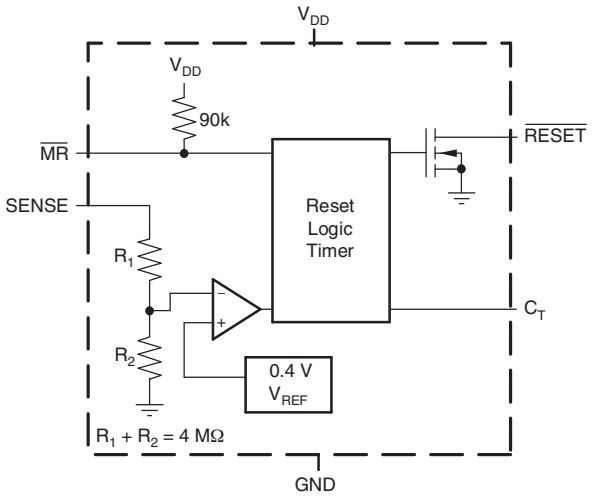
(1) Power-up reset voltage is the lowest supply voltage ($V_{DD}$) at which $\overline{RESET}$ becomes active ($t_{rise(VDD)}$ ≥ 15 µs/V).

## FUNCTIONAL BLOCK DIAGRAMS

**Adjustable-Voltage Version**

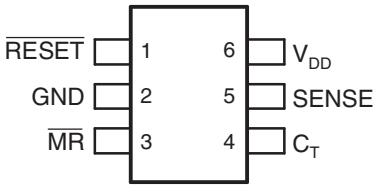



**Fixed-Voltage Versions**

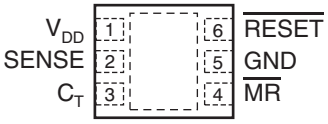



## PIN ASSIGNMENTS

**DBV (SOT-23) PACKAGE**
**(TOP VIEW)**




**DRV PACKAGE**
**(TOP VIEW)**




### PIN FUNCTIONS

| PIN | | DESCRIPTION |
|---|---|---|
| NAME | NO. | |
| $\overline{RESET}$ | 1 | Reset. This is an open-drain output that is driven to a low impedance state when $\overline{RESET}$ is asserted (either the SENSE input is lower than the threshold voltage ($V_{IT}$) or the $\overline{MR}$ pin is set to a logic low). $\overline{RESET}$ remains low (asserted) for the reset period after both SENSE is above $V_{IT}$ and $\overline{MR}$ is set to a logic high. A pullup resistor from 10 kΩ to 1 MΩ should be used on this pin, and allows the reset pin to attain voltages higher than $V_{DD}$. |
| GND | 2 | Ground |
| $\overline{MR}$ | 3 | Manual reset. Driving this pin low asserts $\overline{RESET}$. $\overline{MR}$ is internally tied to $V_{DD}$ by a 90-kΩ pullup resistor. |
| $C_T$ | 4 | Reset period programming. Connecting this pin to $V_{DD}$ through a 40-kΩ to 200-kΩ resistor or leaving it open results in fixed delay times (see *Electrical Characteristics*). Connecting this pin to a ground referenced capacitor ≥ 100 pF gives a user-programmable delay time. |
| SENSE | 5 | Voltage sense. This pin is connected to the voltage to be monitored. If the voltage at this terminal drops below the threshold voltage ($V_{IT}$), $\overline{RESET}$ is asserted. |
| $V_{DD}$ | 6 | Supply voltage. It is good analog design practice to place a 0.1-μF ceramic capacitor close to this pin. |

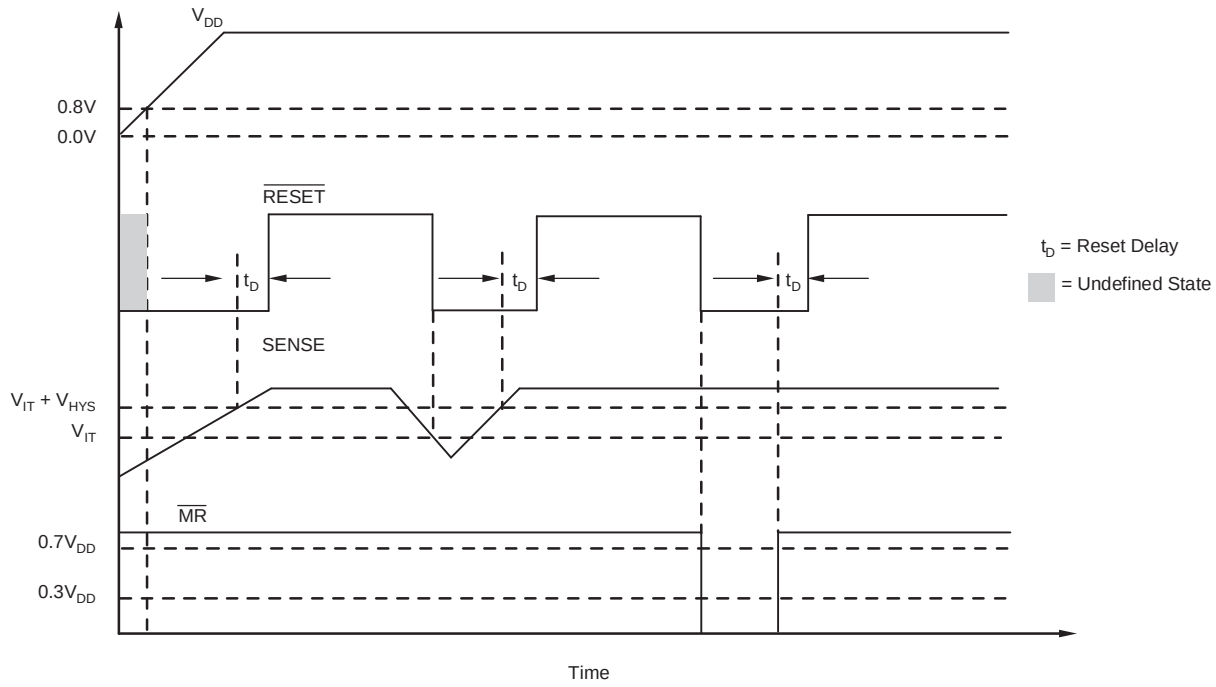



**Figure 1. $\overline{MR}$ and SENSE Reset Timing Diagram**

**TRUTH TABLE**

| $\overline{MR}$ | SENSE > $V_{IT}$ | $\overline{RESET}$ |
|---|---|---|
| L | 0 | L |
| L | 1 | L |
| H | 0 | L |
| H | 1 | H |

## TYPICAL CHARACTERISTICS

At $T_J$ = 25°C, $V_{DD}$ = 3.3 V, $R_{LRESET}$ = 100 kΩ, and $C_{LRESET}$ = 50 pF (unless otherwise noted)

**SUPPLY CURRENT vs SUPPLY VOLTAGE**

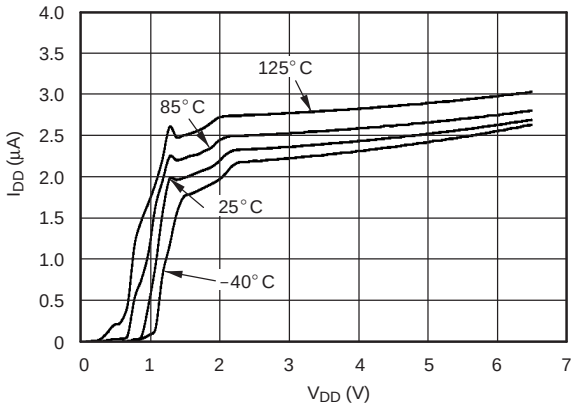



**Figure 2.**

**$\overline{\text{RESET}}$ TIMEOUT PERIOD vs $C_T$**

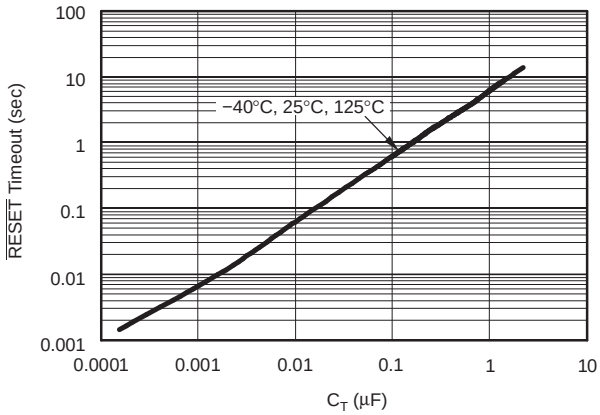



**Figure 3.**

**NORMALIZED $\overline{\text{RESET}}$ TIMEOUT PERIOD vs TEMPERATURE ($C_T$ = OPEN, $C_T$ = $V_{DD}$, $C_T$ = Any)**

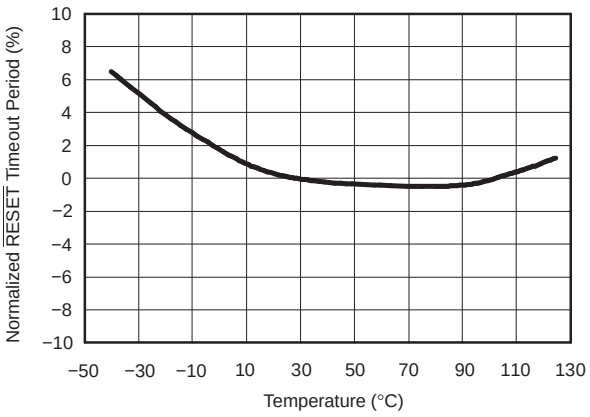



**Figure 4.**

**MAXIMUM TRANSIENT DURATION AT SENSE vs SENSE THRESHOLD OVERDRIVE VOLTAGE**

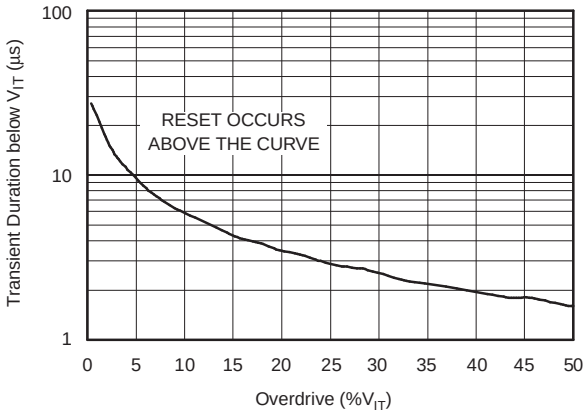



**Figure 5.**

## TYPICAL CHARACTERISTICS (continued)

At $T_J$ = 25°C, $V_{DD}$ = 3.3 V, $R_{LRESET}$ = 100 kΩ, and $C_{LRESET}$ = 50 pF (unless otherwise noted)

**NORMALIZED SENSE THRESHOLD VOLTAGE ($V_{IT}$) vs TEMPERATURE**

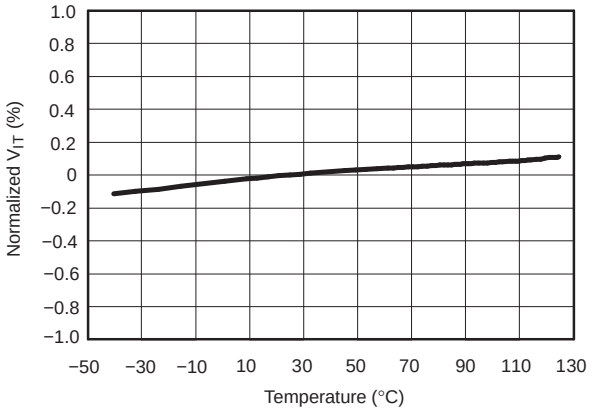



**Figure 6.**

**LOW-LEVEL $\overline{\text{RESET}}$ VOLTAGE vs $\overline{\text{RESET}}$ CURRENT**

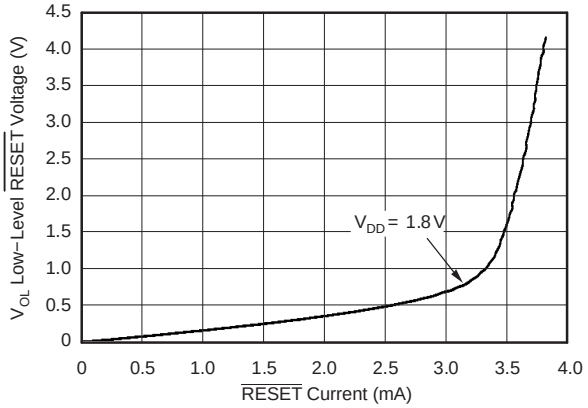



**Figure 7.**

**LOW-LEVEL $\overline{\text{RESET}}$ VOLTAGE vs $\overline{\text{RESET}}$ CURRENT**

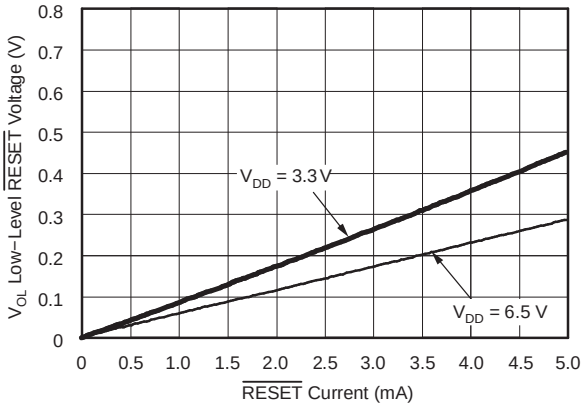



**Figure 8.**

## DEVICE OPERATION

The TPS3808 microprocessor supervisory product family is designed to assert a $\overline{\text{RESET}}$ signal when either the SENSE pin voltage drops below $V_{IT}$ or the manual reset ($\overline{\text{MR}}$) is driven low. The $\overline{\text{RESET}}$ output remains asserted for a user-adjustable time after both the manual reset ($\overline{\text{MR}}$) and SENSE voltages return above the respective thresholds. A broad range of voltage threshold and reset delay time adjustments are available, allowing these devices to be used in a wide array of applications. Reset threshold voltages can be factory-set from 0.82 V to 3.3 V or from 4.4 V to 5.0 V, while the TPS3808G01 can be set to any voltage above 0.405 V using an external resistor divider. Two preset delay times are also user-selectable: connecting the $C_T$ pin to $V_{DD}$ results in a 300-ms reset delay, while leaving the $C_T$ pin open yields a 20-ms reset delay. In addition, connecting a capacitor between $C_T$ and GND allows the designer to select any reset delay period from 1.25 ms to 10 s.

### SENSE Input

The SENSE input provides a terminal at which any system voltage can be monitored. If the voltage on this pin drops below $V_{IT}$, $\overline{\text{RESET}}$ is asserted. The comparator has a built-in hysteresis to ensure smooth $\overline{\text{RESET}}$ assertions and deassertions. It is good analog design practice to put a 1-nF to 10-nF bypass capacitor on the SENSE input to reduce sensitivity to transients and layout parasitics.

The TPS3808G01 can be used to monitor any voltage rail down to 0.405 V using the circuit shown in Figure 9.

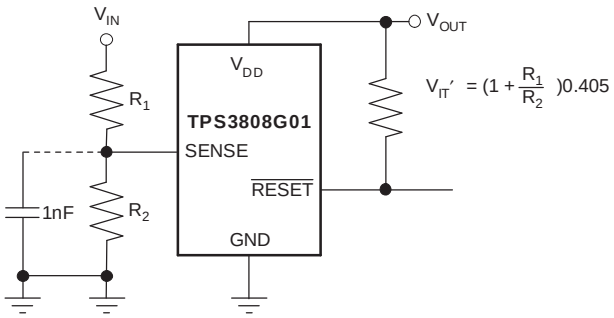



**Figure 9. Using the TPS3808G01 to Monitor a User-Defined Threshold Voltage**

### Manual Reset ($\overline{\text{MR}}$) Input

The manual reset ($\overline{\text{MR}}$) input allows a processor or other logic circuits to initiate a reset. A logic low (0.3 $V_{DD}$) on $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to assert. After $\overline{\text{MR}}$ returns to a logic high and SENSE is above its reset threshold, $\overline{\text{RESET}}$ is deasserted after the user-defined reset delay expires. Note that $\overline{\text{MR}}$ is internally tied to $V_{DD}$ using a 90-kΩ resistor, so this pin can be left unconnected if $\overline{\text{MR}}$ is not used.

Refer to Figure 10 for how $\overline{\text{MR}}$ can be used to monitor multiple system voltages. Note that if the logic signal driving $\overline{\text{MR}}$ does not go fully to $V_{DD}$, there will be some additional current draw into $V_{DD}$ as a result of the internal pullup resistor on $\overline{\text{MR}}$. To minimize current draw, a logic-level FET can be used as shown in Figure 11.

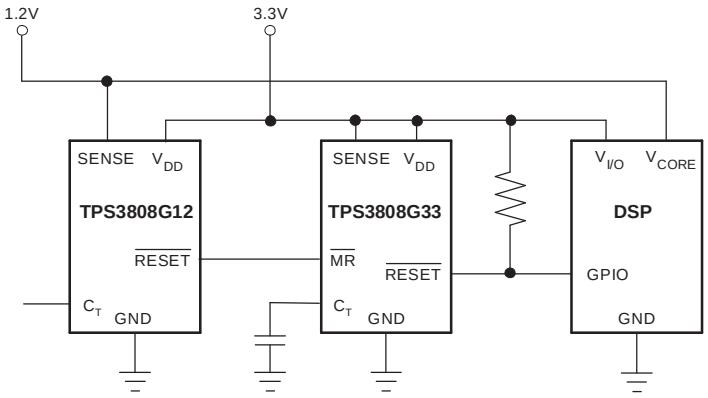



**Figure 10. Using $\overline{\text{MR}}$ to Monitor Multiple System Voltages**

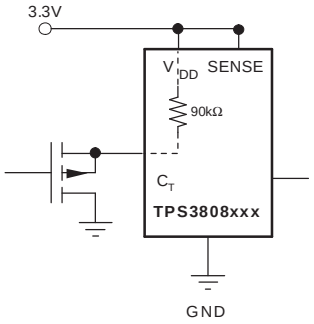



**Figure 11. Using an External MOSFET to Minimize $I_{DD}$ When $\overline{MR}$ Signal Does Not Go to $V_{DD}$**

## Selecting the Reset Delay Time

The TPS3808 has three options for setting the $\overline{RESET}$ delay time as shown in Figure 12. Figure 12a shows the configuration for a fixed 300-ms typical delay time by tying $C_T$ to $V_{DD}$; a resistor from 40 kΩ to 200 kΩ must be used. Supply current is not affected by the choice of resistor. Figure 12b shows a fixed 20-ms delay time by leaving the $C_T$ pin open. Figure 12c shows a ground referenced capacitor connected to $C_T$ for a user-defined program time between 1.25 ms and 10 s.

The capacitor $C_T$ should be ≥100 pF nominal value in order for the TPS3808 to recognize that the capacitor is present. The capacitor value for a given delay time can be calculated using the following equation:

$$C_T\,(nF) = \left[t_D\,(s) - 0.5 \times 10^{-3}\,(s)\right] \times 175 \quad (1)$$

The reset delay time is determined by the time it takes an on-chip precision 220-nA current source to charge the external capacitor to 1.23 V. When a $\overline{RESET}$ is asserted, the capacitor is discharged. When the $\overline{RESET}$ conditions are cleared, the internal current source is enabled and begins to charge the external capacitor. When the voltage on this capacitor reaches 1.23 V, $\overline{RESET}$ is deasserted. Note that a low-leakage type capacitor such as a ceramic should be used and that stray capacitance around this pin may cause errors in the reset delay time.

## Immunity to SENSE Pin Voltage Transients

The TPS3808 is relatively immune to short negative transients on the SENSE pin. Sensitivity to transients is dependent on threshold overdrive, as shown in the *Maximum Transient Duration at Sense vs Sense Threshold Overdrive Voltage* graph (Figure 5) in the Typical Characteristics section.

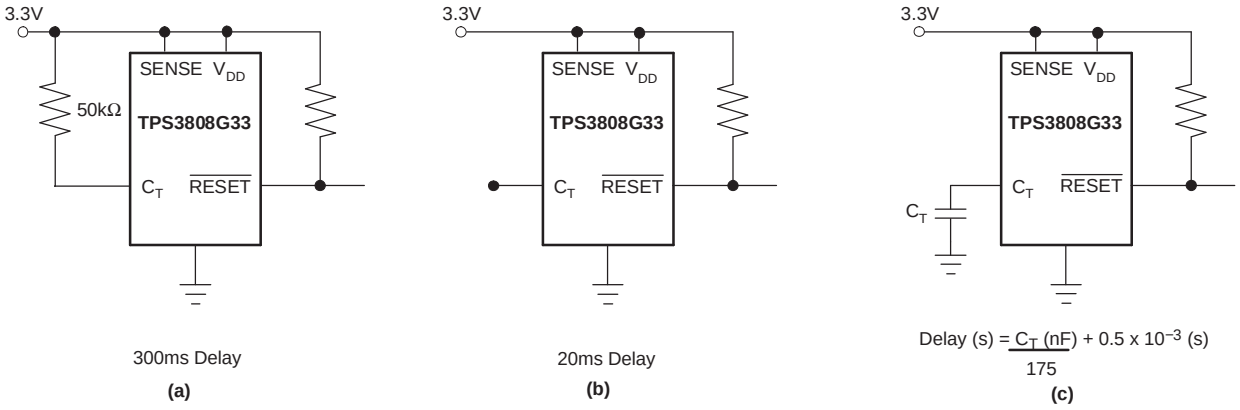



**Figure 12. Configuration Used to Set the $\overline{RESET}$ Delay Time**

## REVISION HISTORY

| Changes from Revision G (November, 2010) to Revision H | Page |
|---|---|
| • Changed $I_{SENSE}$ from µA to nA | 3 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS3808G01QDBVRQ1 | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | BAZ | Samples |
| TPS3808G01QDRVRQ1 | ACTIVE | SON | DRV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PSJQ | Samples |
| TPS3808G125QDBVRQ1 | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | QWZ | Samples |
| TPS3808G12QDBVRQ1 | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CEM | Samples |
| TPS3808G15QDBVRQ1 | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | OFV | Samples |
| TPS3808G18QDBVRQ1 | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | OBZ | Samples |
| TPS3808G30QDBVRQ1 | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AVP | Samples |
| TPS3808G33QDBVRQ1 | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AVQ | Samples |
| TPS3808G50QDBVRQ1 | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | CEL | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.



**OTHER QUALIFIED VERSIONS OF TPS3808G01-Q1, TPS3808G12-Q1, TPS3808G125-Q1, TPS3808G15-Q1, TPS3808G18-Q1, TPS3808G30-Q1, TPS3808G33-Q1, TPS3808G50-Q1 :**

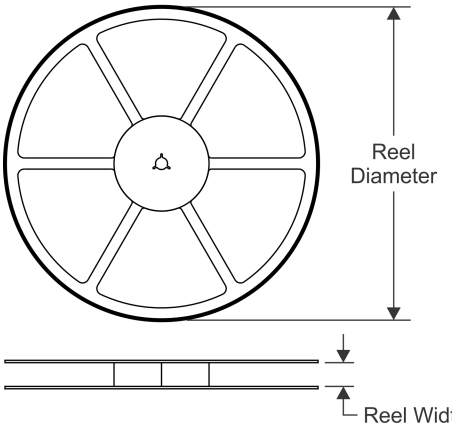
- Catalog: TPS3808G01, TPS3808G12, TPS3808G125, TPS3808G15, TPS3808G18, TPS3808G30, TPS3808G33, TPS3808G50

NOTE: Qualified Version Definitions:

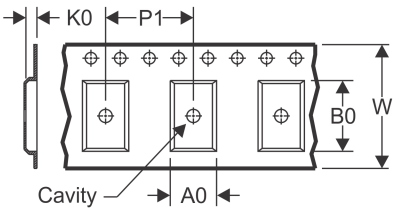
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

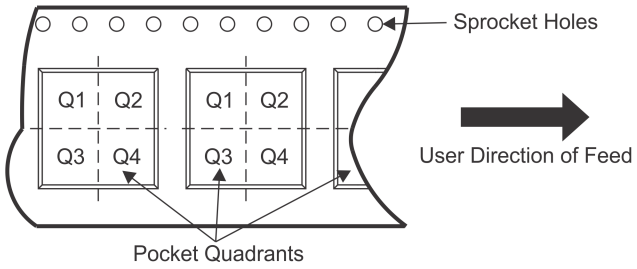



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

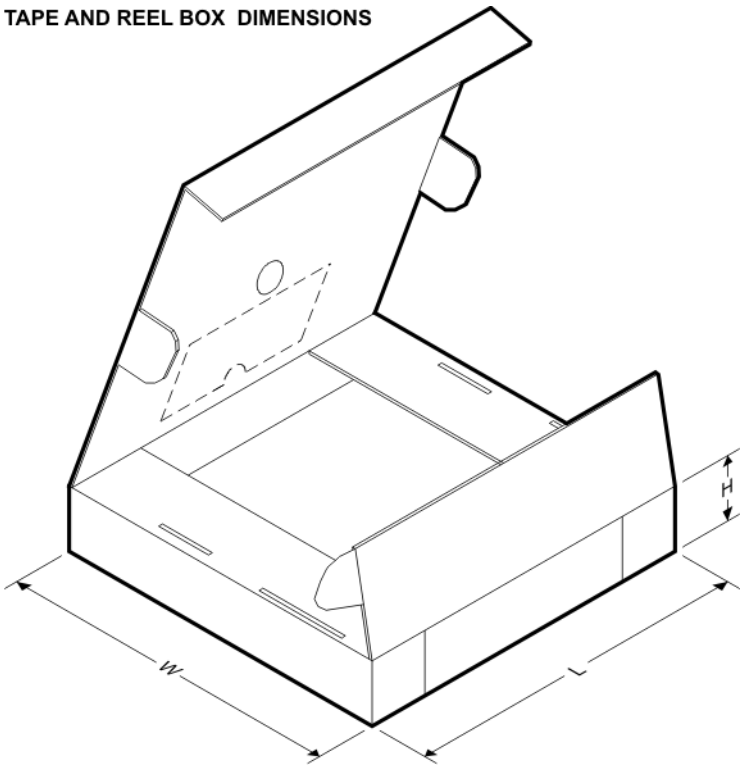
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS3808G01QDBVRQ1 | SOT-23 | DBV | 6 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS3808G01QDRVRQ1 | SON | DRV | 6 | 3000 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| TPS3808G125QDBVRQ1 | SOT-23 | DBV | 6 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS3808G12QDBVRQ1 | SOT-23 | DBV | 6 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS3808G15QDBVRQ1 | SOT-23 | DBV | 6 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS3808G18QDBVRQ1 | SOT-23 | DBV | 6 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS3808G30QDBVRQ1 | SOT-23 | DBV | 6 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS3808G33QDBVRQ1 | SOT-23 | DBV | 6 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS3808G50QDBVRQ1 | SOT-23 | DBV | 6 | 3000 | 179.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

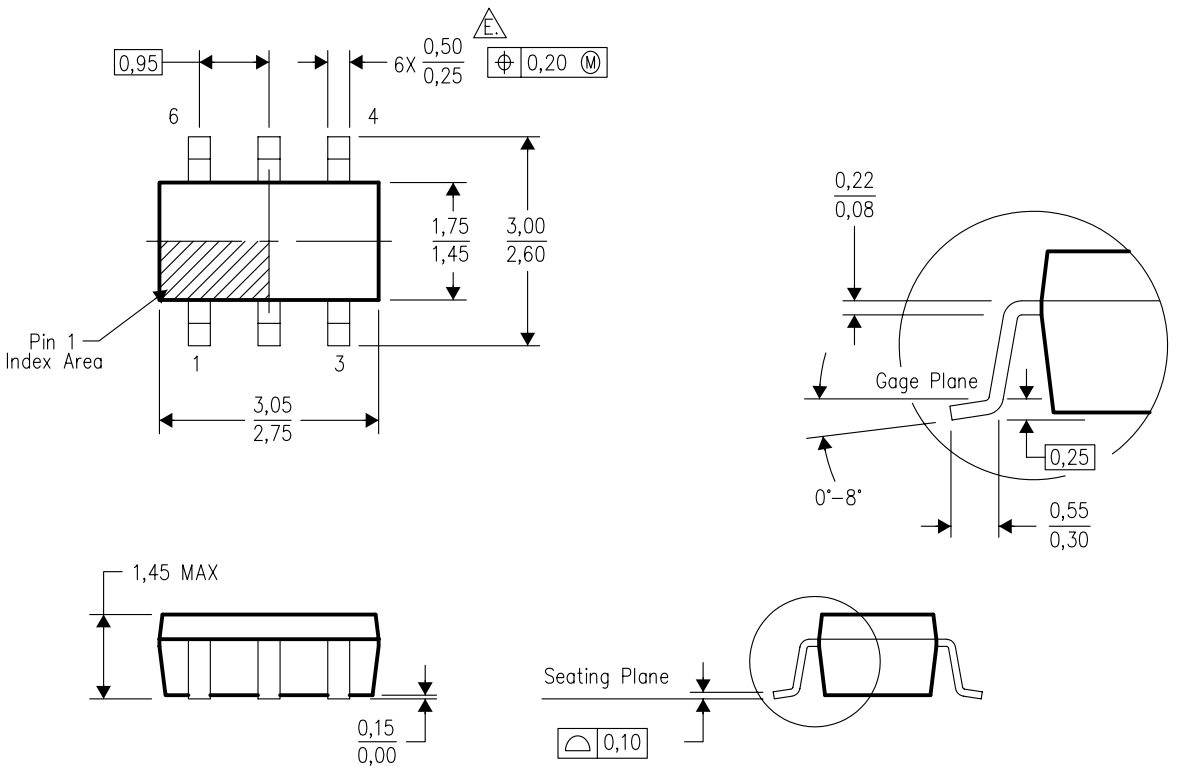
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS3808G01QDBVRQ1 | SOT-23 | DBV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS3808G01QDRVRQ1 | SON | DRV | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS3808G125QDBVRQ1 | SOT-23 | DBV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS3808G12QDBVRQ1 | SOT-23 | DBV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS3808G15QDBVRQ1 | SOT-23 | DBV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS3808G18QDBVRQ1 | SOT-23 | DBV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS3808G30QDBVRQ1 | SOT-23 | DBV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS3808G33QDBVRQ1 | SOT-23 | DBV | 6 | 3000 | 203.0 | 203.0 | 35.0 |
| TPS3808G50QDBVRQ1 | SOT-23 | DBV | 6 | 3000 | 203.0 | 203.0 | 35.0 |

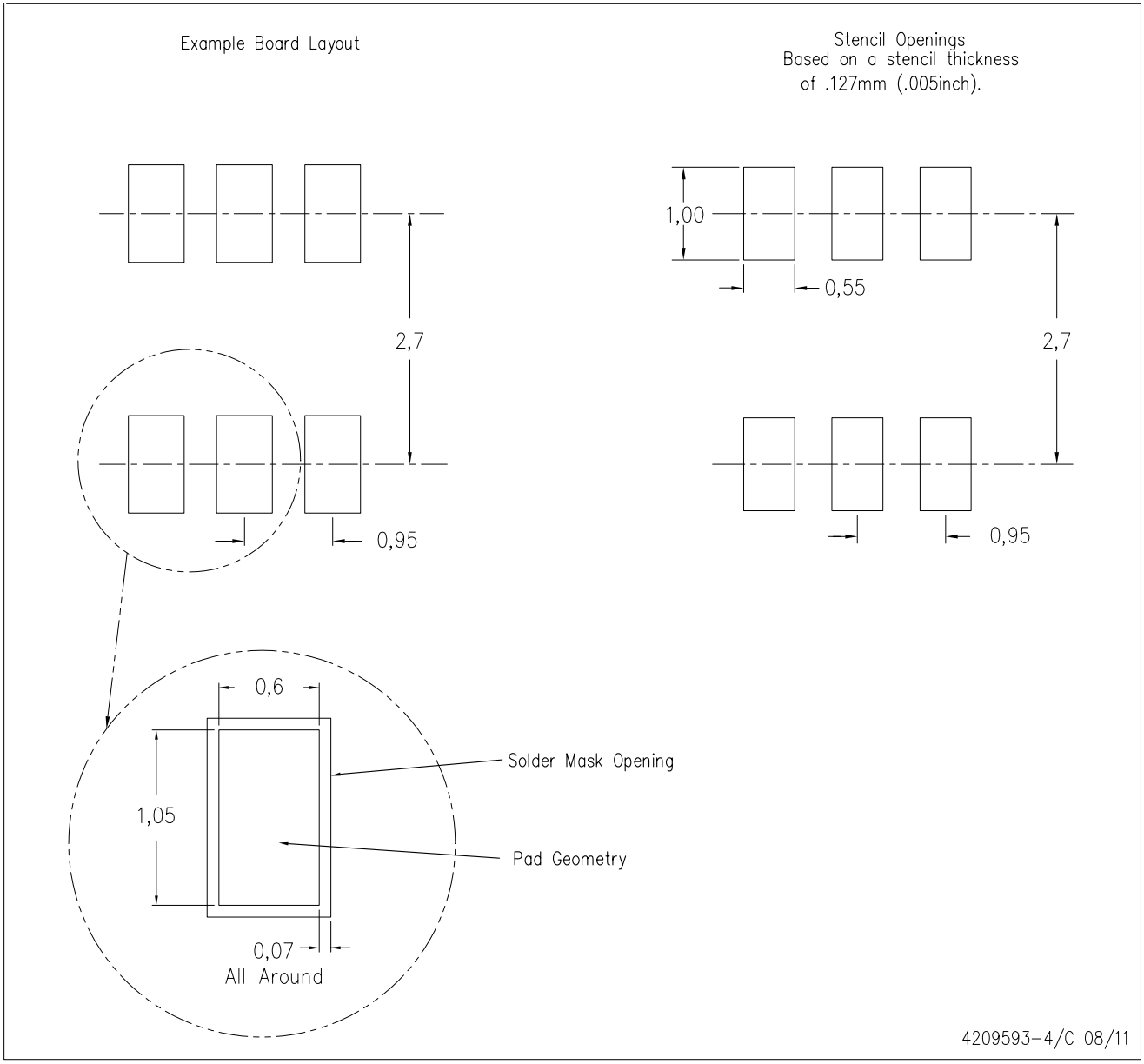
## DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE




4073253–5/K 03/2006

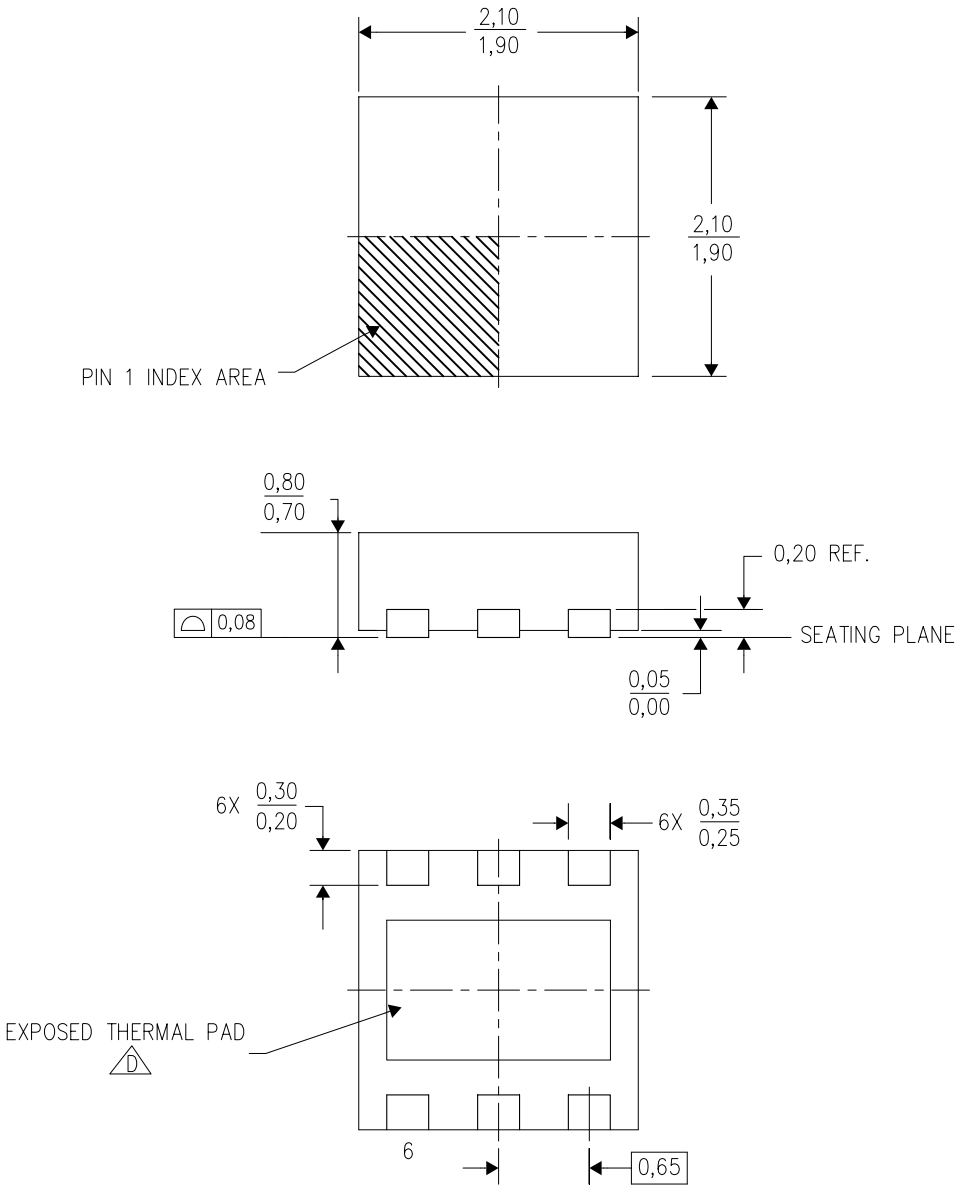
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD




4206925/E 10/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

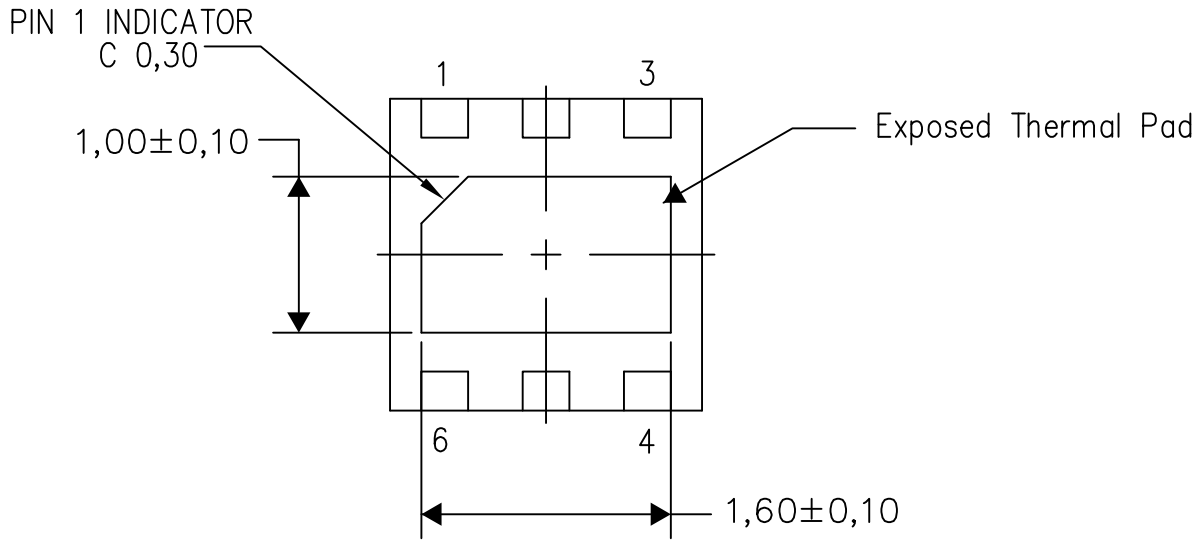
DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



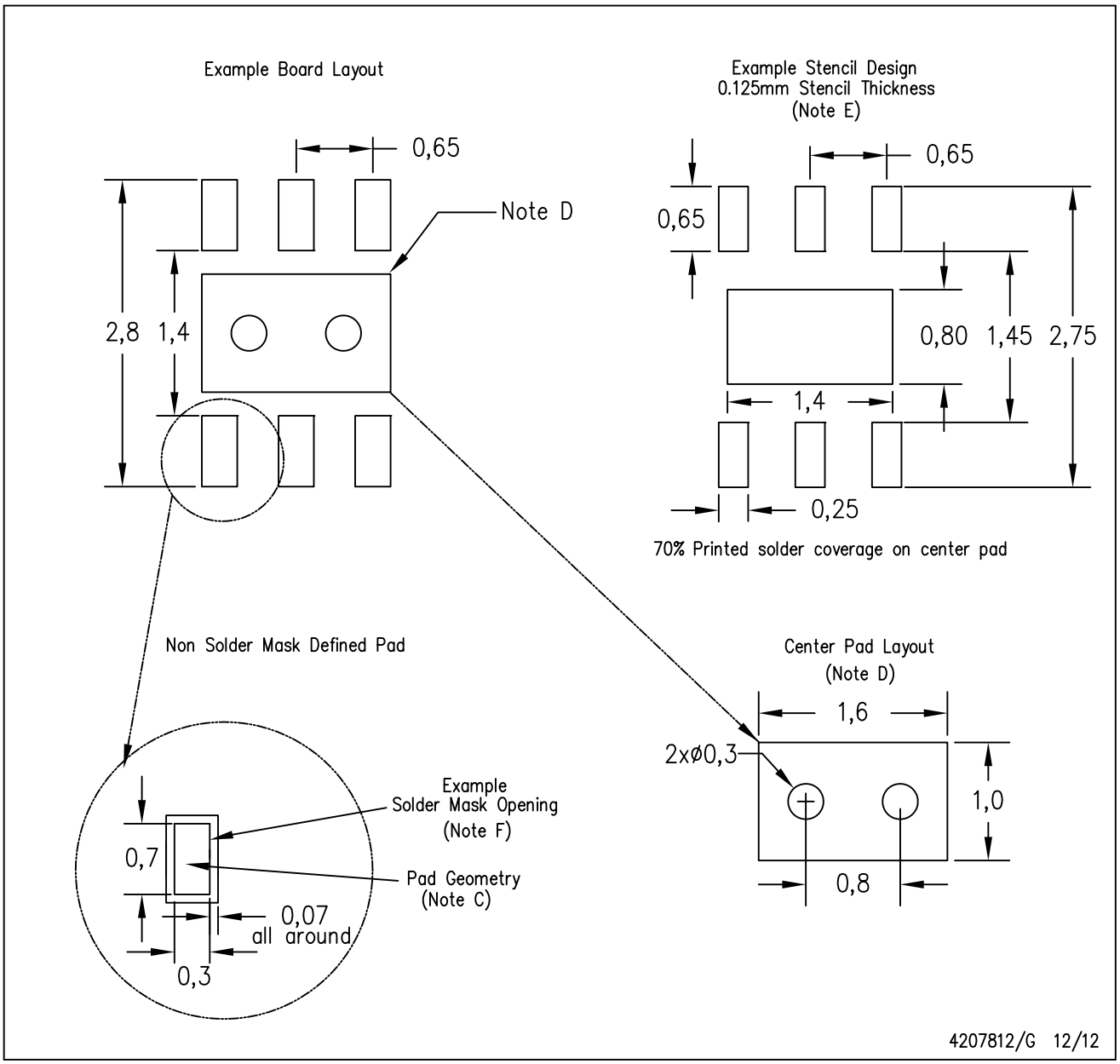

Bottom View

Exposed Thermal Pad Dimensions

4206926/N 03/13

NOTE: All linear dimensions are in millimeters

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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