Low-Noise, Wide-Bandwidth, High PSRR, Low-Dropout 1A Linear Regulator

Check for Samples: TPS7A80xx

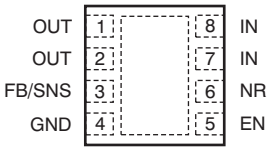
FEATURES

- **Low-Dropout 1A Regulator with Enable**
- **Available in Multiple Output Versions:**
  - **Fixed Output Voltages: 0.8V to 5.0V Using Innovative Factory EEPROM Programming**
  - **Adjustable Output Voltages: 0.8V to 6.0V**
- **Wide-Bandwidth High PSRR:**
  - **63dB at 1kHz**
  - **57dB at 100kHz**
  - **38dB at 1MHz**
- **Low Noise: (12.6 × V_{OUT} + 13.5) μV_{RMS} typical (100Hz to 100kHz)**
- **Stable with a 4.7µF Ceramic Capacitor**
- **Excellent Load/Line Transient Response**
- **3% Overall Accuracy (over Load/Line/Temp)**
- **Over-Current and Over-Temperature Protection**
- **Very Low Dropout: 170mV Typical at 1A**
- **3mm × 3mm SON-8 DRB Package**

APPLICATIONS

- **Telecom Infrastructure**
- **Audio**
- **High-Speed I/F (PLL/VCO)**

DRB PACKAGE
3mm x 3mm SON
(TOP VIEW)



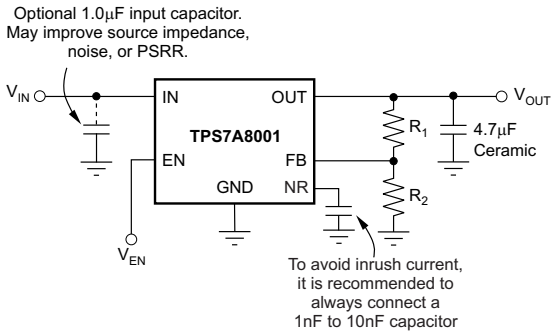
DESCRIPTION

The TPS7A80xx family of low-dropout linear regulators (LDOs) offer very high power-supply ripple rejection (PSRR) at the output. This series of LDOs uses an advanced BiCMOS process and a PMOSFET pass device to achieve very low noise, excellent transient response, and excellent PSRR performance.

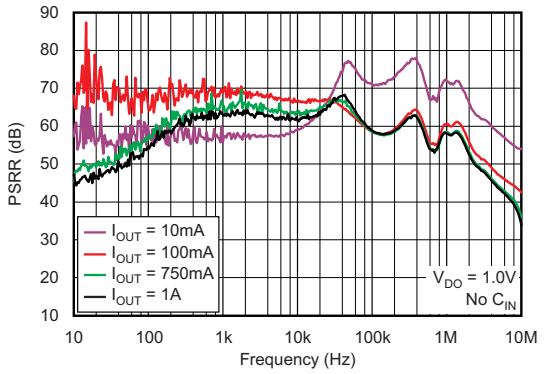
The TPS7A80xx is stable with a 4.7µF ceramic output capacitor, and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 3% over all load, line, process, and temperature variations.

This device is fully specified over the temperature range of T_J = –40°C to +125°C and is offered in a 3mm × 3mm, SON-8 package with a thermal pad.

Typical Application Circuit for Adjustable Voltage Versions



TYPICAL POWER-SUPPLY RIPPLE REJECTION



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT}(2)
TPS7A80**xxyyyz**	**XX** is nominal output voltage (for example, 28 = 2.8V, 285 = 2.85V, 01 = Adjustable). **YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 0.9V to 5.0V in 50mV increments are available through the use of innovative factory EEPROM programming; minimum order quantities may apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE		UNIT
		MIN	MAX	
Voltage	IN	–0.3	+7.0	V
	FB, NR	–0.3	+3.6	V
	EN	–0.3	V_{IN} + 0.3(2)	V
	OUT	–0.3	+7.0	V
Current	OUT	Internally Limited		A
Temperature	Operating virtual junction, T_J	–55	+150	°C
	Storage, T_{stg}	–55	+150	°C
Electrostatic discharge (ESD) rating(3)	Human body model (HBM) QSS 009-105 (JESD22-A114A)		2	kV
	Charged device model (CDM) QSS 009-147 (JESD22-C101B.01)		500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) V_{EN} absolute maximum rating is V_{IN} + 0.3V or +7.0V, whichever is smaller.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL INFORMATION

THERMAL METRIC(1)(2)		TPS7A80xx DRB(3) 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(4)	47.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(5)	53.9	
θ_{JB}	Junction-to-board thermal resistance(6)	23.4	
ψ_{JT}	Junction-to-top characterization parameter(7)	1.0	
ψ_{JB}	Junction-to-board characterization parameter(8)	23.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(9)	7.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953A.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.
(3) Thermal data for the DRB package are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
  (a) The exposed pad is connected to the PCB ground layer through a 2×2 thermal via array.
  (b) The top and bottom copper layers are assumed to have a 5% thermal conductivity of copper representing a 20% copper coverage.
  (c) This data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3in × 3in copper area. To understand the effects of the copper area on thermal performance, refer to the *Power Dissipation* and *Estimating Junction Temperature* sections.
(4) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(5) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the top of the package. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(6) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(7) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(8) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(9) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

Over the operating temperature range of T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V (whichever is greater), I_{OUT} = 1mA, V_{EN} = 2.2V, C_{OUT} = 4.7µF, and C_{NR} = 0.01µF, unless otherwise noted. TPS7A8001 is tested at V_{OUT} = 0.8V and V_{OUT} = 6.0V. Typical values are at T_J = +25°C.

PARAMETER		TEST CONDITIONS		TPS7A80xx MIN	TPS7A80xx TYP	TPS7A80xx MAX	UNIT
V_{IN}	Input voltage range(1)			2.2		6.5	V
V_{NR}	Internal reference			0.790	0.800	0.810	V
V_{OUT}	Output voltage range	TPS7A80xx (fixed versions)		0.8		5.0	V
		TPS7A8001 (adjustable version)		0.8		6.0	V
	Output accuracy(2)	V_{OUT} + 0.5V ≤ V_{IN} ≤ 6.0V, V_{IN} ≥ 2.5V, 100mA ≤ I_{OUT} ≤ 500mA, 0°C ≤ T_J ≤ 85°C		-2.0		+2.0	%
		V_{OUT} + 0.5V ≤ V_{IN} ≤ 6.5V, V_{IN} ≥ 2.2V, 100mA ≤ I_{OUT} ≤ 1A		–3.0	±0.3	+3.0	%
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	$V_{OUT(NOM)}$ + 0.5V ≤ V_{IN} ≤ 6.5V, V_{IN} ≥ 2.2V, I_{OUT} = 100mA			150		µV/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	100mA ≤ I_{OUT} ≤ 1A			2		µV/mA
V_{DO}	Dropout voltage(3)	V_{OUT} + 0.5V ≤ V_{IN} ≤ 6.5V, V_{IN} ≥ 2.2V, I_{OUT} = 500mA, V_{FB} = GND or V_{SNS} = GND				250	mV
		V_{OUT} + 0.5V ≤ V_{IN} ≤ 6.5V, V_{IN} ≥ 2.5V, I_{OUT} = 750mA, V_{FB} = GND or V_{SNS} = GND				350	mV
		V_{OUT} + 0.5V ≤ V_{IN} ≤ 6.5V, V_{IN} ≥ 2.5V, I_{OUT} = 1A, V_{FB} = GND or V_{SNS} = GND				500	mV
I_{CL}	Output current limit	V_{OUT} = 0.85 × $V_{OUT(NOM)}$, V_{IN} ≥ 3.3V		1100	1400	2000	mA
I_{GND}	Ground pin current	I_{OUT} = 1mA			60	100	µA
		I_{OUT} = 1A				350	µA
I_{SHDN}	Shutdown current (I_{GND})	V_{EN} ≤ 0.4V, V_{IN} ≥ 2.2V, R_L = 1kΩ, 0°C ≤ T_J ≤ 85°C			0.20	2	µA
I_{FB}	Feedback pin current	TPS7A8001 (adjustable), V_{IN} = 6.5V, V_{FB} = 0.8V			0.02	1.0	µA
I_{SNS}	Sense pin current	TPS7A80xx (fixed), V_{IN} = 6.5V, V_{SNS} = $V_{OUT(NOM)}$			0.02	1.0	µA
PSRR	Power-supply rejection ratio	V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 750mA	f = 100Hz		48		dB
			f = 1kHz		63		dB
			f = 10kHz		63		dB
			f = 100kHz		57		dB
			f = 1MHz		38		dB
V_N	Output noise voltage	BW = 100Hz to 100kHz, V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 100mA	C_{NR} = 0.001µF		15.6 × V_{OUT}		μV_{RMS}
			C_{NR} = 0.01µF		15.6 × V_{OUT}		μV_{RMS}
			C_{NR} = 0.1µF		15.1 × V_{OUT}		μV_{RMS}
$V_{EN(HI)}$	Enable high (enabled)	2.2V ≤ V_{IN} ≤ 3.6V, R_L = 1kΩ		1.2			V
		3.6V < V_{IN} ≤ 6.5V, R_L = 1kΩ		1.35			V
$V_{EN(LO)}$	Enable low (shutdown)	R_L = 1kΩ		0		0.4	V
$I_{EN(HI)}$	Enable pin current, enabled	V_{IN} = V_{EN} = 6.5V			0.02	1.0	µA
t_{STR}	Startup time	$V_{OUT(NOM)}$ = 3.3V, V_{OUT} = 0% to 90% $V_{OUT(NOM)}$, R_L = 3.3kΩ, C_{OUT} = 4.7µF	C_{NR} = 1nF		0.1		ms
			C_{NR} = 10nF		1.6		ms
UVLO	Undervoltage lockout	V_{IN} rising, R_L = 1kΩ		1.86	2	2.10	V
	Hysteresis	V_{IN} falling, R_L = 1kΩ			75		mV
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing			+160		°C
		Reset, temperature decreasing			+140		°C
T_J	Operating junction temperature			–40		+125	°C

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 2.2V, whichever is greater.
(2) As for TPS7A8001 (adjustable); it does not include external resistor tolerances and it is not tested at this condition: V_{OUT} = 0.8V, 4.5V ≤ V_{IN} ≤ 6.5V, and 750mA ≤ I_{OUT} ≤ 1A because of power dissipation higher than maximum rating of the package.
(3) V_{DO} is not measured for fixed output voltage devices with V_{OUT} < 1.7V because minimum V_{IN} = 2.2V.

FUNCTIONAL BLOCK DIAGRAMS

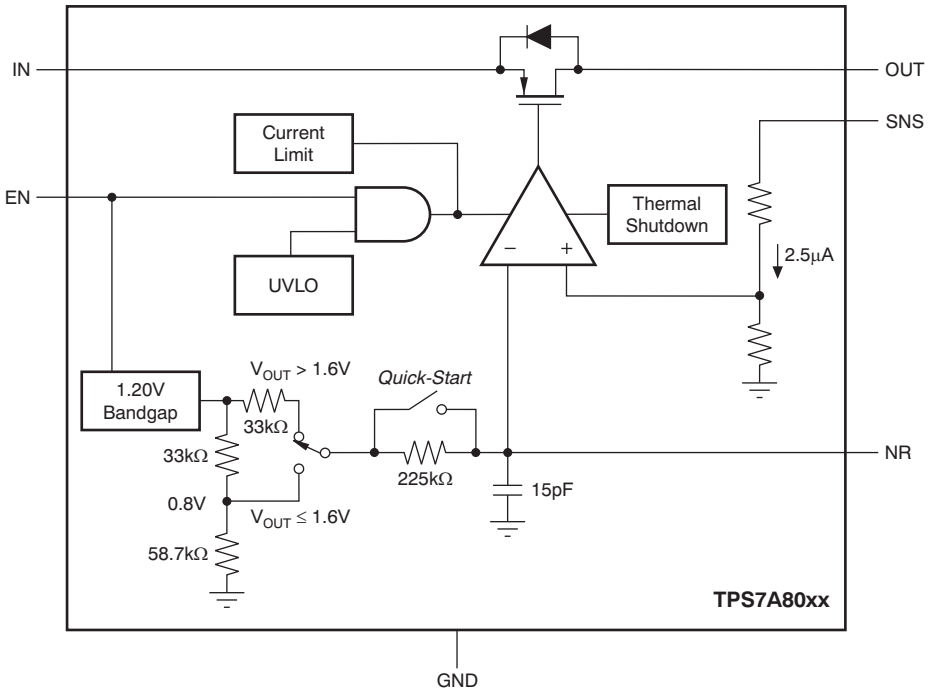


Figure 1. Fixed Voltage Versions

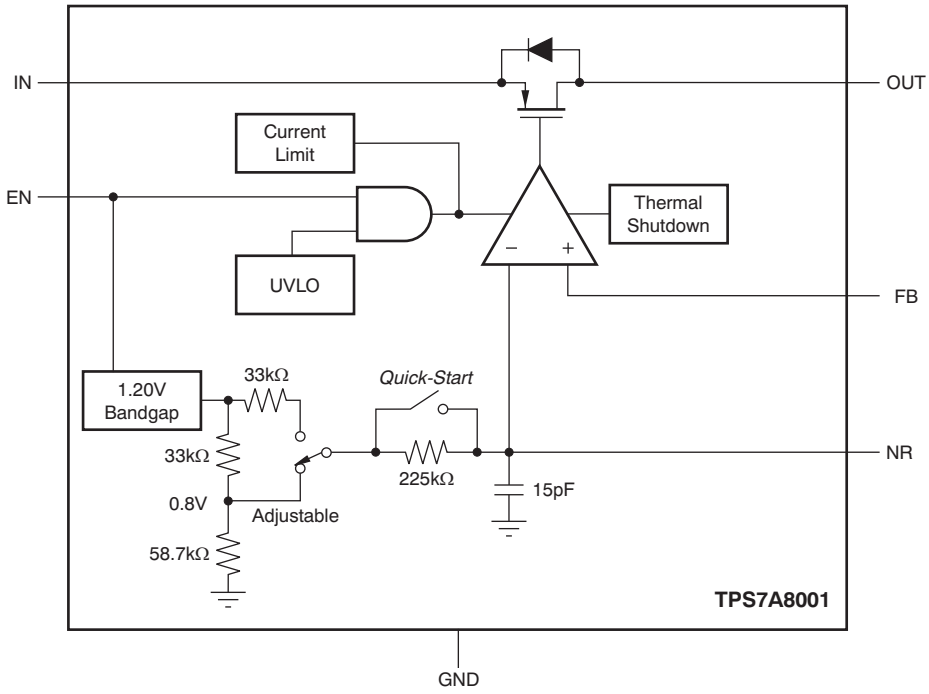


Figure 2. Adjustable Voltage Version

PIN CONFIGURATION

DRB PACKAGE
3mm x 3mm SON-8
(TOP VIEW)

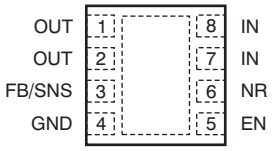


Table 1. PIN DESCRIPTIONS

NAME	PIN NO.	DESCRIPTION
IN	7, 8	Unregulated input supply.
GND	4, pad	Ground.
EN	5	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. Refer to *Shutdown* in the *Application Information* section for more details. EN must not be left floating and can be connected to IN if not used.
NR	6	Connect an external capacitor between this pin and ground to reduce output noise to very low levels. Also, the capacitor slows down the V_{OUT} ramp (RC softstart).
FB	3	***Adjustable voltage version only***. This pin is the input to the control loop error amplifier and is used to set the output voltage of the device.
SNS	3	***Fixed voltage versions only***. This pin is the input to the control loop error amplifier and is used to set the output voltage of the device. This pin is to be shorted to OUT at load devices.
OUT	1, 2	Regulator output. A 4.7µF or larger capacitor of any type is required for stability.

TYPICAL CHARACTERISTICS: TPS7A8001

At $V_{OUT(TYP)}$ = 3.3V, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V (whichever is greater), I_{OUT} = 100mA, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{OUT} = 4.7µF, and C_{NR} = 0.01µF, all temperature values refer to T_J, unless otherwise noted.

LOAD REGULATION

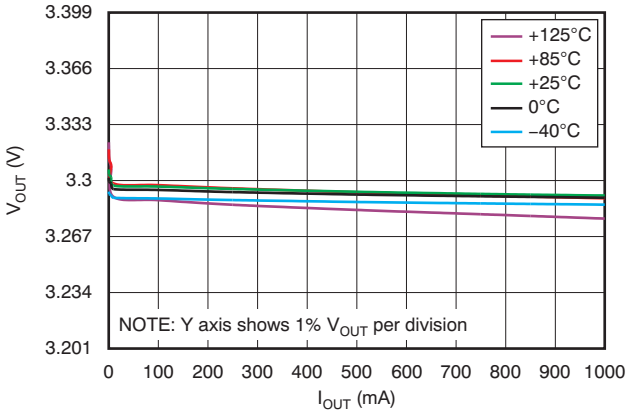


Figure 3.

LOAD REGULATION UNDER LIGHT LOADS

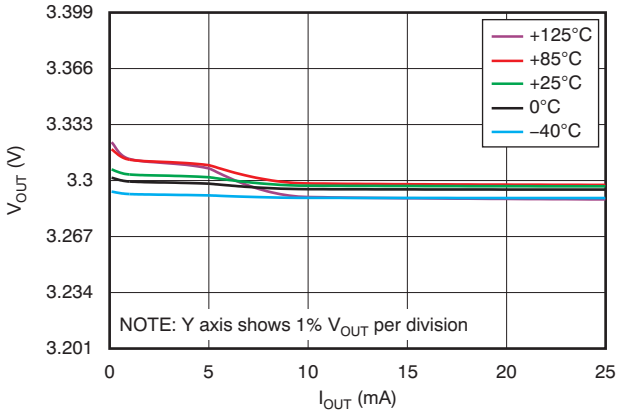


Figure 4.

LINE REGULATION

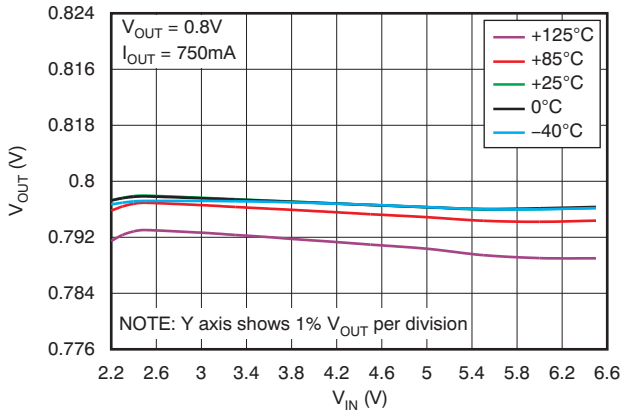


Figure 5.

LINE REGULATION UNDER LIGHT LOADS

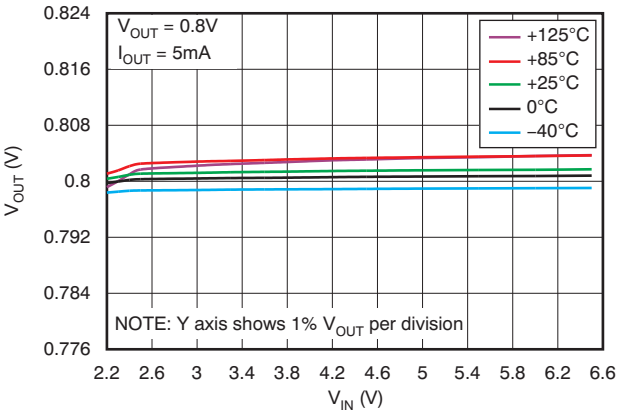


Figure 6.

TYPICAL CHARACTERISTICS: TPS7A8001 (continued)

At $V_{OUT(TYP)}$ = 3.3V, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V (whichever is greater), I_{OUT} = 100mA, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{OUT} = 4.7µF, and C_{NR} = 0.01µF, all temperature values refer to T_J, unless otherwise noted.

DROPOUT VOLTAGE vs INPUT VOLTAGE

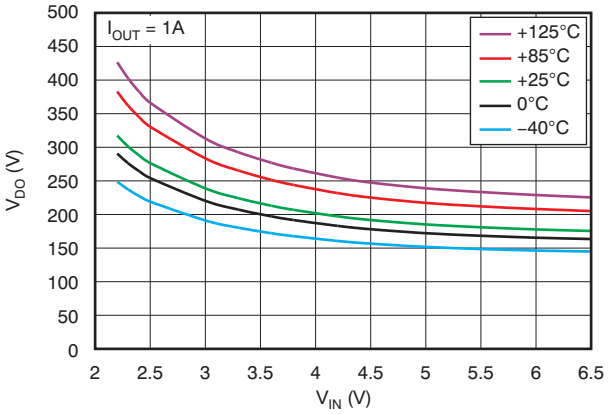


Figure 7.

DROPOUT VOLTAGE vs INPUT VOLTAGE

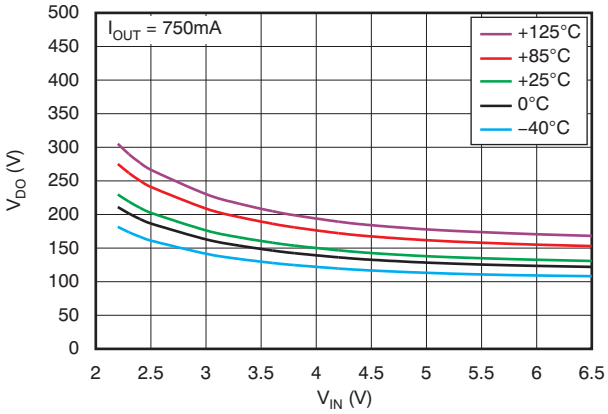


Figure 8.

DROPOUT VOLTAGE vs INPUT VOLTAGE

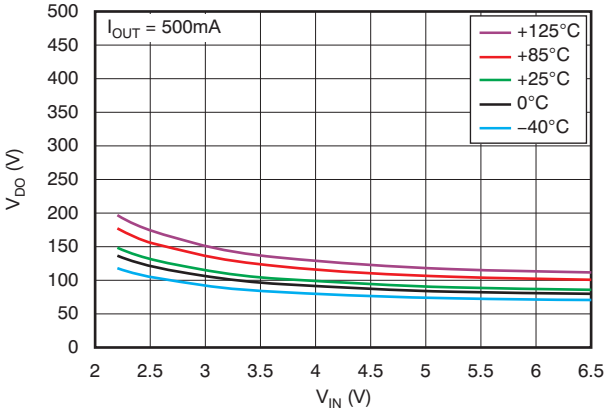


Figure 9.

DROPOUT VOLTAGE vs LOAD CURRENT

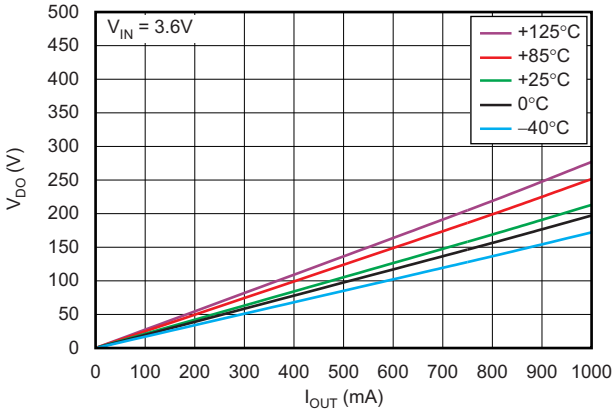


Figure 10.

DROPOUT VOLTAGE vs TEMPERATURE

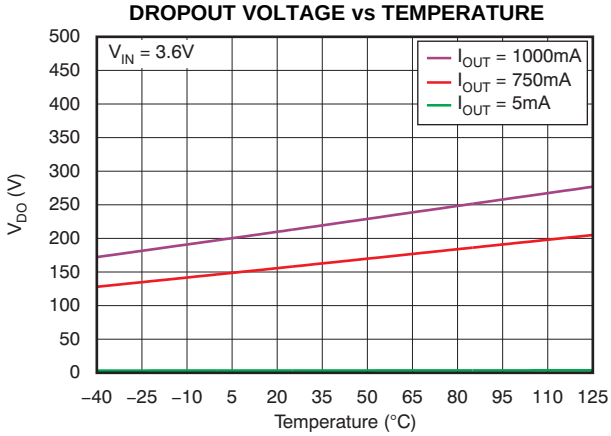


Figure 11.

TYPICAL CHARACTERISTICS: TPS7A8001 (continued)

At $V_{OUT(TYP)}$ = 3.3V, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V (whichever is greater), I_{OUT} = 100mA, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{OUT} = 4.7µF, and C_{NR} = 0.01µF, all temperature values refer to T_J, unless otherwise noted.

GROUND PIN CURRENT vs INPUT VOLTAGE

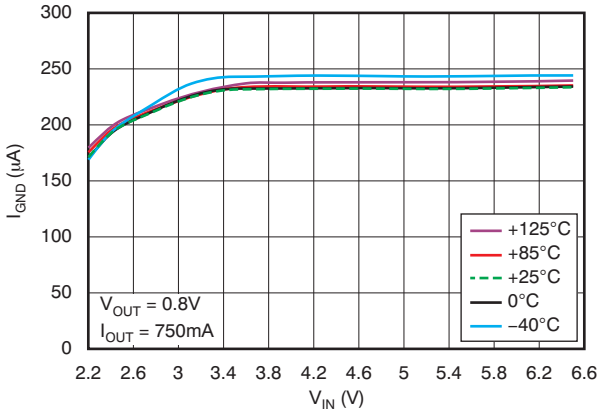


Figure 12.

GROUND PIN CURRENT vs LOAD CURRENT

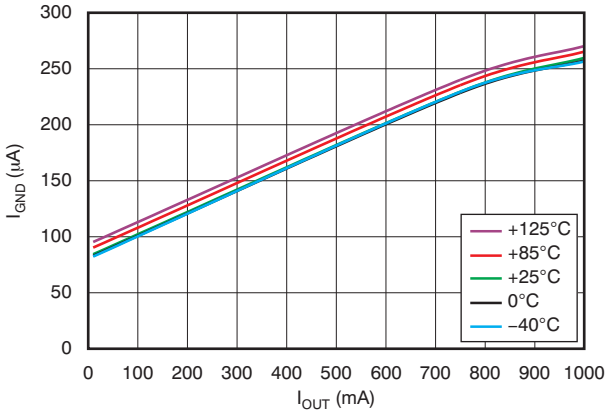


Figure 13.

SHUTDOWN CURRENT vs TEMPERATURE

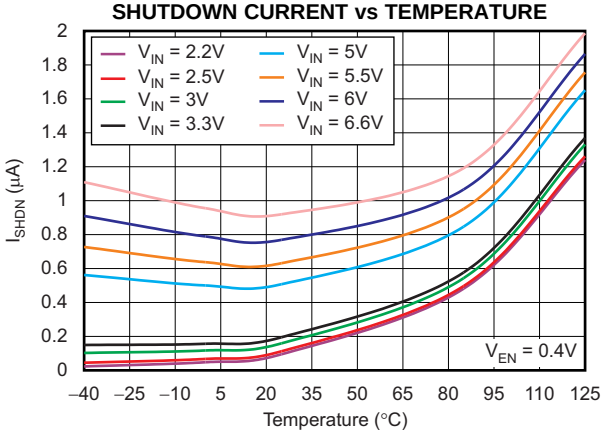


Figure 14.

CURRENT LIMIT vs TEMPERATURE

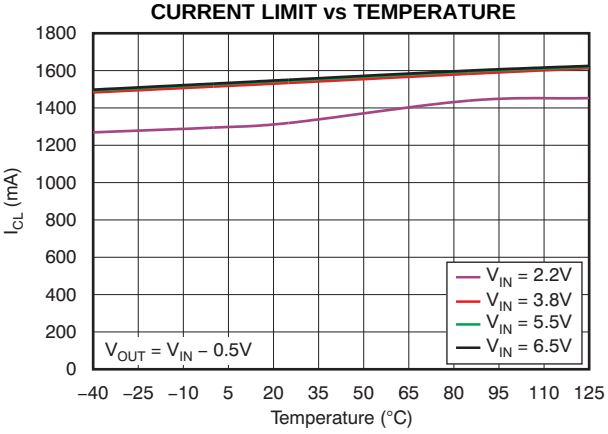


Figure 15.

TYPICAL CHARACTERISTICS: TPS7A8001 (continued)

At $V_{OUT(TYP)}$ = 3.3V, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V (whichever is greater), I_{OUT} = 100mA, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{OUT} = 4.7µF, and C_{NR} = 0.01µF, all temperature values refer to T_J, unless otherwise noted.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY

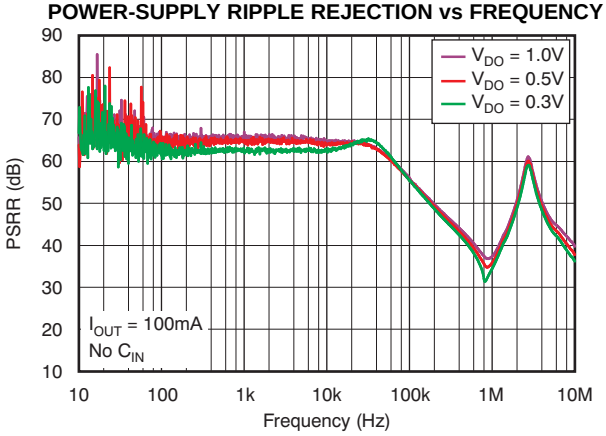


Figure 16.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY

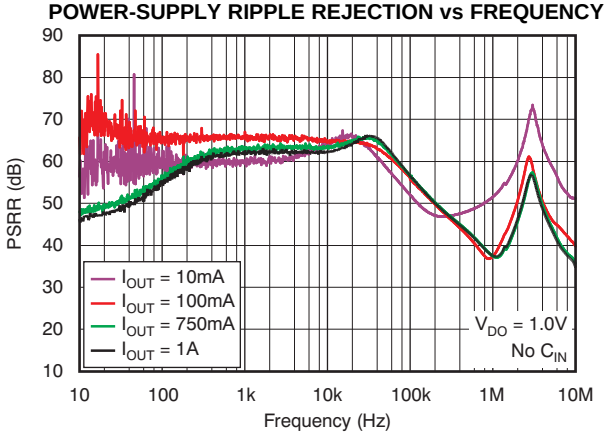


Figure 17.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY

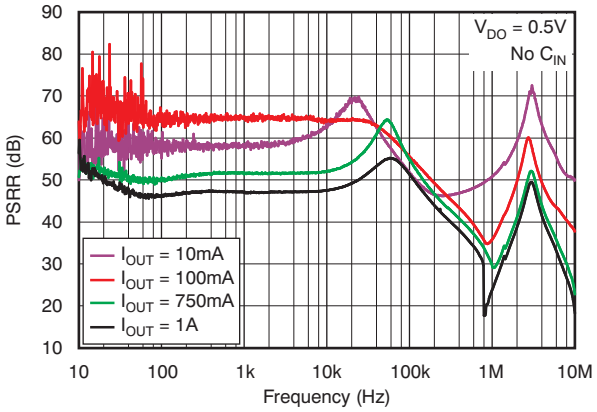


Figure 18.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY

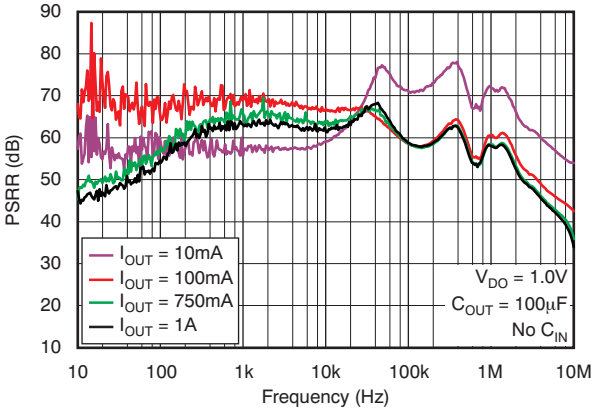


Figure 19.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY

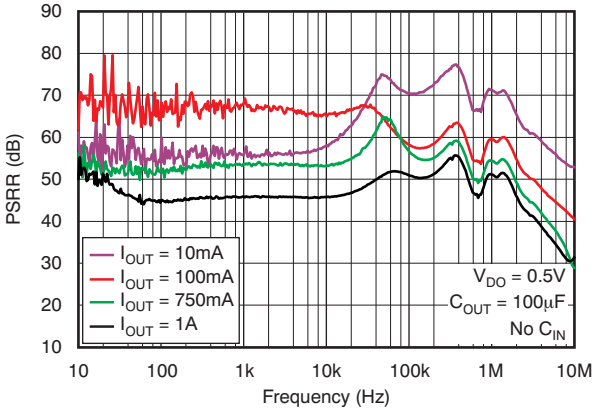


Figure 20.

TYPICAL CHARACTERISTICS: TPS7A8001 (continued)

At $V_{OUT(TYP)}$ = 3.3V, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V (whichever is greater), I_{OUT} = 100mA, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{OUT} = 4.7µF, and C_{NR} = 0.01µF, all temperature values refer to T_J, unless otherwise noted.

POWER-SUPPLY RIPPLE REJECTION vs DROPOUT VOLTAGE

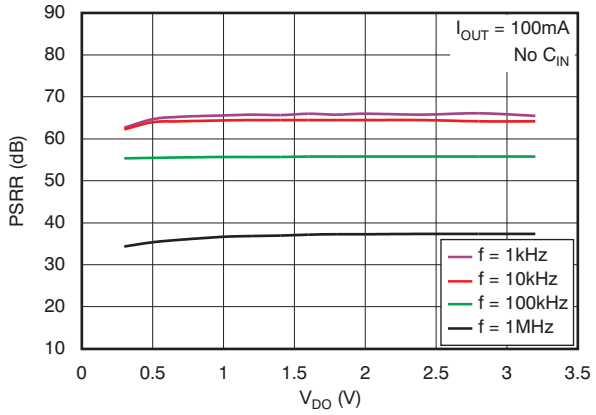


Figure 21.

POWER-SUPPLY RIPPLE REJECTION vs DROPOUT VOLTAGE

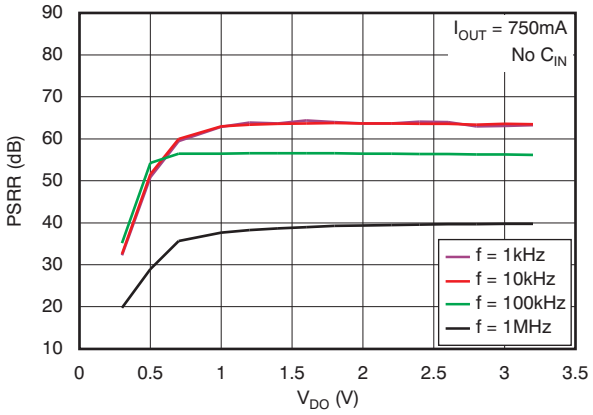


Figure 22.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

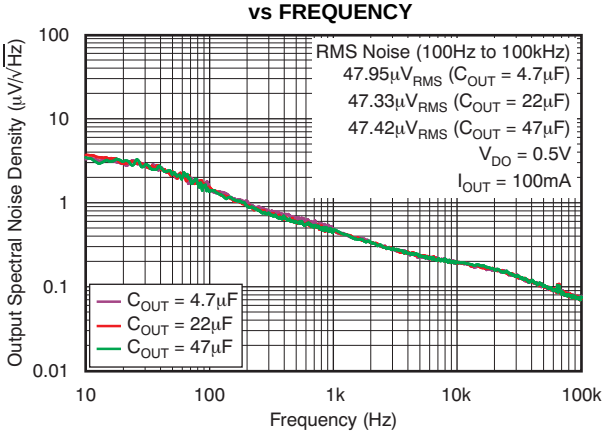


Figure 23.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

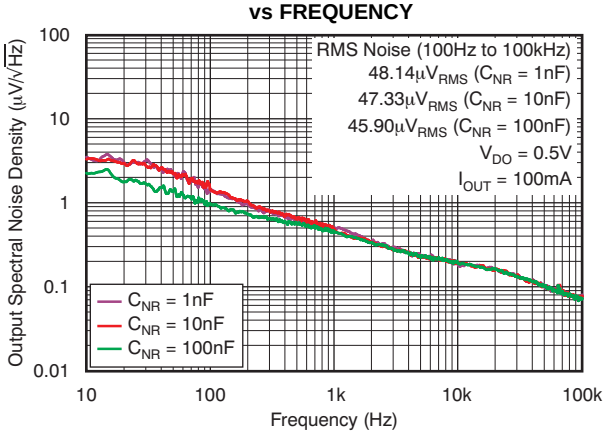


Figure 24.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

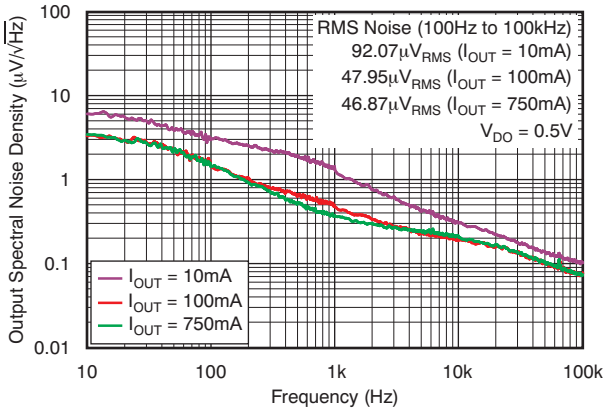


Figure 25.

TYPICAL CHARACTERISTICS: TPS7A8001 (continued)

At $V_{OUT(TYP)}$ = 3.3V, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.2V (whichever is greater), I_{OUT} = 100mA, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{OUT} = 4.7µF, and C_{NR} = 0.01µF, all temperature values refer to T_J, unless otherwise noted.

STARTUP TIME vs NOISE REDUCTION CAPACITANCE

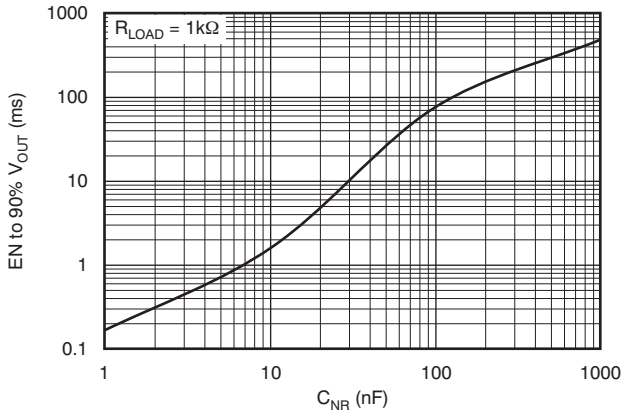


Figure 26.

LINE TRANSIENT RESPONSE

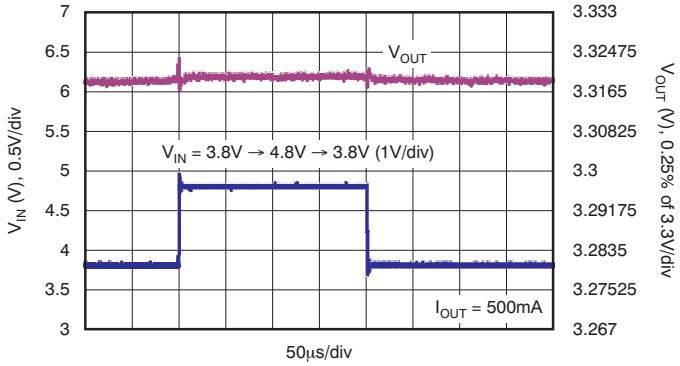


Figure 27.

LOAD TRANSIENT RESPONSE

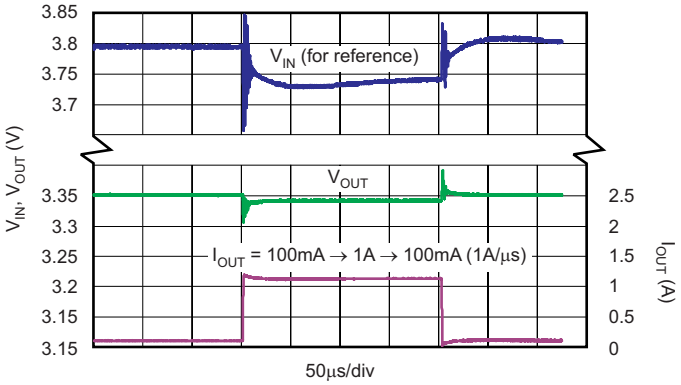


Figure 28.

ENABLE PULSE RESPONSE

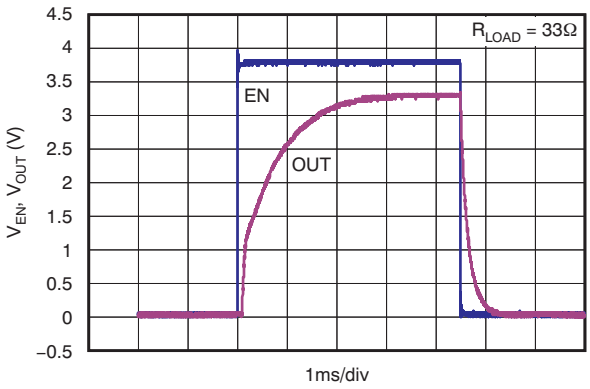


Figure 29.

POWER-UP/POWER-DOWN RESPONSE(1)

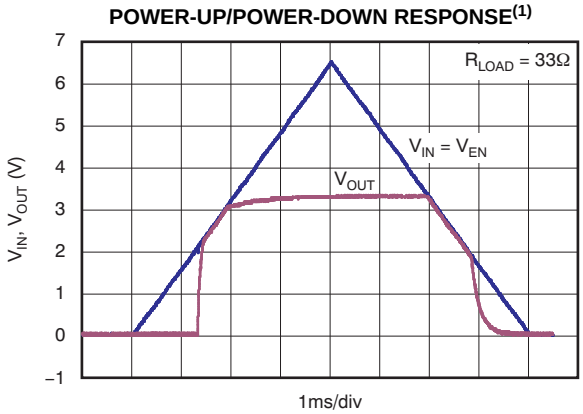


Figure 30.

(1) The internal reference requires approximately 2ms of rampup time (see Startup); therefore, V_{OUT} fully reaches the target output voltage of 3.3V in 2ms from starup.

APPLICATION INFORMATION

The TPS7A80xx belongs to a family of new generation LDO regulators that use innovative circuitry to achieve wide bandwidth and high loop gain, resulting in extremely high PSRR (over a 1MHz range) at very low headroom (V_{IN} – V_{OUT}). A noise reduction capacitor (C_{NR}) at the NR pin bypasses noise generated by the bandgap reference in order to improve PSRR, while a quick-start circuit fast-charges this capacitor. This family of regulators offers sub-bandgap output voltages, current limit, and thermal protection, and is fully specified from –40°C to +125°C.

Figure 31 shows the basic circuit connections for the fixed voltage options. Figure 32 gives the connections for the adjustable output version (TPS7A8001).

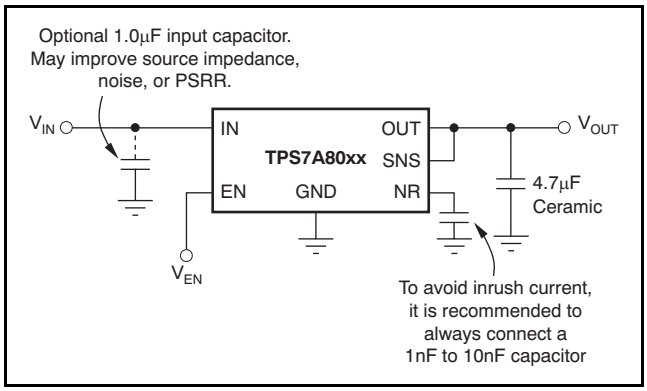


Figure 31. Typical Application Circuit (Fixed Voltage Versions)

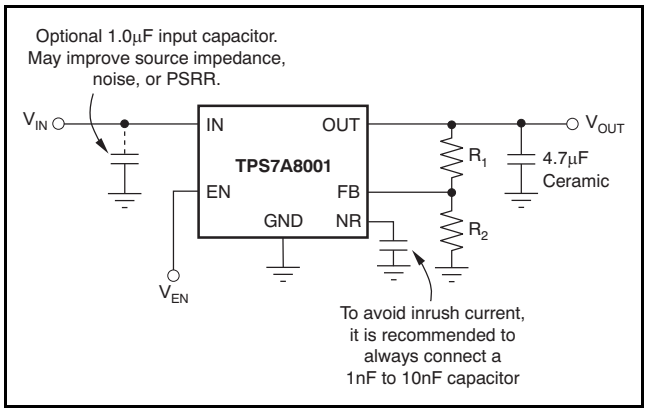


Figure 32. Typical Application Circuit (Adjustable Voltage Version)

For the adjustable version (TPS7A8001), the voltage on the FB pin sets the output voltage and is determined by the values of R_1 and R_2. The values of R_1 and R_2 can be calculated for any voltage using the formula given in Equation 1:

$$V_{OUT} = \frac{(R_1 + R_2)}{R_2} \times 0.800 \quad (1)$$

Sample resistor values for common output voltages are shown in Table 2. In Table 2, E96 series resistors are used, and all values meet 1% of the target V_{OUT}, assuming resistors with zero error. For the actual design, pay attention to any resistor error factors. Using lower values for R_1 and R_2 reduces the noise injected from the FB pin.

Table 2. Sample 1% Resistor Values for Common Output Voltages

V_{OUT}	R_1	R_2
0.8V	0Ω (Short)	10.0kΩ
1.0V	2.49kΩ	10.0kΩ
1.2V	4.99kΩ	10.0kΩ
1.5V	8.87kΩ	10.0kΩ
1.8V	12.5kΩ	10.0kΩ
2.5V	21.0kΩ	10.0kΩ
3.3V	30.9kΩ	10.0kΩ
5.0V	52.3kΩ	10.0kΩ

Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1µF to 1.0µF low equivalent series resistance (ESR) capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or if the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1µF input capacitor may be necessary to ensure stability.

The TPS7A80xx is designed to be stable with standard ceramic capacitors of capacitance values 4.7µF or larger. This device is evaluated using a 4.7µF ceramic capacitor of 10V rating, 10% tolerance, X5R type, and 0805 size (2.0mm x 1.25mm).

X5R- and X7R-type capacitors are highly recommended because they have minimal variation in value and ESR over temperature. Maximum ESR should be <1.0Ω.

The TPS7A80xx implements an innovative internal compensation circuit that does not require a feedback capacitor across R_2 for stability. A feedback capacitor should not be used for this device.

Output Noise

In most LDOs, the bandgap is the dominant noise source. If a noise reduction capacitor (C_{NR}) is used with the TPS7A80xx, the bandgap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. To minimize noise in a given application, use a 0.01µF (minimum) noise-reduction capacitor.

Equation 2 approximates the total noise when C_{NR} = 0.01µF:

$$V_N = 12.6 \times V_{OUT} + 13.5 \ (\mu V_{RMS}) \quad (2)$$

Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

Internal Current Limit

The TPS7A80xx internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in a current limit state for extended periods of time.

The PMOS pass element in the TPS7A80xx has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting may be appropriate.

Shutdown

The enable pin (EN) is active high and is compatible with standard and low voltage, TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

Dropout Voltage

The TPS7A80xx uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device in dropout behaves the same way as a resistor.

As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in Figure 21 and Figure 22 in the *Typical Characteristics* section.

Startup

Through a lower resistance, the bandgap reference can quickly charge the noise reduction capacitor (C_{NR}). The TPS7A80xx has a *quick-start* circuit to quickly charge C_{NR}, if present; see the *Functional Block Diagrams*. At startup, this quick-start switch is closed, with only 33kΩ of resistance between the bandgap reference and the NR pin. The quick-start switch opens approximately 2ms after any device enabling event, and the resistance between the bandgap reference and the NR pin becomes higher in value (approximately 250kΩ) to form a very good low-pass (RC) filter. This low-pass filter achieves very good noise reduction for the reference voltage.

Inrush current can be a problem in many applications. The 33kΩ resistance during the startup period is intentionally put there to slow down the reference voltage ramp up, thus reducing the inrush current. For example, the capacitance of connecting the recommended C_{NR} value of 0.01µF along with the 33kΩ resistance causes approximately 1ms RC delay. Startup time with the other C_{NR} values can be calculated as:

$$t_{STR} \ (s) = 76{,}000 \times C_{NR} \ (F) \quad (3)$$

Note that Equation 3 is valid up to t_{STR} = 2ms or C_{NR} = 26nF, whichever is smaller.

Although the noise reduction effect is nearly saturated at 0.01µF, connecting a C_{NR} value greater than 0.01µF can help reduce noise slightly more; however, startup time will be extremely long because the quick-start switch opens after approximately 2ms. That is, if C_{NR} is not fully charged during this 2ms period, C_{NR} finishes charging through a higher resistance of 250kΩ, and takes much longer to fully charge.

Note that a low leakage C_{NR} should be used; most ceramic capacitors are suitable.

Transient Response

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

Undervoltage Lock-Out (UVLO)

The TPS7A80xx utilizes an undervoltage lock-out circuit to keep the output shut off until the internal circuitry is operating properly. The UVLO circuit has a de-glitch feature so that it typically ignores undershoot transients on the input if they are less than 50µs duration.

Minimum Load

The TPS7A80xx is stable and well-behaved with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TPS7A80xx employs an innovative low-current mode circuit to increase loop gain under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current.

THERMAL INFORMATION

Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage because of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A80xx has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS7A80xx into thermal shutdown degrades device reliability.

Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation.

Power dissipation of the device depends on input voltage and load conditions and can be calculated using Equation 4:

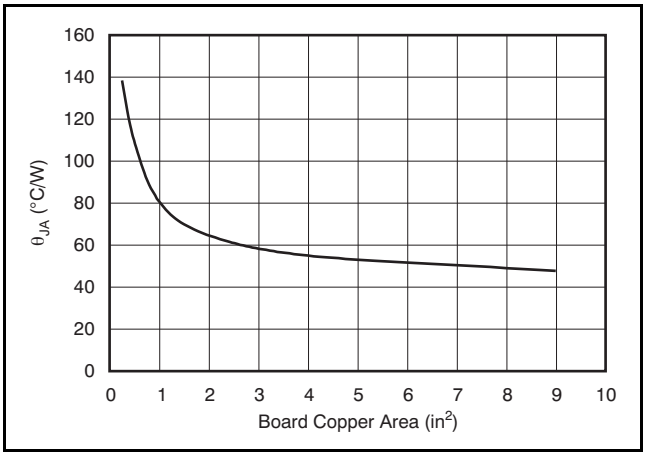
$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

On the SON (DRB) package, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or be left floating; however, it should be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using Equation 5:

$$R_{\theta JA} = \frac{(+125^{o}C - T_A)}{P_D} \quad (5)$$

Knowing the maximum $R_{\theta JA}$, the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using Figure 33.



Note: θ_{JA} value at board size of 9in^2 (that is, 3in × 3in) is a JEDEC standard.

Figure 33. θ_{JA} vs Board Size

Figure 33 shows the variation of θ_{JA} as a function of ground plane copper area in the board. It is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and should not be used to estimate actual thermal performance in real application environments.

NOTE: When the device is mounted on an application PCB, it is strongly recommended to use Ψ_{JT} and Ψ_{JB}, as explained in the *Estimating Junction Temperature* section.

ESTIMATING JUNCTION TEMPERATURE

Using the thermal metrics Ψ_{JT} and Ψ_{JB}, as shown in the *Thermal Information* table, the junction temperature can be estimated with corresponding formulas (given in Equation 6). For backwards compatibility, an older $\theta_{JC,Top}$ parameter is listed as well.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$

$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \tag{6}$$

Where P_D is the power dissipation shown by Equation 5, T_T is the temperature at the center-top of the IC package, and T_B is the PCB temperature measured 1mm away from the IC package *on the PCB surface* (as Figure 35 shows).

NOTE: Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the application note SBVA025, *Using New Thermal Metrics*, available for download at www.ti.com.

By looking at Figure 34, the new thermal metrics (Ψ_{JT} and Ψ_{JB}) have very little dependency on board size. That is, using Ψ_{JT} or Ψ_{JB} with Equation 6 is a good way to estimate T_J by simply measuring T_T or T_B, regardless of the application board size.

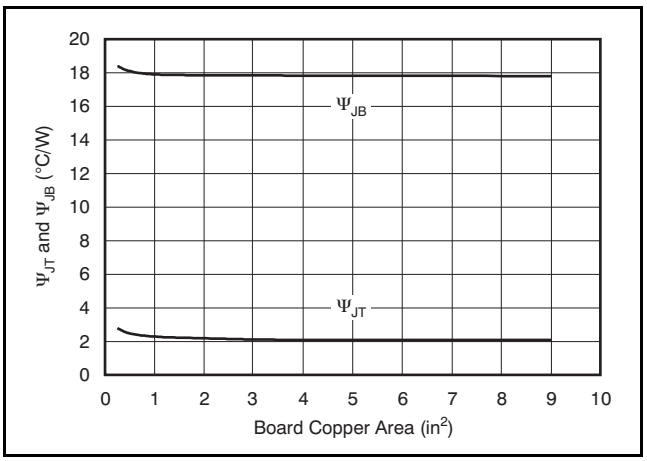


Figure 34. Ψ_{JT} and Ψ_{JB} vs Board Size

For a more detailed discussion of why TI does not recommend using $\theta_{JC(top)}$ to determine thermal characteristics, refer to application report SBVA025, *Using New Thermal Metrics*, available for download at www.ti.com. For further information, refer to application report SPRA953, *IC Package Thermal Metrics*, also available on the TI website.

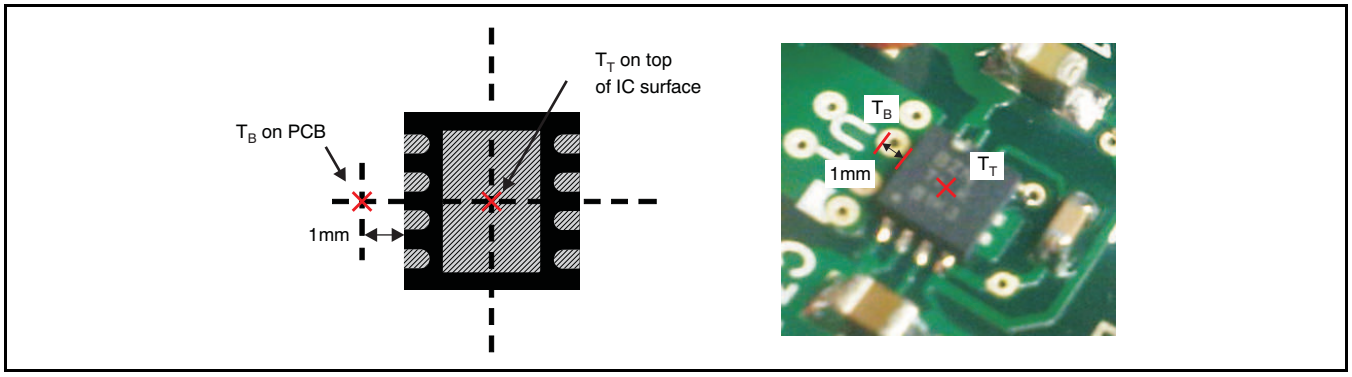


Figure 35. Measuring Points for T_T and T_B

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (April 2012) to Revision H **Page**

- Updated Figure 10 8

Changes from Revision F (March 2012) to Revision G **Page**

- Changed Thermal Information table values, added new footnote 2, changed footnote 3 3

Changes from Revision E (February 2012) to Revision F **Page**

- Changed *Low Noise* Features bullet 1
- Updated Equation 2 14

Changes from Revision D (December 2010) to Revision E **Page**

- Changed *Low Noise* Features bullet 1
- Changed caption of front-page application circuit 1
- Updated Figure 14 9
- Updated Figure 28 12
- Updated Equation 2 14
- Added Equation 3 note in *Startup* section 14

Changes from Revision C (September, 2010) to Revision D **Page**

- Updated front-page figure with new characteristic graph 1
- Revised Figure 19 10
- Changed Figure 20 10

Changes from Revision B (August, 2010) to Revision C **Page**

- Changed data sheet title 1
- Changed *ultra-high PSRR* to *wide-bandwidth lhgh PSRR* in *Features* list 1
- Corrected typos in Figure 23 through Figure 25 11
- Revised first paragraph of *Application Information* to remove phrase *ultra-wide bandwidth* 13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS7A8001DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OFU	Samples
TPS7A8001DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OFU	Samples
TPS7A8101DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SAU	Samples
TPS7A8101DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SAU	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

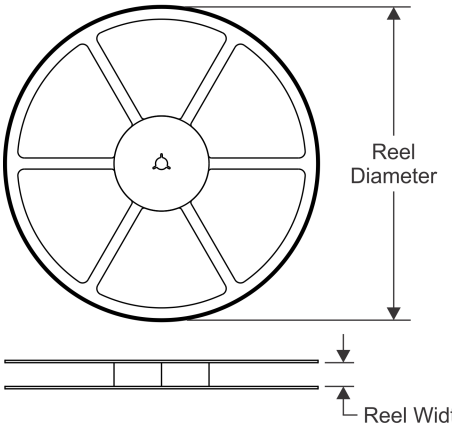
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

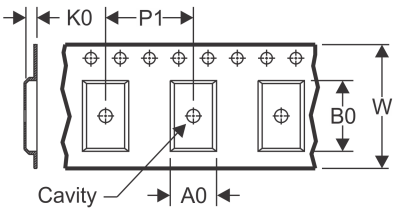
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

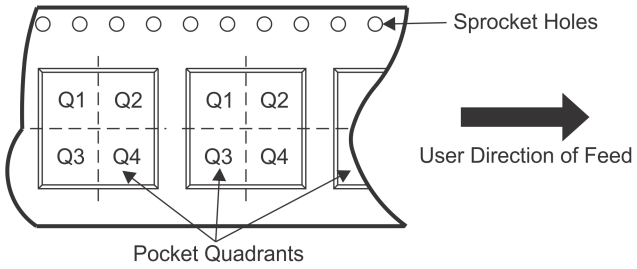


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

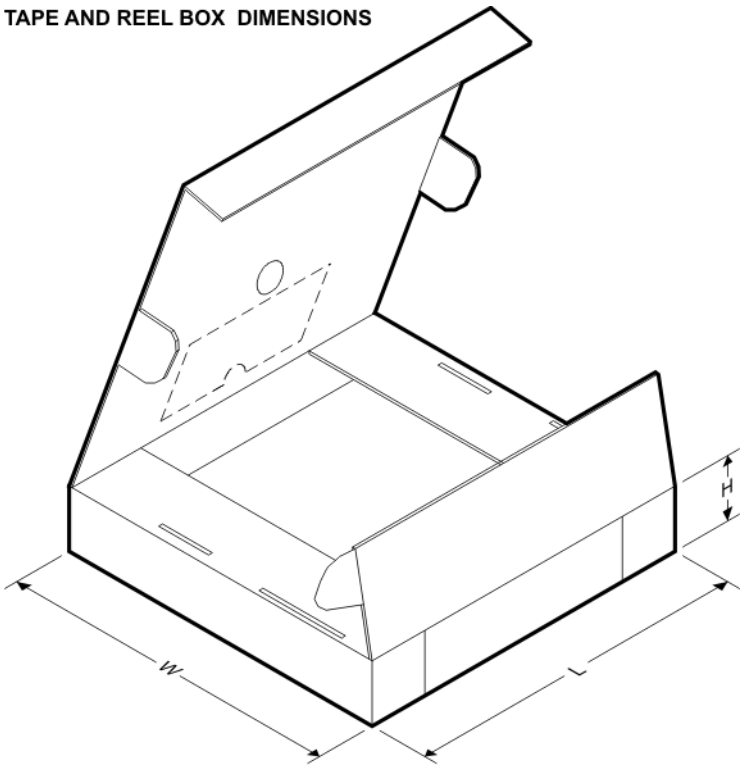
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A8001DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS7A8001DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS7A8001DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS7A8001DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS7A8101DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS7A8101DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

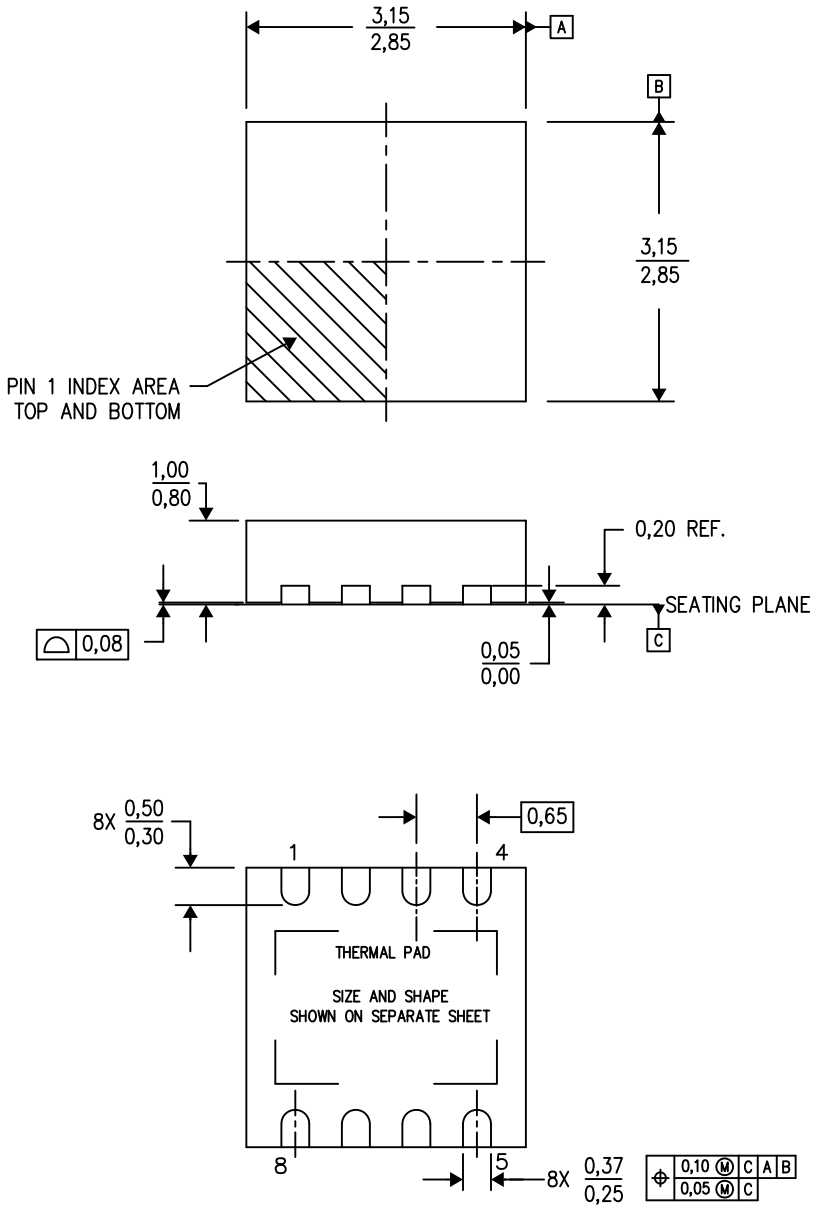
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A8001DRBR	SON	DRB	8	3000	552.0	367.0	36.0
TPS7A8001DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS7A8001DRBT	SON	DRB	8	250	210.0	185.0	35.0
TPS7A8001DRBT	SON	DRB	8	250	552.0	185.0	36.0
TPS7A8101DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS7A8101DRBT	SON	DRB	8	250	210.0	185.0	35.0

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



4203482–2/K 06/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

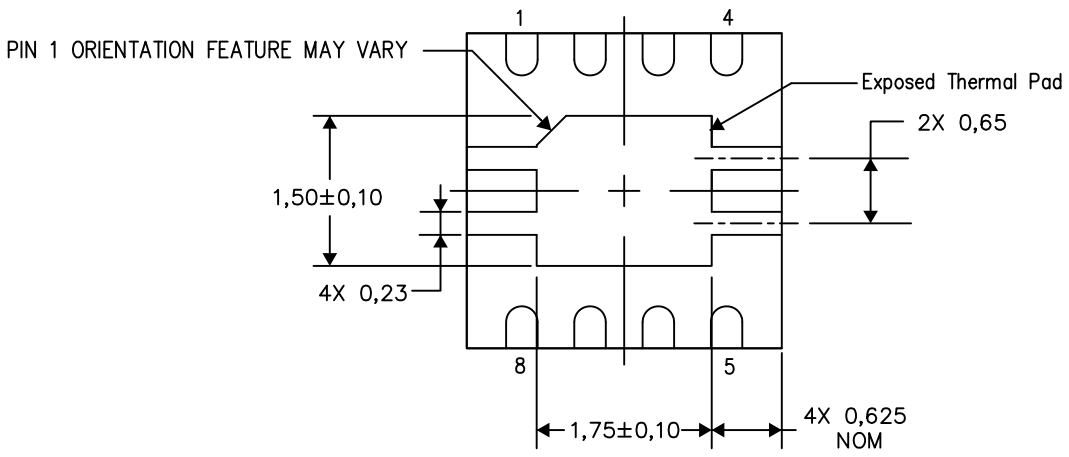
DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



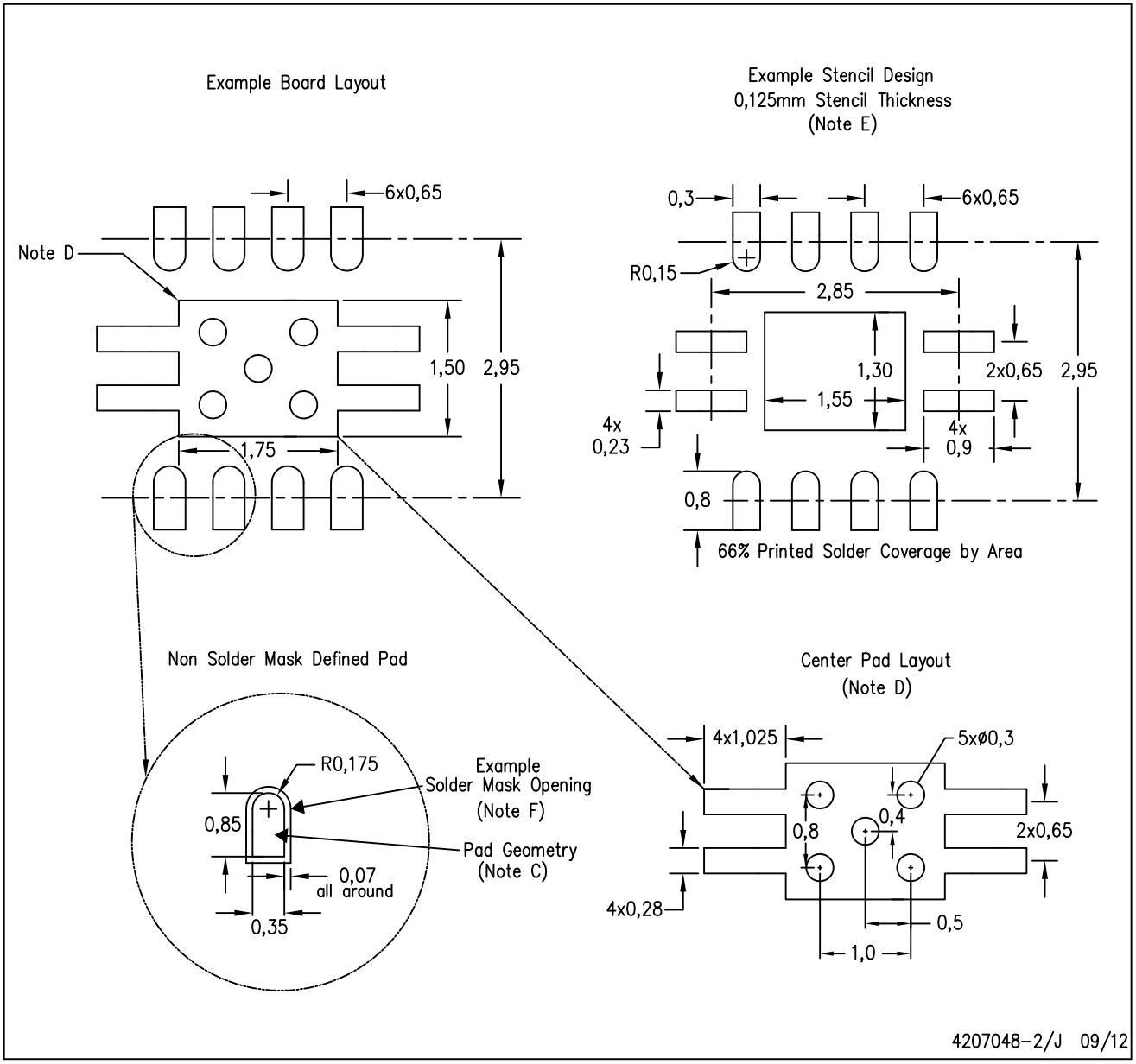
Bottom View

Exposed Thermal Pad Dimensions

4206340–2/N 09/12

NOTE: All linear dimensions are in millimeters

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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