400mA Low-Dropout Regulator for C2000™

Check for Samples: TPS73619

FEATURES

- **Optimal Output Voltage for Core Rail of C2000**
- **Good Line/Load Transient Response for MCUs**
- **400mA LDO Voltage Regulator with Enable**
- **Very Low Dropout Voltage: 75mV (typ) at 400mA**
- **Reverse Current Protection**
- **Stable with or without Output Capacitor**
- **1% Overall Accuracy Over Line, Load, and Temperature**
- **Available in 8-Pin SON-8 Package**

APPLICATIONS

- **C2000 Core Power Rail Supply**

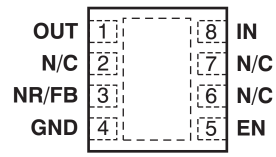
DESCRIPTION

The TPS73619 is a low-dropout (LDO) voltage regulator that offers very good line and load transient response, even without the use of an output capacitor. The TPS73619 is suitable for driving the C2000 MCUs from Texas Instruments. These devices offer very low voltage, thereby reducing power loss.

In combination with a voltage supervisor such as the TPS3808G19 or TPS3808G01, the TPS73619 can deliver tight V_{CORE} voltage and generate accurate power-good signals that meet or exceed power requirements for the C2000.

The TPS73619 is available in an 8-pin SON-8 package.

DRB PACKAGE
3mm x 3mm SON
(TOP VIEW)



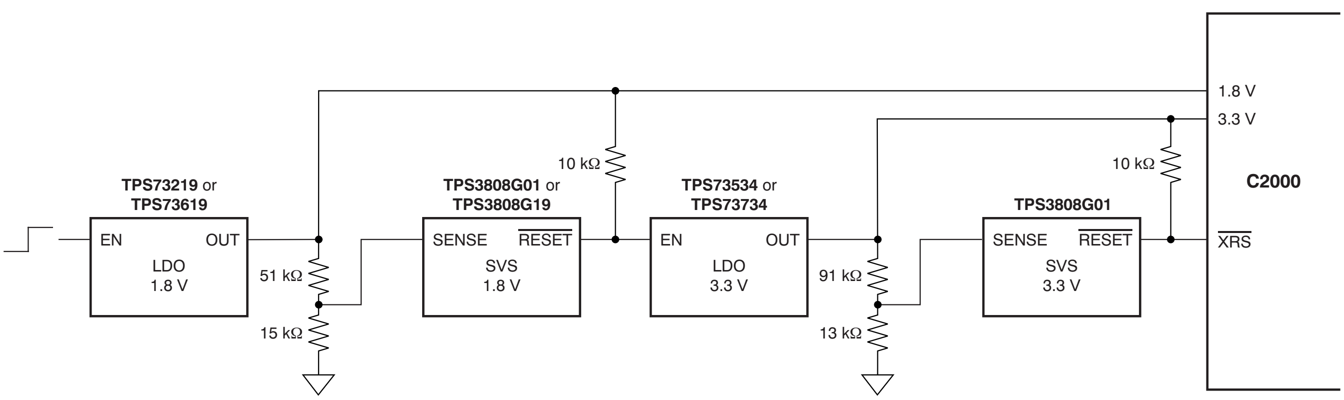


Figure 1. Typical Application

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT} (2)
TPS736**xx *yy yz***	**XX** is nominal output voltage (for example, 25 = 2.5V, 01 = Adjustable(3)). **YYY** is package designator. **Z** is package quantity.

(1) For the most current specification and package information, refer to the Package Option Addendum located at the end of this datasheet or see the TI website at www.ti.com.
(2) Most output voltages of 1.25V and 1.3V to 5.0V in 100mV increments are available on a quick-turn basis using innovative factory EEPROM programming. Minimum order quantities apply; contact factory for details and availability.
(3) For fixed 1.20V operation, tie FB to OUT.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

PARAMETER	TPS73619	UNIT
V_{IN} range	–0.3 to 6.0	V
V_{EN} range	–0.3 to 6.0	V
V_{OUT} range	–0.3 to 5.5	V
V_{NR}, V_{FB} range	–0.3 to 6.0	V
Peak output current	Internally limited	
Output short-circuit duration	Indefinite	
Continuous total power dissipation	See *Thermal Information* Table	
Junction temperature range, T_J	–55 to +150	°C
Storage temperature range	–65 to +150	°C
ESD rating, HBM	2	kV
ESD rating, CDM	500	V

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the Electrical Characteristics is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC[1][2]		TPS73619[3] DRB 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance[4]	47.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[5]	83	
θ_{JB}	Junction-to-board thermal resistance[6]	N/A	
ψ_{JT}	Junction-to-top characterization parameter[7]	2.1	
ψ_{JB}	Junction-to-board characterization parameter[8]	17.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[9]	12.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953A.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.
(3) Thermal data for the DRB, DCQ, and DRV packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
  (a) The exposed pad is connected to the PCB ground layer through a 2x2 thermal via array.
  (b) The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
  (c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3in × 3in copper area. To understand the effects of the copper area on thermal performance, see the *Power Dissipation* section of this data sheet.
(4) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(5) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the top of the package. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(6) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(7) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(8) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(9) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = 24V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1μF, unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range			2.1		5.5	V
V_{OUT}	Accuracy	Nominal	T_J = +25°C	–0.5		+0.5	%
		over V_{IN}, I_{OUT}, and T	V_{OUT} + 0.5V ≤ V_{IN} ≤ 5.5V; 10mA ≤ I_{OUT} ≤ 400mA	–1.0	±0.5	+1.0	
$\Delta V_{OUT}\%/\Delta V_{IN}$	Line regulation		$V_{O(nom)}$ + 0.5V ≤ V_{IN} ≤ 5.5V		0.01		%/V
$\Delta V_{OUT}\%/\Delta I_{OUT}$	Load regulation		1mA ≤ I_{OUT} ≤ 400mA		0.002		%/mA
			10mA ≤ I_{OUT} ≤ 400mA		0.0005		
V_{DO}	Dropout voltage (V_{IN} = $V_{OUT(nom)}$ – 0.1V)		I_{OUT} = 400mA		75	200	mV
Z_O(DO)	Output impedance in dropout		1.7V ≤ V_{IN} ≤ V_{OUT} + V_{DO}		0.25		Ω
I_{CL}	Output current limit		V_{OUT} = 0.9 × $V_{OUT(nom)}$	400	650	800	mA
			3.6V ≤ V_{IN} ≤ 4.2V, 0°C ≤ T_J ≤ +70°C	500		800	mA
I_{SC}	Short-circuit current		V_{OUT} = 0V		450		mA
I_{REV}	Reverse leakage current[(1)] (–I_{IN})		V_{EN} ≤ 0.5V, 0V ≤ V_{IN} ≤ V_{OUT}		0.1	10	μA
I_{GND}	GND pin current		I_{OUT} = 10mA (I_Q)		400	550	μA
			I_{OUT} = 400mA		800	1000	
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.5V, V_{OUT} ≤ V_{IN} ≤ 5.5, –40°C ≤ T_J ≤ +100°C		0.02	1	μA
PSRR	Power-supply rejection ratio (ripple rejection)		f = 100Hz, I_{OUT} = 400mA		58		dB
			f = 10KHz, I_{OUT} = 400mA		37		
V_N	Output noise voltage BW = 10Hz – 100KHz		C_{OUT} = 10μF, No C_{NR}		27 × V_{OUT}		μV_{RMS}
			C_{OUT} = 10μF, C_{NR} = 0.01μF		8.5 × V_{OUT}		
t_{STR}	Startup time		V_{OUT} = 3V, R_L = 30Ω C_{OUT} = 1μF, C_{NR} = 0.01μF		600		μs
V_{EN}(HI)	EN pin high (enabled)			1.7		V_{IN}	V
V_{EN}(LO)	EN pin low (shutdown)			0		0.5	V
I_{EN}(HI)	EN pin current (enabled)		V_{EN} = 5.5V		0.02	0.1	μA
T_{SD}	Thermal shutdown temperature		Shutdown, temperature increasing		+160		°C
			Reset, temperature decreasing		+140		
T_J	Operating junction temperature			–40		+125	°C

(1) Fixed-voltage versions only; refer to Applications section for more information.

FUNCTIONAL BLOCK DIAGRAM

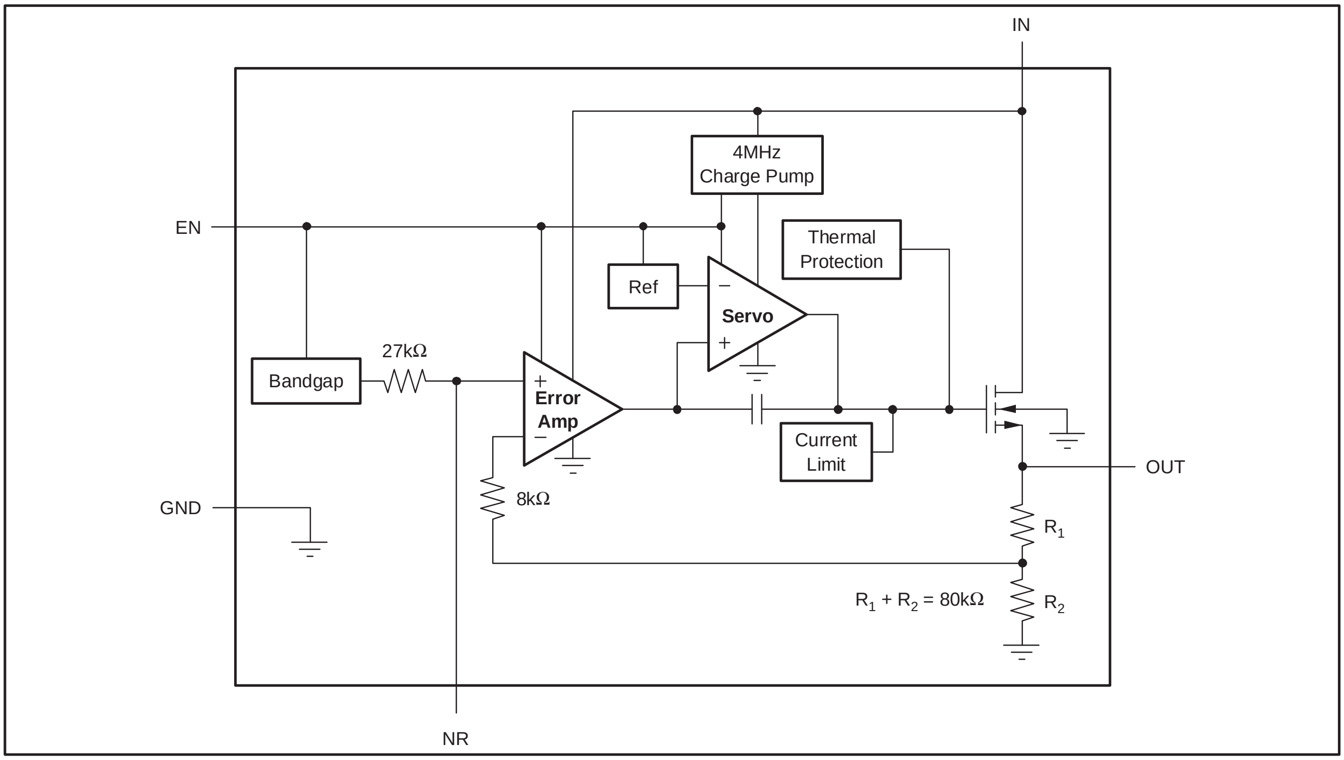
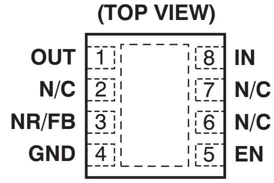


Figure 2. Fixed Voltage Version

PIN CONFIGURATION

DRB PACKAGE
3mm x 3mm SON
(TOP VIEW)



PIN DESCRIPTIONS

NAME	3x3 SON (DRB) PIN NO.	DESCRIPTION
IN	8	Input supply
GND	4, Pad	Ground
EN	5	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. Refer to the Shutdown section under Applications Information for more details. EN can be connected to IN if not used.
NR	3	Fixed voltage versions only—connecting an external capacitor to this pin bypasses noise generated by the internal bandgap, reducing output noise to very low levels.
FB	3	Adjustable voltage version only—this is the input to the control loop error amplifier, and is used to set the output voltage of the device.
OUT	1	Output of the Regulator. There are no output capacitor requirements for stability.

TYPICAL CHARACTERISTICS

For all voltage versions, at T_J = +25°C, V_{IN} = 24V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1μF, unless otherwise noted.

LOAD REGULATION

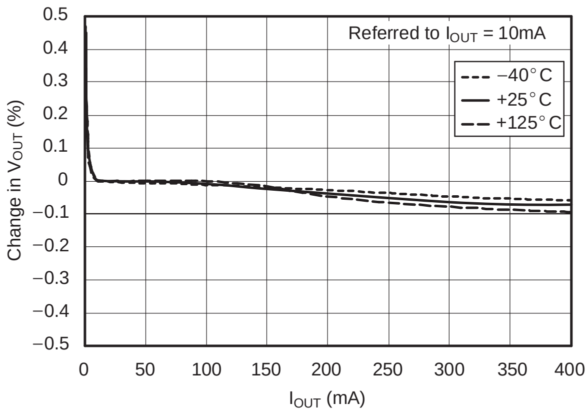


Figure 3.

LINE REGULATION

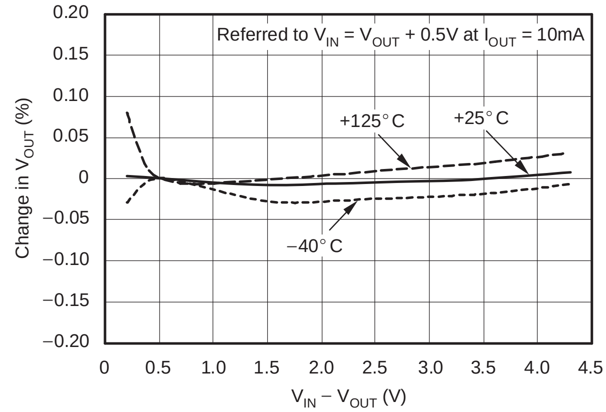


Figure 4.

DROPOUT VOLTAGE vs OUTPUT CURRENT

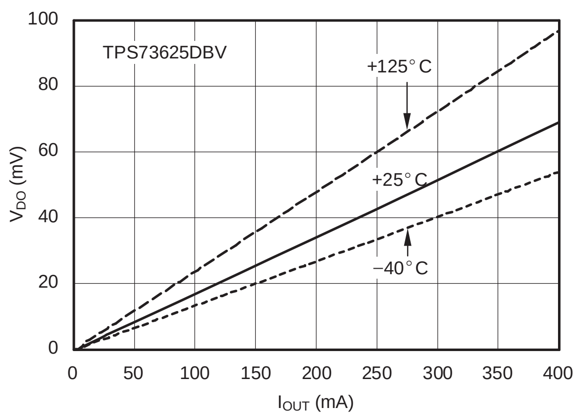


Figure 5.

DROPOUT VOLTAGE vs TEMPERATURE

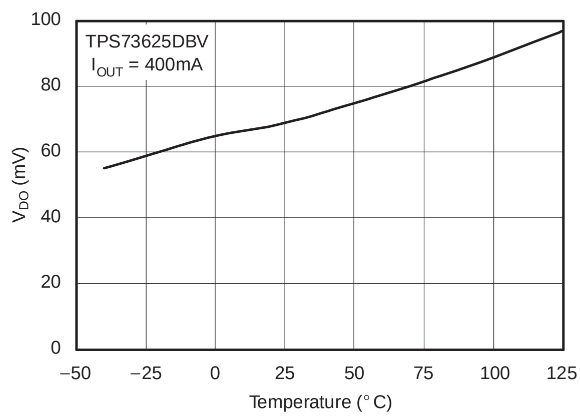


Figure 6.

OUTPUT VOLTAGE ACCURACY HISTOGRAM

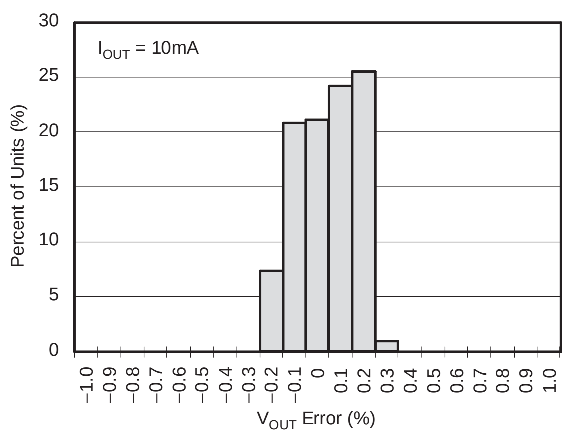


Figure 7.

OUTPUT VOLTAGE DRIFT HISTOGRAM

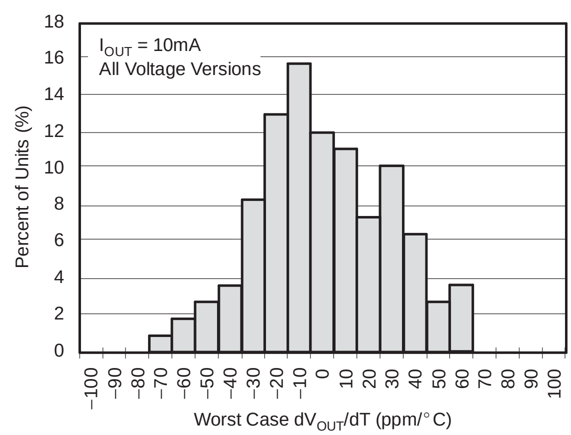


Figure 8.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions, at T_J = +25°C, V_{IN} = 24V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF, unless otherwise noted.

GROUND PIN CURRENT vs OUTPUT CURRENT

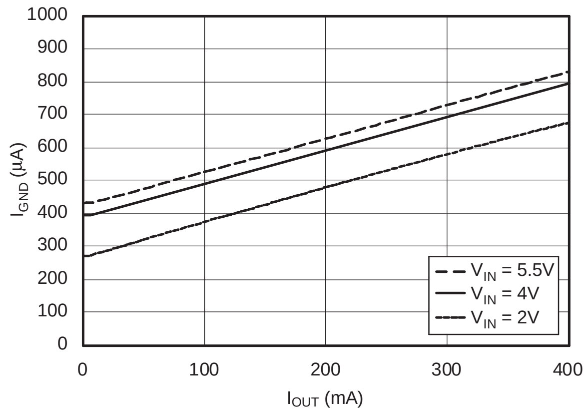


Figure 9.

GROUND PIN CURRENT vs TEMPERATURE

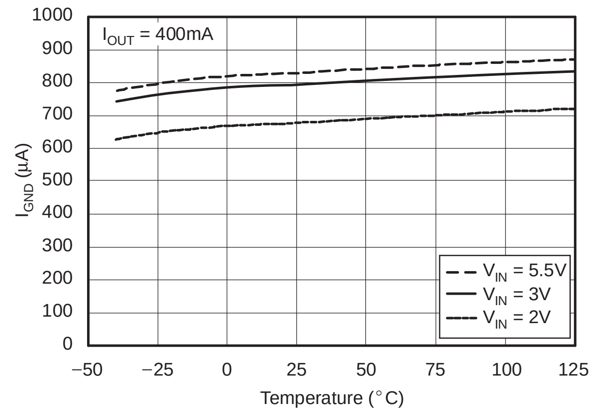


Figure 10.

GROUND PIN CURRENT in SHUTDOWN vs TEMPERATURE

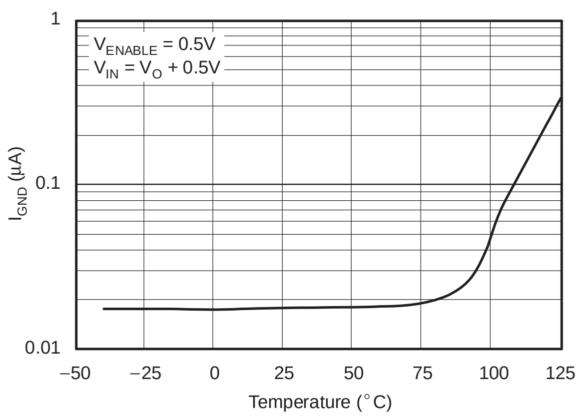


Figure 11.

CURRENT LIMIT vs V_{OUT} (FOLDBACK)

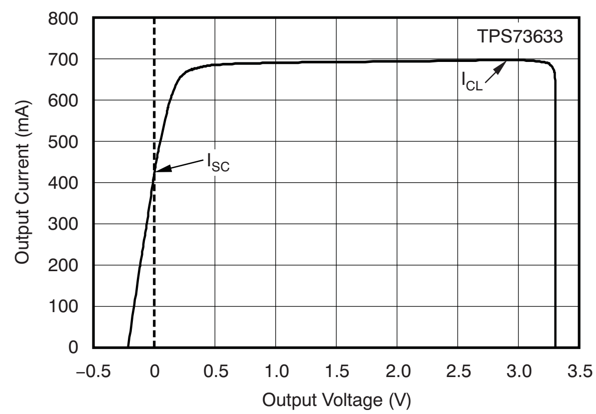


Figure 12.

CURRENT LIMIT vs V_{IN}

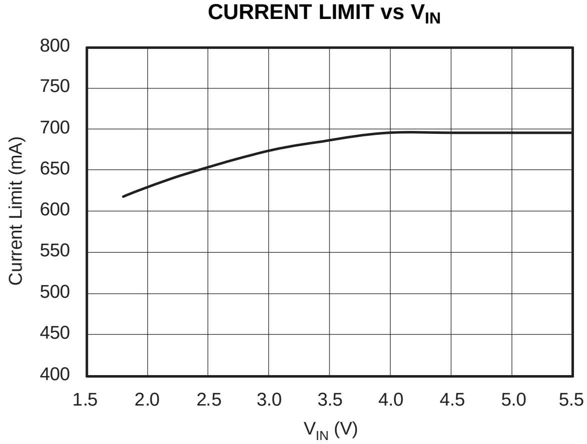


Figure 13.

CURRENT LIMIT vs TEMPERATURE

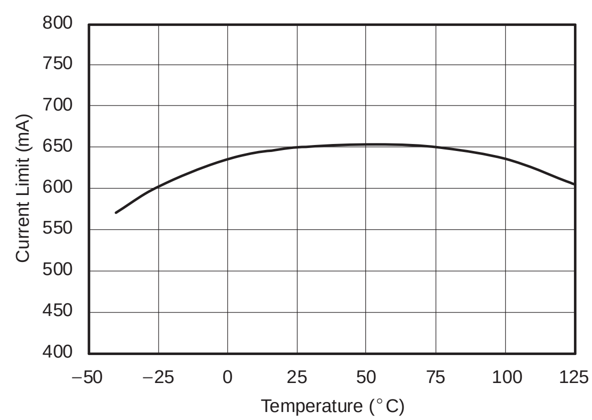


Figure 14.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions, at $T_J = +25°C$, $V_{IN} = 24V$, $I_{OUT} = 10mA$, $V_{EN} = 1.7V$, and $C_{OUT} = 0.1\mu F$, unless otherwise noted.

PSRR (RIPPLE REJECTION) vs FREQUENCY

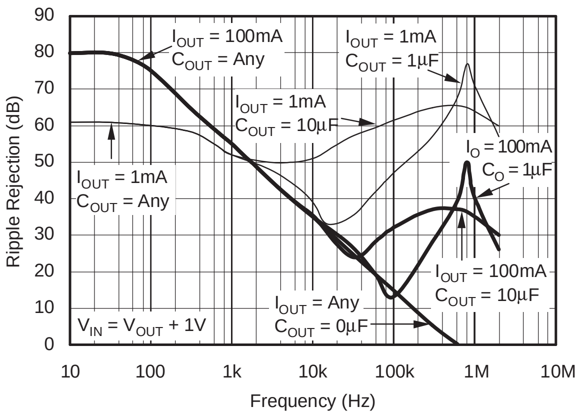


Figure 15.

PSRR (RIPPLE REJECTION) vs $V_{IN} - V_{OUT}$

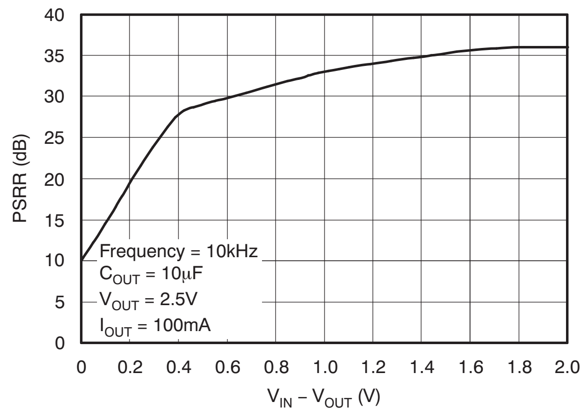


Figure 16.

NOISE SPECTRAL DENSITY
$C_{NR} = 0\mu F$

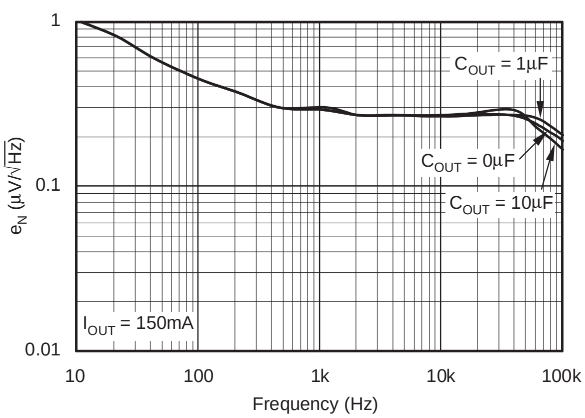


Figure 17.

NOISE SPECTRAL DENSITY
$C_{NR} = 0.01\mu F$

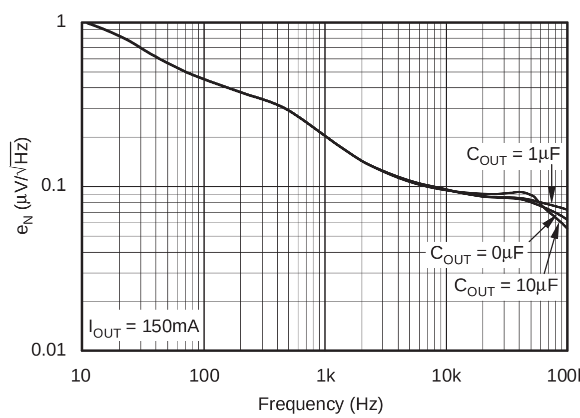


Figure 18.

RMS NOISE VOLTAGE vs C_{OUT}

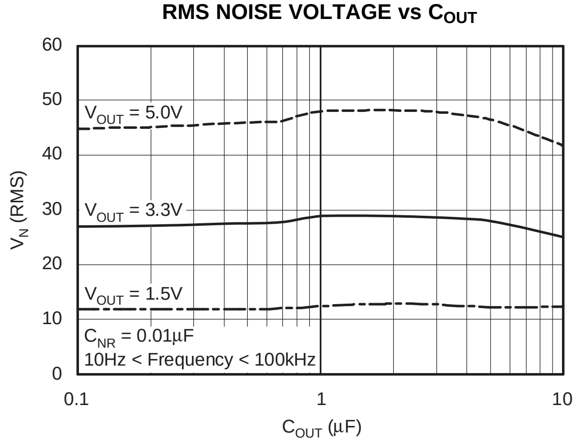


Figure 19.

RMS NOISE VOLTAGE vs C_{NR}

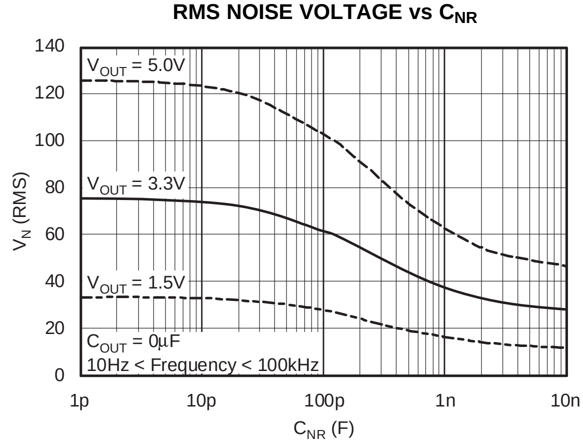


Figure 20.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions, at T_J = +25°C, V_{IN} = 24V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1μF, unless otherwise noted.

TPS73633
LOAD TRANSIENT RESPONSE

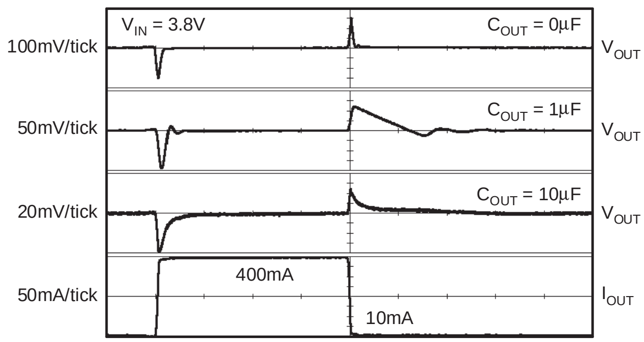


Figure 21.

TPS73633
LINE TRANSIENT RESPONSE

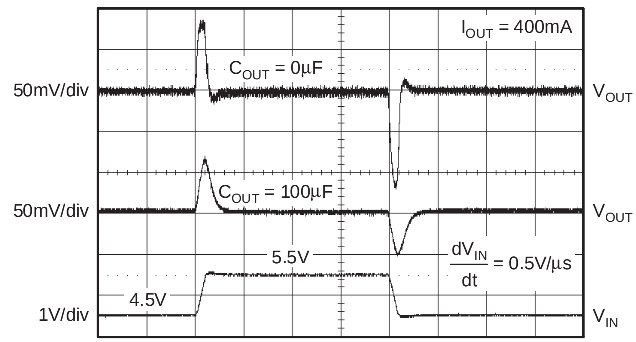


Figure 22.

TPS73633
TURN-ON RESPONSE

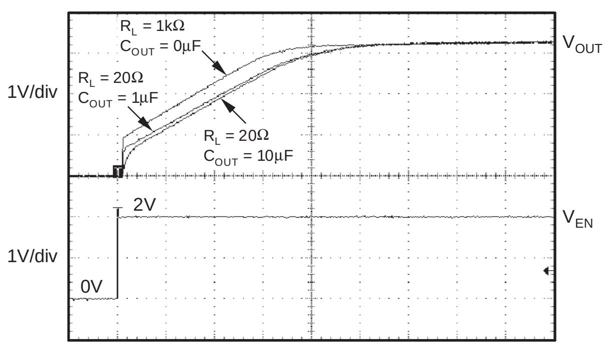


Figure 23.

TPS73633
TURN-OFF RESPONSE

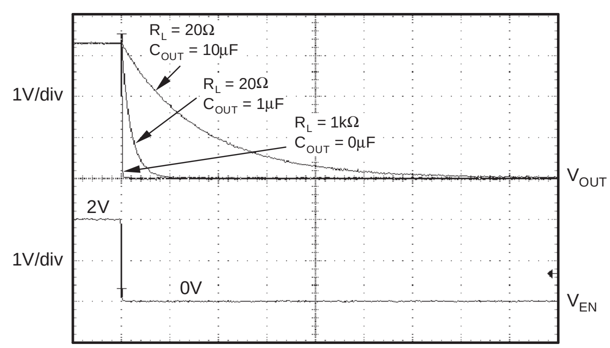


Figure 24.

TPS73633
POWER UP / POWER DOWN

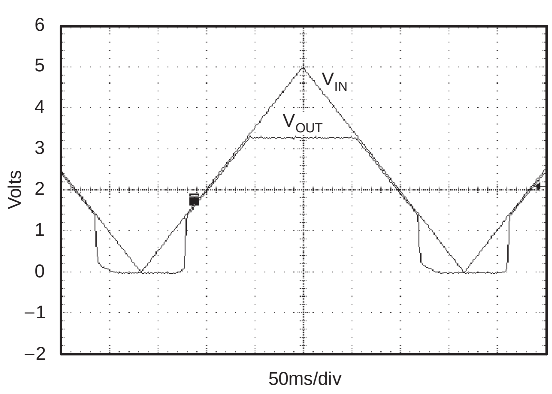


Figure 25.

I_{ENABLE} vs TEMPERATURE

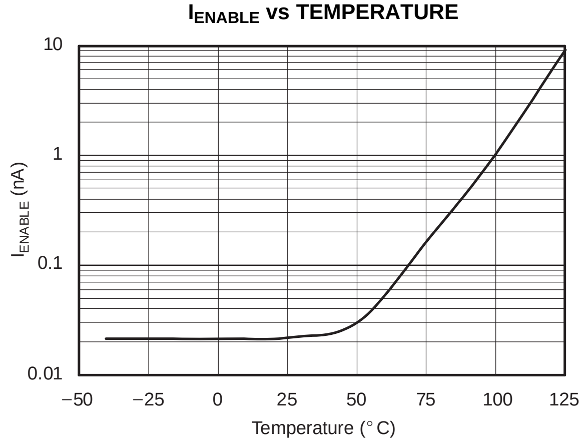


Figure 26.

TYPICAL CHARACTERISTICS (continued)

For all voltage versions, at T_J = +25°C, V_{IN} = 24V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF, unless otherwise noted.

TPS73601
RMS NOISE VOLTAGE vs C_{FB}

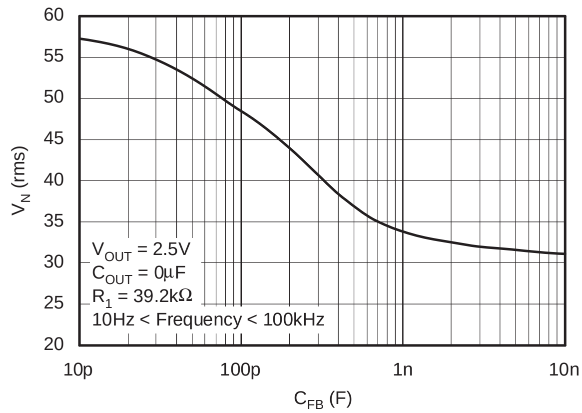


Figure 27.

TPS73601
I_{FB} vs TEMPERATURE

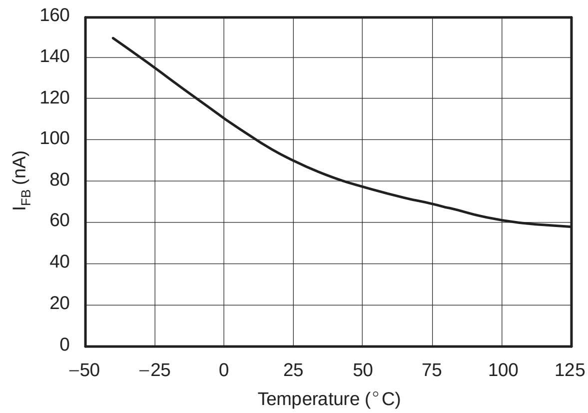


Figure 28.

TPS73601
LOAD TRANSIENT, ADJUSTABLE VERSION

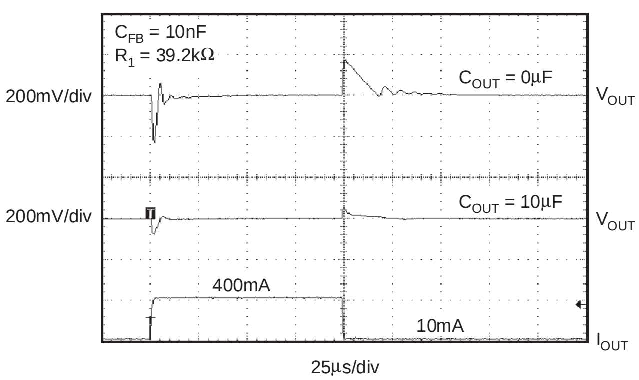


Figure 29.

TPS73601
LINE TRANSIENT, ADJUSTABLE VERSION

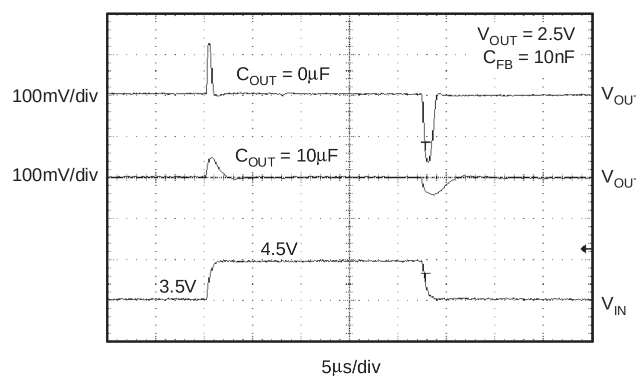


Figure 30.

APPLICATION INFORMATION

The TPS73619 belongs to a family of new generation LDO regulators that use an NMOS pass transistor to achieve ultra-low-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features, combined with low noise and an enable input, make the TPS73619 ideal for portable applications. This regulator family offers a wide selection of fixed output voltage versions and an adjustable output version. All versions have thermal and over-current protection, including foldback current limit.

Figure 31 shows the basic circuit connections for the fixed voltage models.

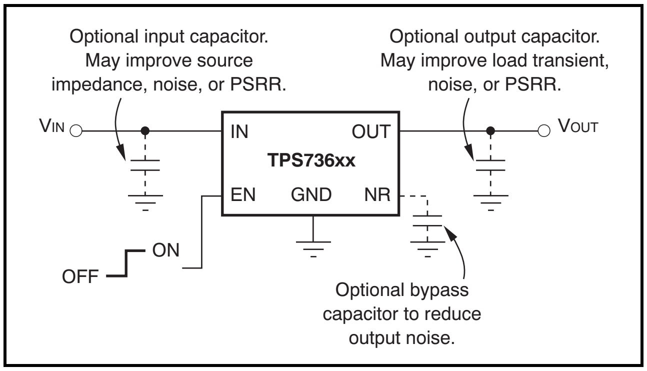


Figure 31. Typical Application Circuit for Fixed-Voltage Versions

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1μF to 1μF low ESR capacitor across the input supply near the regulator. This counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS73619 does not require an output capacitor for stability and has maximum phase margin with no capacitor. It is designed to be stable for all available types and values of capacitors. In applications where multiple low ESR capacitors are in parallel, ringing may occur when the product of C_{OUT} and total ESR drops below 50nΩF. Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder joint resistance. In most applications, the sum of capacitor ESR and trace resistance will meet this requirement.

OUTPUT NOISE

A precision band-gap reference is used to generate the internal reference voltage, V_{REF}. This reference is the dominant noise source within the TPS73619 and it generates approximately 32μV_{RMS} (10Hz to 100kHz) at the reference output (NR). The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by:

$$V_N = 32\mu V_{RMS} \times \frac{(R_1 + R_2)}{R_2} = 32\mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \quad (1)$$

Since the value of V_{REF} is 1.2V, this relationship reduces to:

$$V_N(\mu V_{RMS}) = 27\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (2)$$

for the case of no C_{NR}.

An internal 27kΩ resistor in series with the noise reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise reduction capacitor, C_{NR}, is connected from NR to ground. For C_{NR} = 10nF, the total noise in the 10Hz to 100kHz bandwidth is reduced by a factor of ~3.2, giving the approximate relationship:

$$V_N(\mu V_{RMS}) = 8.5\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \quad (3)$$

for C_{NR} = 10nF.

This noise reduction effect is shown as RMS Noise Voltage vs C_{NR} in the Typical Characteristics section.

The TPS73619 uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass element above V_{OUT}. The charge pump generates ~250μV of switching noise at ~4MHz; however, charge-pump noise contribution is negligible at the output of the regulator for most values of I_{OUT} and C_{OUT}.

BOARD LAYOUT RECOMMENDATION TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

INTERNAL CURRENT LIMIT

The TPS73619 internal current limit helps protect the regulator during fault conditions. Foldback current limit helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when V_{OUT} drops below 0.5V. See Figure 12 in the Typical Characteristics section.

Note from Figure 12 that approximately –0.2V of V_{OUT} results in a current limit of 0mA. Therefore, if OUT is forced below –0.2V before EN goes high, the device may not start up. In applications that work with both a positive and negative voltage supply, the TPS73619 should be enabled first.

ENABLE PIN AND SHUTDOWN

The enable pin (EN) is active high and is compatible with standard TTL-CMOS levels. A V_{EN} below 0.5V (max) turns the regulator off and drops the GND pin current to approximately 10nA. When EN is used to shutdown the regulator, all charge is removed from the pass transistor gate, and the output ramps back up to a regulated V_{OUT} (see Figure 23).

When shutdown capability is not required, EN can be connected to V_{IN}. However, the pass gate may not be discharged using this configuration, and the pass transistor may be left on (enhanced) for a significant time after V_{IN} has been removed. This scenario can result in reverse current flow (if the IN pin is low impedance) and faster ramp times upon power-up. In addition, for V_{IN} ramp times slower than a few milliseconds, the output may overshoot upon power-up.

Note that current limit foldback can prevent device start-up under some conditions. See the *Internal Current Limit* section for more information.

DROPOUT VOLTAGE

The TPS73619 uses an NMOS pass transistor to achieve extremely low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the NMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS\text{-}ON}$ of the NMOS pass element.

For large step changes in load current, the TPS73619 requires a larger voltage drop from V_{IN} to V_{OUT} to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the dc dropout. Values of V_{IN} – V_{OUT} above this line ensure normal transient response.

Operating in the transient dropout region can cause an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom (V_{IN} to V_{OUT} voltage drop). Under worst-case conditions [full-scale instantaneous load change with (V_{IN} – V_{OUT}) close to dc dropout levels], the TPS73619 can take a couple of hundred microseconds to return to the specified regulation accuracy.

TRANSIENT RESPONSE

The low open-loop output impedance provided by the NMOS pass element in a voltage follower configuration allows operation without an output capacitor for many applications. As with any regulator, the addition of a capacitor (nominal value 1μF) from the OUT pin to ground will reduce undershoot magnitude but increase its duration. In the adjustable version, the addition of a capacitor, C_{FB}, from the OUT pin to the FB pin will also improve the transient response.

The TPS73619 does not have active pull-down when the output is over-voltage. This allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This also results in an output overshoot of several percent if load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot can be reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor C_{OUT} and the internal/external load resistance. The rate of decay is given by:

(Fixed Voltage Version)

$$dV/dt = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \parallel R_{LOAD}} \quad (4)$$

REVERSE CURRENT

The NMOS pass element of the TPS73619 provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass device is pulled low. To ensure that all charge is removed from the gate of the pass element, the EN pin must be driven low before the input voltage is removed. If this is not done, the pass element may be left on due to stored charge on the gate.

After the EN pin is driven low, no bias voltage is needed on any pin for reverse current blocking. Note that reverse current is specified as the current flowing out of the IN pin due to voltage applied on the OUT pin. There will be additional current flowing into the OUT pin due to the 80kΩ internal resistor divider to ground (see Figure 2).

THERMAL PROTECTION

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS73619 has been designed to protect against overload conditions. It was not intended to replace proper heat sinking. Continuously running the TPS73619 into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are shown in the Thermal Information table. Using heavier copper will increase the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers will also improve the heat-sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (5)$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

PACKAGE MOUNTING

Solder pad footprint recommendations for the TPS73619 are presented in Application Bulletin *Solder Pad Recommendations for Surface-Mount Devices* (SBFA015), available from the Texas Instruments web site at www.ti.com.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS73619DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS73619DRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS73619DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS73619DRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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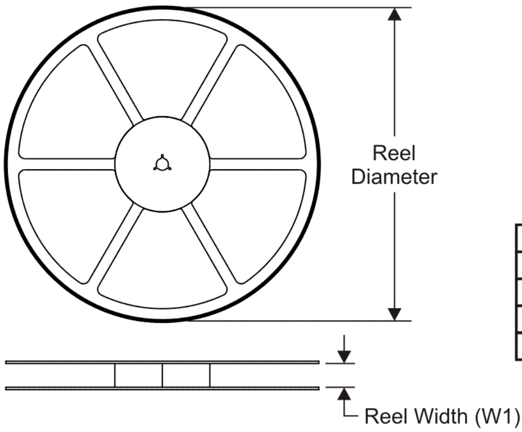
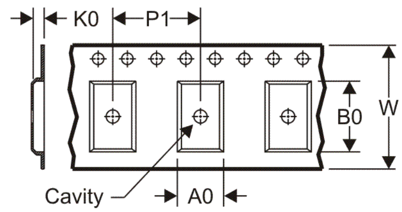
TAPE AND REEL INFORMATION

REEL DIMENSIONS

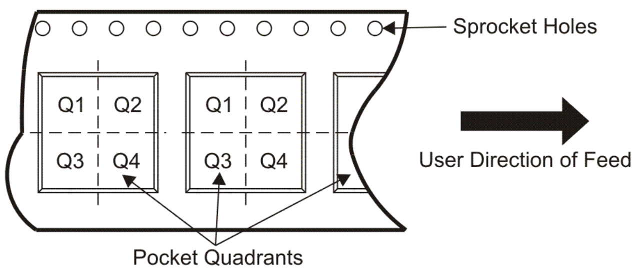


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

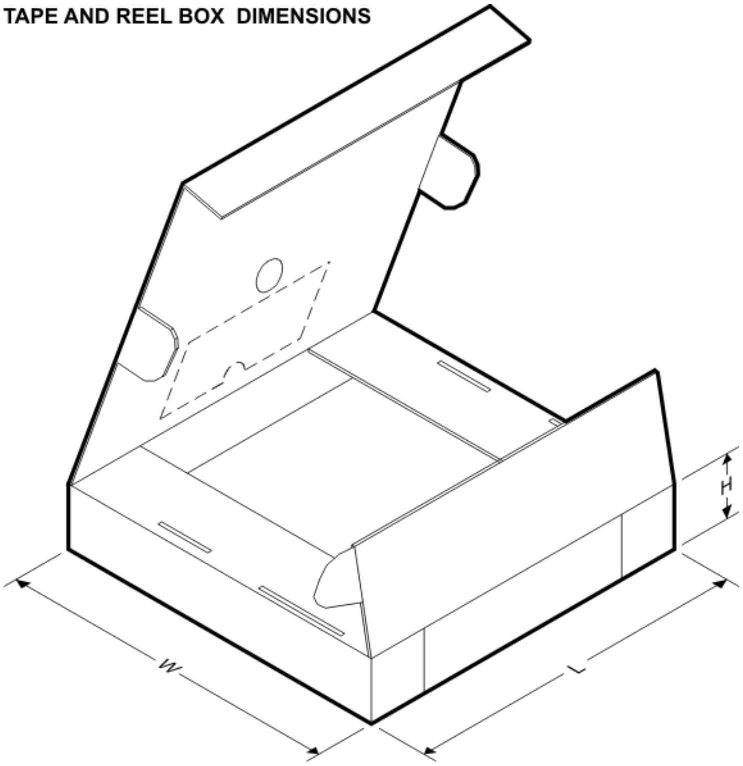
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73619DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
TPS73619DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2

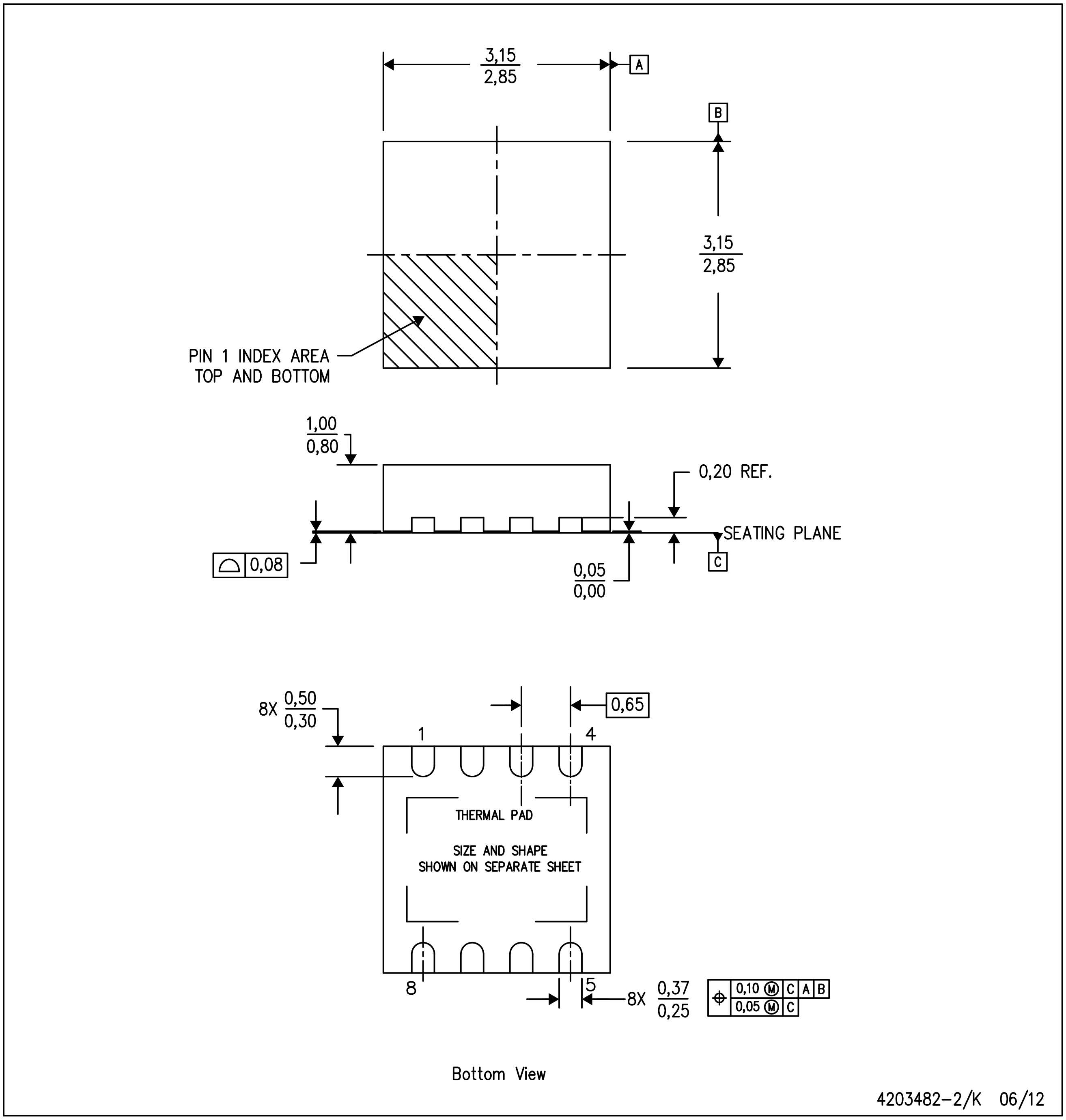
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73619DRBR	SON	DRB	8	3000	370.0	355.0	55.0
TPS73619DRBT	SON	DRB	8	250	220.0	205.0	50.0

DRB (S-PVSON-N8) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Small Outline No-Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

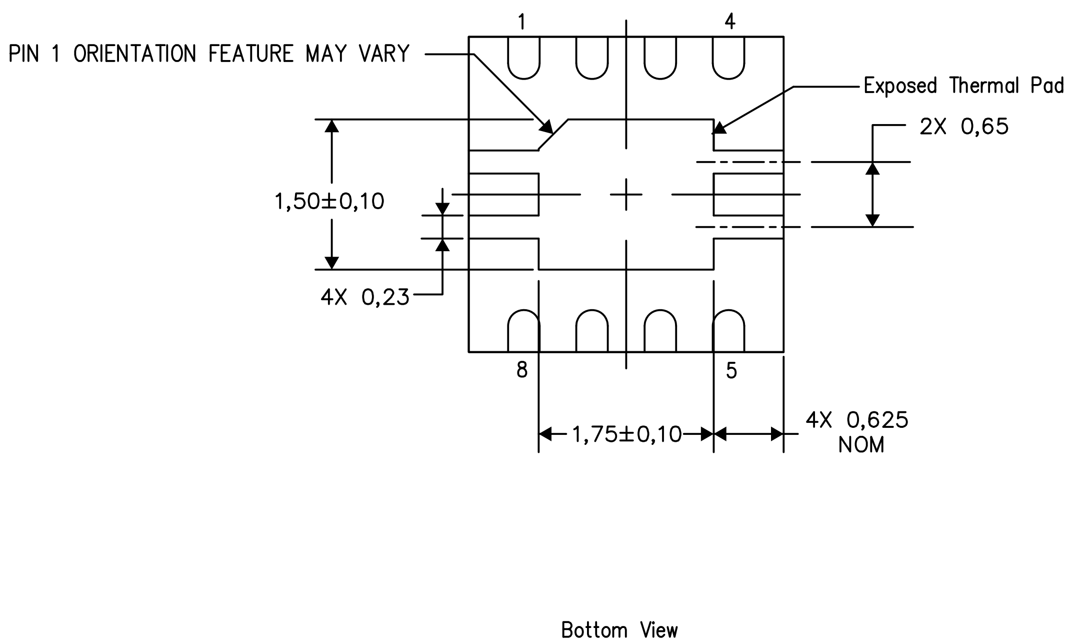
DRB (S-PVSON-N8) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

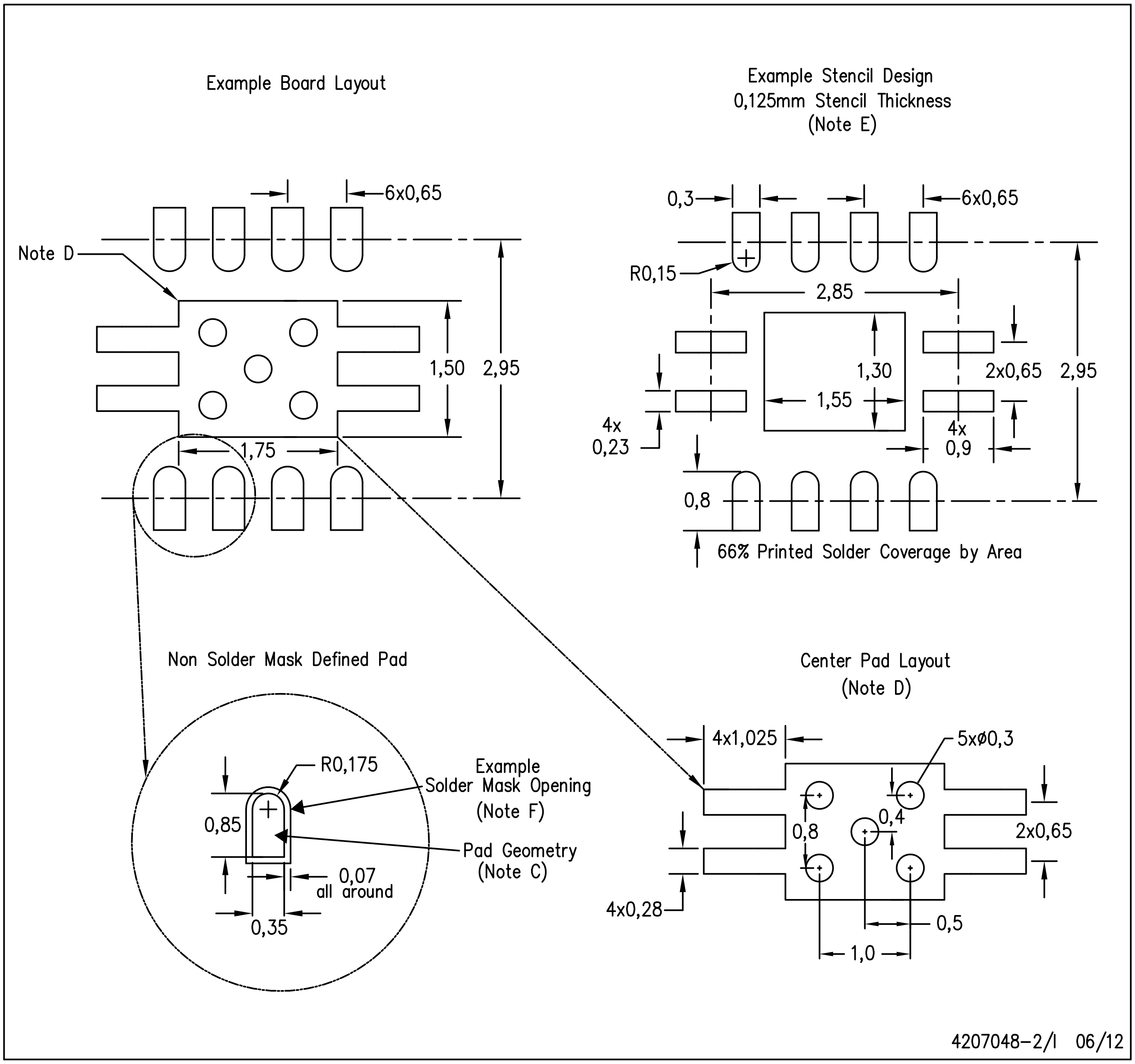


Exposed Thermal Pad Dimensions

4206340-2/M 06/12

NOTE: All linear dimensions are in millimeters

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.