28-V Input Voltage, 50-mA Voltage Regulator

Check for Samples: TPS7A42

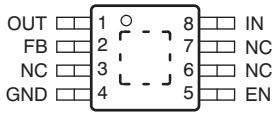
FEATURES

- **Wide Input Voltage Range: 7 V to 28 V**
- **Accuracy:**
  - **Nominal: 1%**
  - **Over Line, Load, and Temperature: 2.5%**
- **Low Quiescent Current: 25 µA**
- **Quiescent Current at Shutdown: 4.1 µA**
- **Maximum Output Current: 50 mA**
- **CMOS Logic-Level-Compatible Enable Pin**
- **Adjustable Output Voltage: ~1.175 V to 26 V**
- **Stable with Ceramic Capacitors:**
  - **Input Capacitance: ≥ 1 µF**
  - **Output Capacitance: ≥ 4.7 µF**
- **Dropout Voltage: 290 mV**
- **Built-In Current-Limit and Thermal Shutdown Protection**
- **Package: High Thermal Performance MSOP-8 PowerPAD™**
- **Operating Temperature Range: –40°C to +125°C**

APPLICATIONS

- **Microprocessors, Microcontrollers Powered by Industrial Busses with High Voltage Transients**
- **Industrial Automation**
- **Automotive**
- **LED Lighting**

DGN PACKAGE
3-mm × 5-mm MSOP-8 PowerPAD
(TOP VIEW)



DESCRIPTION

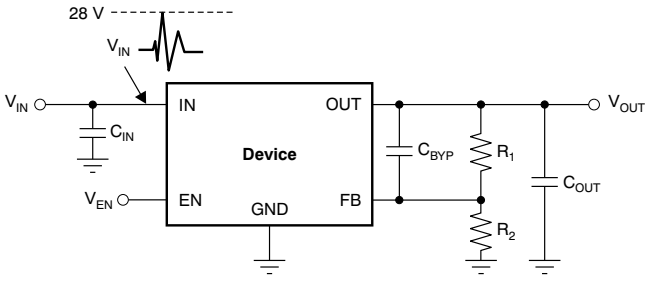
The TPS7A42 is a very high voltage-tolerant linear regulator that offers the benefits of a thermally-enhanced package (MSOP-8), and is able to withstand continuous dc or transient input voltages of up to 28 V.

The TPS7A42 is stable with any output capacitance greater than 4.7 µF and any input capacitance greater than 1 µF (over temperature and tolerance). Therefore, implementations of this device require minimal board space because of its miniaturized packaging (MSOP-8) and a potentially small output capacitor. In addition, the TPS7A42 offers an enable pin (EN) compatible with standard CMOS logic to enable a low-current shutdown mode.

The TPS7A42 has an internal thermal shutdown and current limiting to protect the system during fault conditions. The MSOP-8 packages has an operating temperature range of T_J = –40°C to +125°C.

In addition, the TPS7A42 is ideal for generating a low-voltage supply from intermediate voltage rails in telecom and industrial applications; not only it can supply a well-regulated voltage rail, but it can also withstand and maintain regulation during fast voltage transients. These features translate to simpler and more cost-effective electrical surge-protection circuitry for a wide range of applications.

Typical Application



Post DC/DC Converter Regulation for High-Performace Analog Circuitry

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT}
TPS7A4201 ***yyy z***	**YYY** is package designator. **Z** is package quantity.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		VALUE		UNIT
		MIN	MAX	
Voltage	IN pin to GND pin	–0.3	+30	V
	OUT pin to GND pin	–0.3	+30	V
	OUT pin to IN pin	–30	+0.3	V
	FB pin to GND pin	–0.3	+2	V
	FB pin to IN pin	–30	+0.3	V
	EN pin to IN pin	–30	0.3	
	EN pin to GND pin	–0.3	+30	V
Current	Peak output	Internally limited		
Temperature	Operating virtual junction, T_J	–40	+125	°C
	Storage, T_{stg}	–65	+150	°C
Electrostatic discharge rating	Human body model (HBM)		2.5	kV
	Charged device model (CDM)		500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS7A42 DGN (MSOP) 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	66.7	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	54.1	
θ_{JB}	Junction-to-board thermal resistance	38.1	
ψ_{JT}	Junction-to-top characterization parameter	2.0	
ψ_{JB}	Junction-to-board characterization parameter	37.8	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	15.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\theta JA}$	$R_{\theta JC}$	DERATING FACTOR ABOVE T_A = +25°C	$T_A \le$ +25°C POWER RATING	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
High-K(1)	DGN	55.9°C/W	8.47°C/W	16.6mW/°C	1.83W	1.08W	0.833W

(1) The JEDEC High-K (2s2p) board design used to derive this data was a 3-inch x 3-inch multilayer board with 2-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

ELECTRICAL CHARACTERISTICS

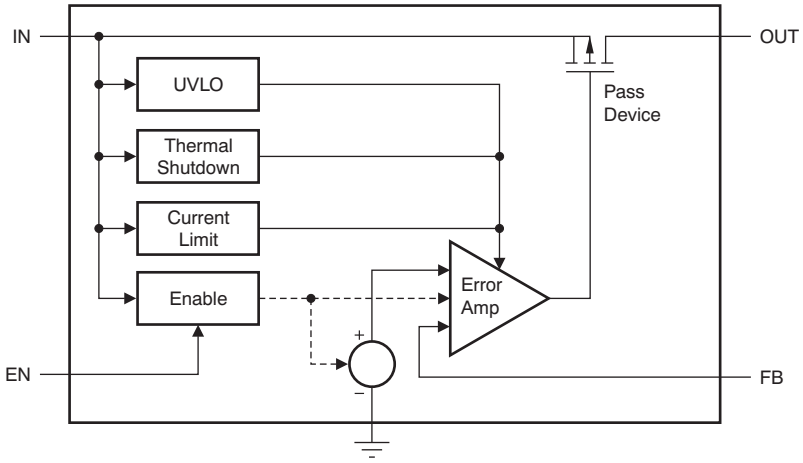
At T_J = –40°C to +125°C, V_{IN} = $V_{OUT(NOM)}$ + 2.0 V or V_{IN} = 7.0 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 100 µA, C_{IN} = 1 µF, C_{OUT} = 4.7 µF, and FB tied to OUT, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TPS7A42			UNIT
			MIN	TYP	MAX	
V_{IN}	Input voltage range		7.0		28.0	V
V_{REF}	Internal reference	T_J = +25°C, V_{FB} = V_{REF}, V_{IN} = 9 V, I_{OUT} = 25 mA	1.161	1.173	1.185	V
V_{OUT}	Output voltage range(1)	V_{IN} ≥ $V_{OUT(NOM)}$ + 2.0 V	V_{REF}		26	V
	Nominal accuracy	T_J = +25°C, V_{IN} = 9 V, I_{OUT} = 25 mA	–1.0		+1.0	%V_{OUT}
	Overall accuracy	$V_{OUT(NOM)}$ + 2.0 V ≤ V_{IN} ≤ 24 V(2) 100 µA ≤ I_{OUT} ≤ 50 mA	–2.5		+2.5	%V_{OUT}
$\Delta V_{O(\Delta VI)}$	Line regulation	7 V ≤ V_{IN} ≤ 28 V		0.03		%V_{OUT}
$\Delta V_{O(\Delta VL)}$	Load regulation	100 µA ≤ I_{OUT} ≤ 50 mA		0.31		%V_{OUT}
V_{DO}	Dropout voltage	V_{IN} = 17 V, $V_{OUT(NOM)}$ = 18 V, I_{OUT} = 20 mA		290		mV
		V_{IN} = 17 V, $V_{OUT(NOM)}$ = 18 V, I_{OUT} = 50 mA		0.78	1.3	V
I_{LIM}	Current limit	V_{OUT} = 90% $V_{OUT(NOM)}$, V_{IN} = 7.0 V, T_J ≤ +85°C	51	117	200	mA
		V_{OUT} = 90% $V_{OUT(NOM)}$, V_{IN} = 9.0 V	51	128	200	mA
I_{GND}	Ground current	7 V ≤ V_{IN} ≤ 28 V, I_{OUT} = 0 mA		25	65	µA
		I_{OUT} = 50 mA		25		µA
I_{SHDN}	Shutdown supply current	V_{EN} = +0.4 V		4.1	20	µA
I_{FB}	Feedback current(3)		–0.1	0.01	0.1	µA
I_{EN}	Enable current	7 V ≤ V_{IN} ≤ 28 V, V_{IN} = V_{EN}		0.02	1.0	µA
V_{EN_HI}	Enable high-level voltage		1.5		V_{IN}	V
V_{EN_LO}	Enable low- level voltage		0		0.4	V
V_{NOISE}	Output noise voltage	V_{IN} = 12 V, $V_{OUT(NOM)}$ = V_{REF}, C_{OUT} = 10 µF, BW = 10 Hz to 100 kHz		58		μV_{RMS}
		V_{IN} = 12 V, $V_{OUT(NOM)}$ = 5 V, C_{OUT} = 10 µF, C_{BYP}(4) = 10 nF, BW = 10 Hz to 100 kHz		73		μV_{RMS}
PSRR	Power-supply rejection ratio	V_{IN} = 12 V, $V_{OUT(NOM)}$ = 5 V, C_{OUT} = 10 µF, C_{BYP}(4) = 10 nF, f = 100 Hz		65		dB
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		+170		°C
		Reset, temperature decreasing		+150		°C
T_J	Operating junction temperature range		–40		+125	°C

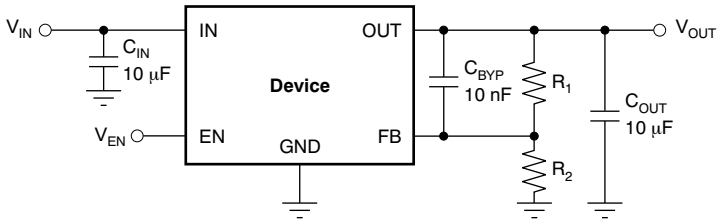
(1) To ensure stability at no-load conditions, a current from the feedback resistive network greater than or equal to 10 µA is required.
(2) Maximum input voltage is limited to 24 V because of the package power dissipation limitations at full load ($P \approx (V_{IN} - V_{OUT}) \times I_{OUT} = (24\ V - V_{REF}) \times 50\ mA \approx 1.14\ W$). The device is capable of sourcing a maximum current of 50mA at higher input voltages as long as the power dissipated is within the thermal limits of the package plus any external heatsinking.
(3) I_{FB} > 0 flows out of the device.
(4) C_{BYP} refers to a bypass capacitor connected to the FB and OUT pins.

DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUIT



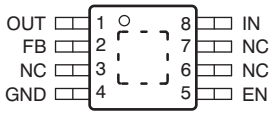
Where: $\frac{V_{OUT}}{R_1 + R_2} \geq 10\ \mu A$, and

$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right)$

Example Circuit to Maximize Transient Performance

PIN CONFIGURATION

DGN PACKAGE
MSOP-8
(TOP VIEW)



PIN DESCRIPTIONS

TPS7A42		DESCRIPTION
NAME	NO.	
EN	5	This pin turns the regulator on or off. If $V_{EN} \geq V_{EN\_HI}$ the regulator is enabled. If $V_{EN} \leq V_{EN\_LO}$, the regulator is disabled. If not used, the EN pin can be connected to IN. Make sure that $V_{EN} \leq V_{IN}$ at all times.
FB	2	This pin is the input to the control-loop error amplifier. It is used to set the output voltage of the device.
GND	4	Ground
IN	8	Input supply
NC	3, 6, 7	Not internally connected. This pin must either be left open or tied to GND.
OUT	1	Regulator output. A capacitor greater than 4.7 µF must be tied from this pin to ground to assure stability.
PowerPAD		Solder to printed circuit board (PCB) to enhance thermal performance. **NOTE: The PowerPAD is internally connected to GND.** Although it can be left floating, it is highly recommended to connect the PowerPAD to the GND plane.

TYPICAL CHARACTERISTICS

At T_J = –40°C to +125°C, V_{IN} = $V_{OUT(NOM)}$ + 2.0 V or V_{IN} = 9.0 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 100 µA, C_{IN} = 1 µF, C_{OUT} = 4.7 µF, and FB tied to OUT, unless otherwise noted.

LOAD TRANSIENT RESPONSE

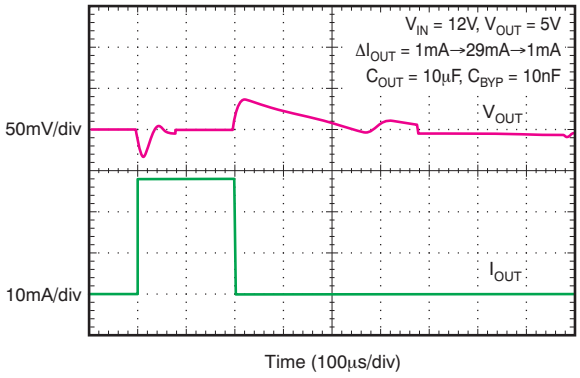


Figure 1.

LINE REGULATION

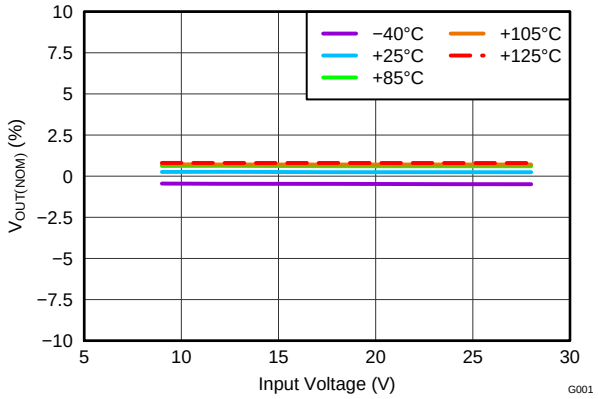


Figure 2.

FEEDBACK VOLTAGE

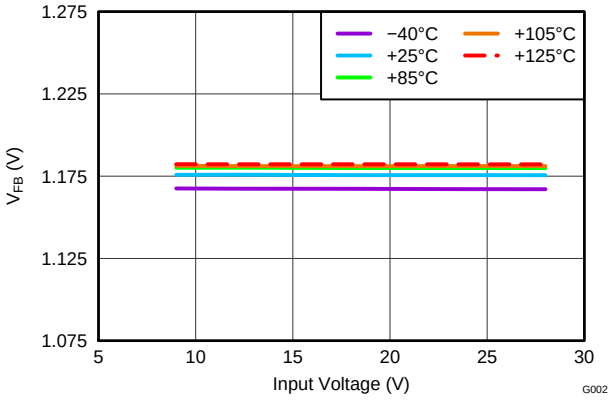


Figure 3.

QUIESCENT CURRENT vs INPUT VOLTAGE

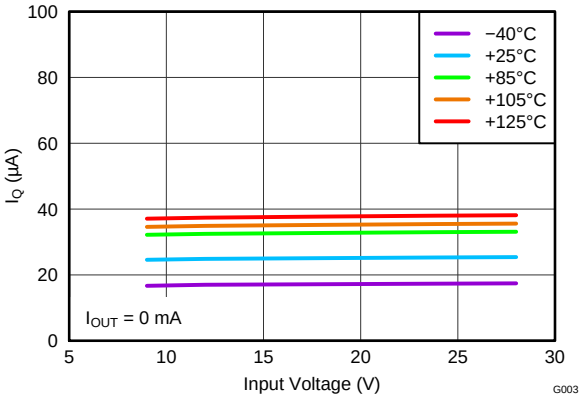


Figure 4.

FEEDBACK CURRENT

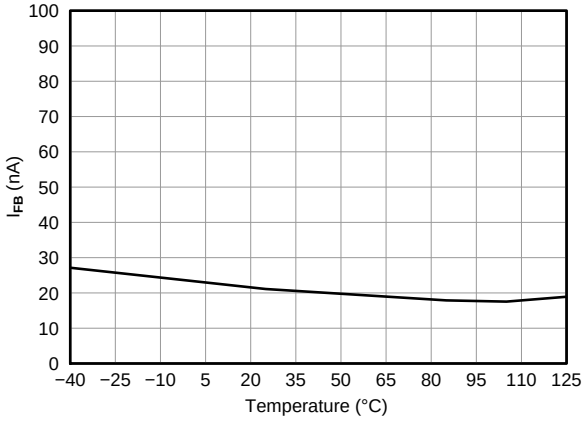


Figure 5.

GROUND CURRENT

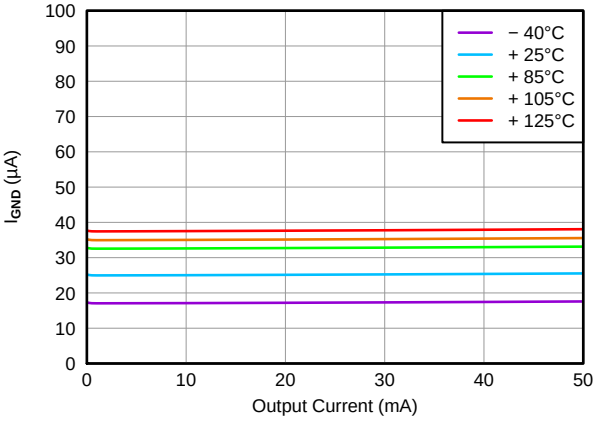


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_J = –40°C to +125°C, V_{IN} = $V_{OUT(NOM)}$ + 2.0 V or V_{IN} = 9.0 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 100 µA, C_{IN} = 1 µF, C_{OUT} = 4.7 µF, and FB tied to OUT, unless otherwise noted.

DROPOUT VOLTAGE

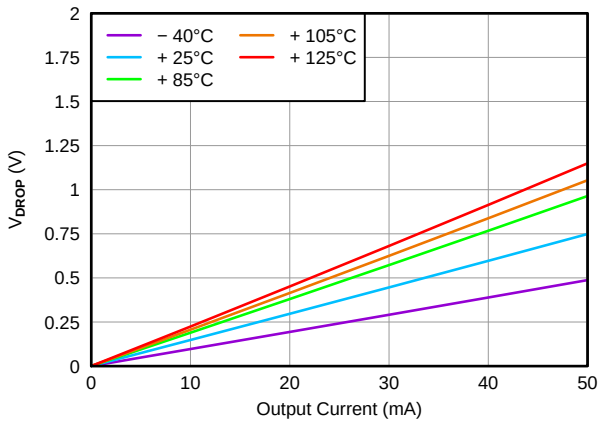


Figure 7.

ENABLE THRESHOLD VOLTAGE

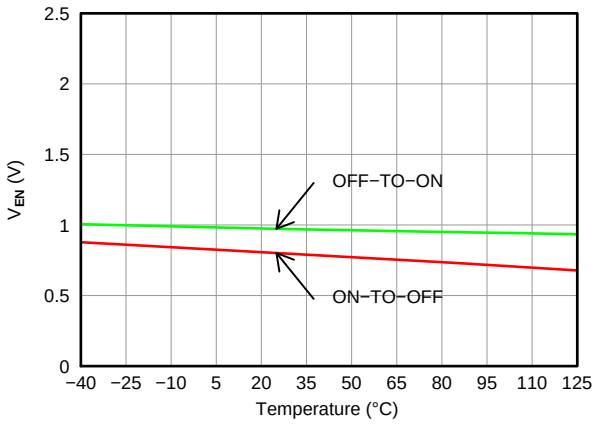


Figure 8.

OUTPUT SPECTRAL NOISE DENSITY

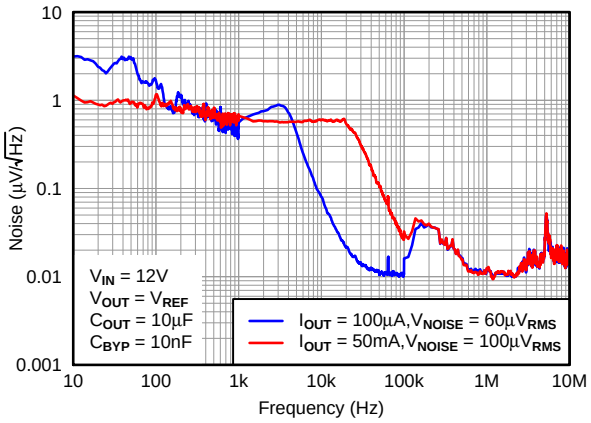


Figure 9.

CURRENT LIMIT

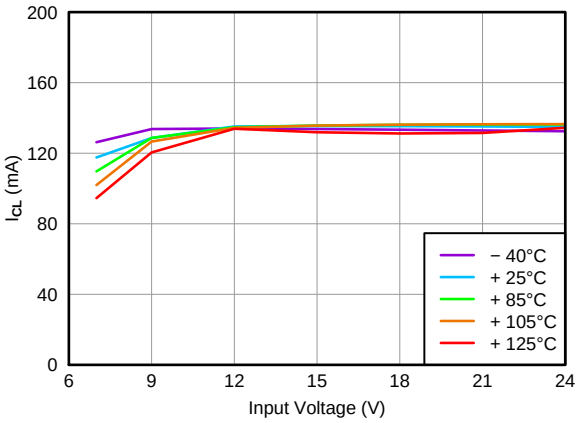


Figure 10.

POWER-SUPPLY REJECTION RATIO

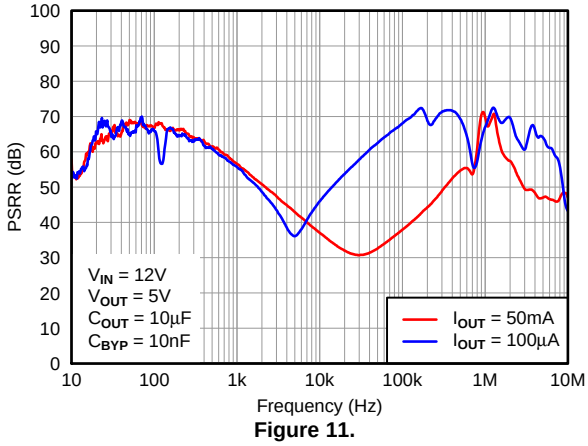


Figure 11.

THEORY OF OPERATION

GENERAL DESCRIPTION

The TPS7A4201 belongs to a new generation of linear regulators that use an innovative BiCMOS process technology to achieve very high maximum input and output voltages.

This process not only allows the TPS7A4201 to maintain regulation during very fast voltage transients up to 28 V, but it also allows the TPS7A4201 to regulate from a continuous high-voltage input rail. Unlike other regulators created using bipolar technology, the TPS7A4201 ground current is also constant over its output current range, resulting in increased efficiency and lower power consumption.

These features, combined with a high thermal performance MSOP-8 PowerPAD package, make this device ideal for industrial and telecom applications.

ADJUSTABLE OPERATION

The TPS7A4201 has an output voltage range of ~1.175 V to 26 V. The nominal output voltage of the device is set by two external resistors, as shown in Figure 12.

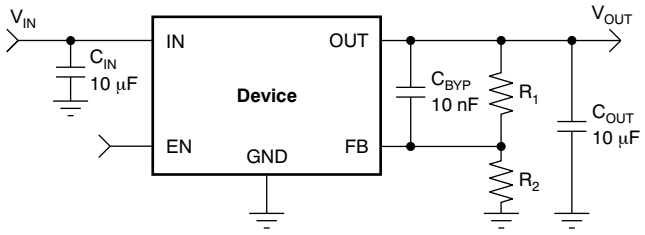


Figure 12. Adjustable Operation for Maximum AC Performance

R_1 and R_2 can be calculated for any output voltage range using the formula shown in Equation 1. To ensure stability under no-load conditions, this resistive network must provide a current greater than or equal to 10 µA.

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right), \quad \text{where } \frac{V_{OUT}}{R_1 + R_2} \geq 10\ \mu A \tag{1}$$

If greater voltage accuracy is required, take into account the output voltage offset contributions because of the feedback pin current and use 0.1% tolerance resistors.

ENABLE PIN OPERATION

The TPS7A4201 provides an enable pin (EN) feature that turns on the regulator when V_{EN} > 1.5 V.

CAPACITOR RECOMMENDATIONS

Low equivalent series resistance (ESR) capacitors should be used for the input, output, and bypass capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved over-temperature performance, while ceramic X5R capacitors are the most cost-effective and are available in higher values.

Note that high ESR capacitors may degrade PSRR.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

The TPS7A4201 high voltage linear regulator achieves stability with a minimum output capacitance of 4.7 µF and input capacitance of 1 µF; however, it is highly recommended to use 10-µF output and input capacitors to maximize ac performance.

BYPASS CAPACITOR REQUIREMENTS

Although a bypass capacitor (C_{BYP}) is not needed to achieve stability, it is highly recommended to use a 10-nF bypass capacitor to maximize ac performance (including line transient, noise and PSRR).

MAXIMUM AC PERFORMANCE

In order to maximize line transient, noise, and PSRR performance, it is recommended to include 10-µF (or higher) input and output capacitors, and a 10-nF bypass capacitor, as shown in Figure 12. The solution shown delivers minimum noise levels of 58 μV_{RMS} and power-supply rejection levels above 36 dB from 10 Hz to 10 MHz.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

Note that the presence of the C_{BYP} capacitor may greatly improve the TPS7A4201 line transient response, as noted in .

APPLICATION INFORMATION

TRANSIENT VOLTAGE PROTECTION

One of the primary applications of the TPS7A4201 is to provide transient voltage protection to sensitive circuitry that may be damaged in the presence of high-voltage spikes.

This transient voltage protection can be more cost-effective and compact compared to topologies that use a transient voltage suppression (TVS) block.

LED ARRAY DRIVER

The TPS7A4201 can be used to drive several LED drivers connected in series, as shown in Figure 13.

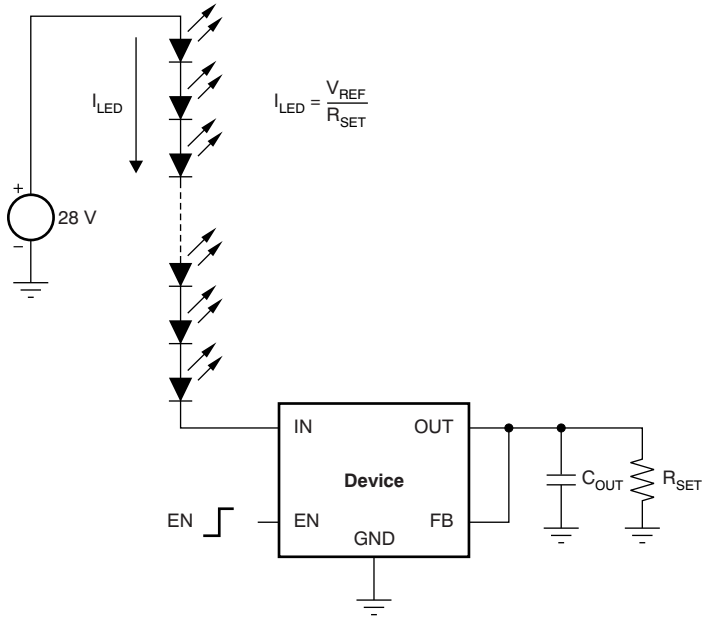


Figure 13. LED Array Driver Application

The TPS7A4201 high voltage rating makes it suitable not only for driving the intensity of an array of multiple LEDs by using a PWM signal at its EN pin, but also for controlling such an array. This PWM signal enables and disables the regulator, causing the LED light to vary its intensity.

Whenever the regulator is disabled, no current flows through the LED array. This condition means that the regulator has the same high voltage applied to the first LED in the array as is applied to the regulator input. Figure 14 illustrates the solution to this problem with the addition of the TPS7A4201 high-voltage regulator.

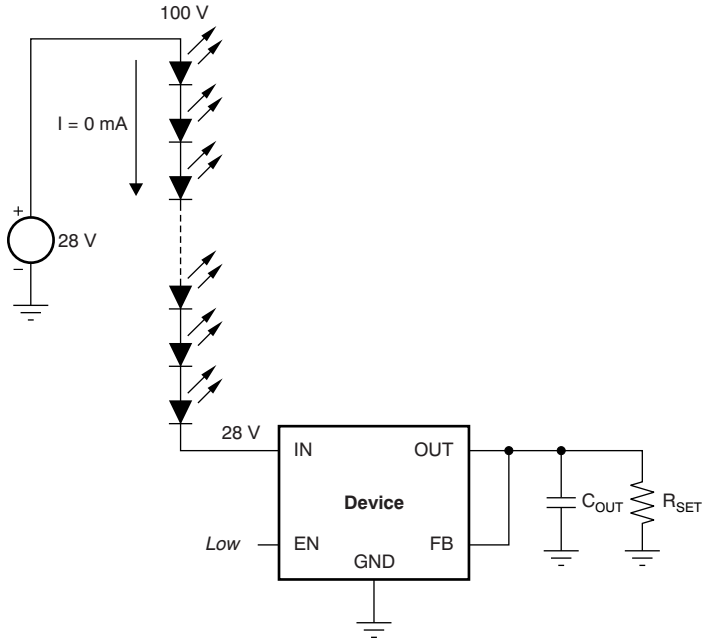


Figure 14. LED Array Driver with Regulator Disabled

LAYOUT

PACKAGE MOUNTING

Solder pad footprint recommendations for the TPS7A4201 are available at the end of this product data sheet and at www.ti.com.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for IN and OUT, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and ESR must be minimized in order to maximize performance and ensure stability. Every capacitor (C_{IN}, C_{OUT}, C_{BYP}) must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because they may impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance denoted in this product data sheet, use the same layout pattern used for TPS7A42 evaluation board, available at www.ti.com.

THERMAL PROTECTION

Thermal protection disables the output when the junction temperature rises to approximately +170°C, allowing the device to cool. When the junction temperature cools to approximately +150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to a maximum of +125°C. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A4201 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS7A4201 into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Dissipation Ratings Table*. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element, as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT})\, I_{OUT} \quad (2)$$

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS7A4201DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SBC	Samples
TPS7A4201DGNT	ACTIVE	MSOP-PowerPAD	DGN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SBC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

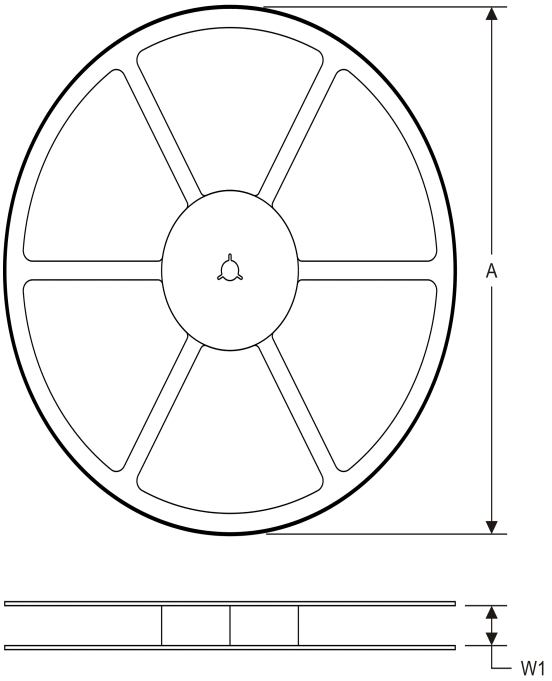
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

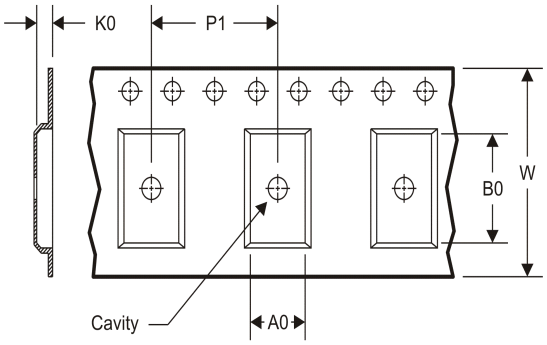
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



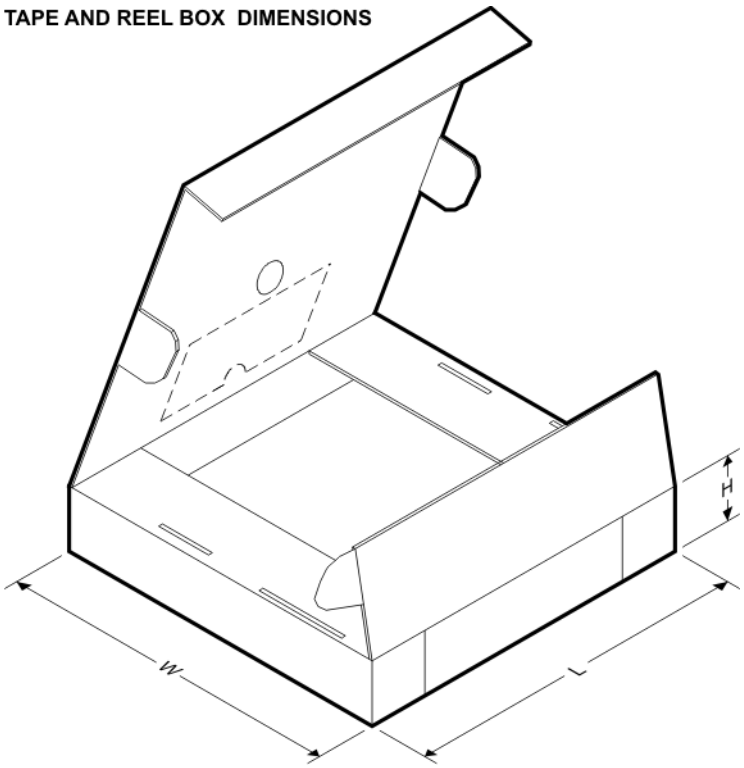
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A4201DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS7A4201DGNT	MSOP-Power PAD	DGN	8	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

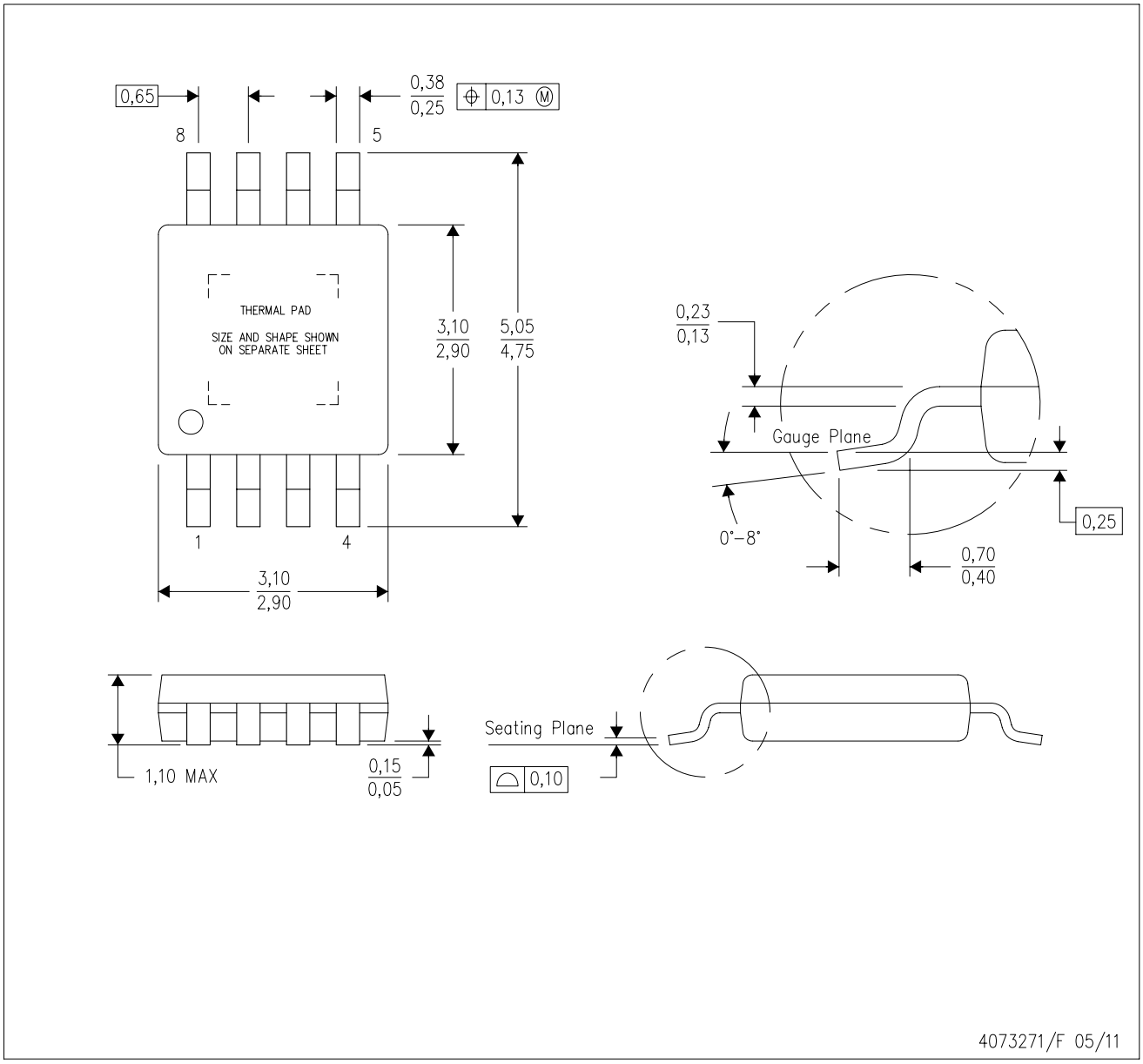
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A4201DGNR	MSOP-PowerPAD	DGN	8	2500	346.0	346.0	35.0
TPS7A4201DGNT	MSOP-PowerPAD	DGN	8	250	203.0	203.0	35.0

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

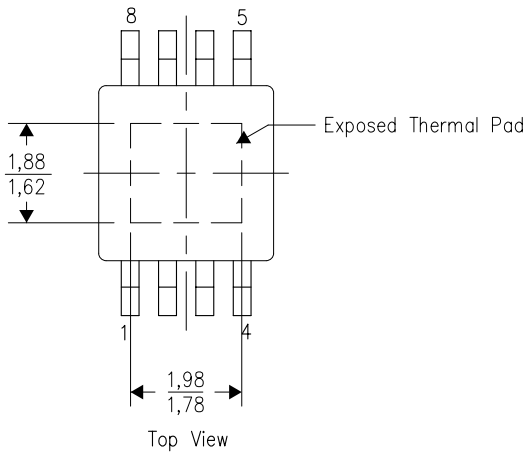
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



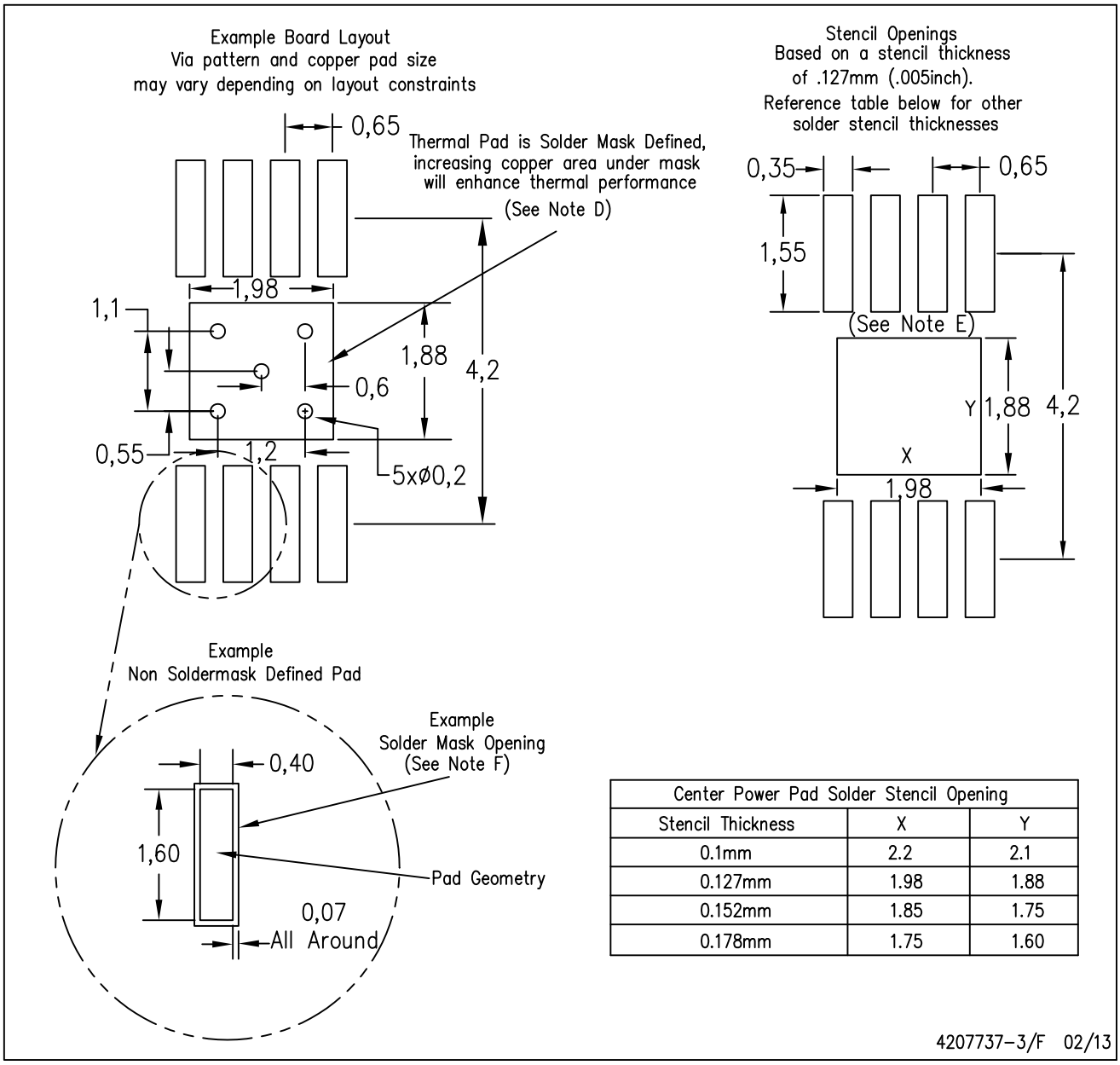
Exposed Thermal Pad Dimensions

4206323–3/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.2	2.1
0.127mm	1.98	1.88
0.152mm	1.85	1.75
0.178mm	1.75	1.60

4207737–3/F 02/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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