Low-Power, Dual-Voltage Detector in Small µSON Package

Check for Samples: TPS3779, TPS3780

FEATURES

- **Very Small Package: 1.45-mm × 1-mm µSON**
- **Low Quiescent Current: 1.8 µA (typ)**
- **High Threshold and Hysteresis Accuracy: 1.0%**
- **Adjustable Thresholds**
- **Different Hysteresis Options:**
  - **0.5%, 1%, 5%, and 10%**
- **Temperature Range: –40°C to +125°C**
- **Push-Pull (TPS3779) and Open-Drain (TPS3780) Output Options**

APPLICATIONS

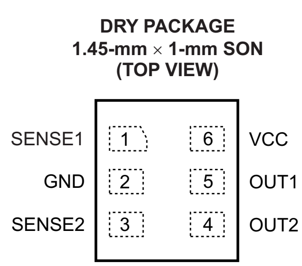
- **DSPs, Microcontrollers, or Microprocessors Applications**
- **Portable and Battery-Powered Products**
- **Cell Phones and PDAs**
- **Notebook and Desktop Computers**
- **Set-Top Boxes**

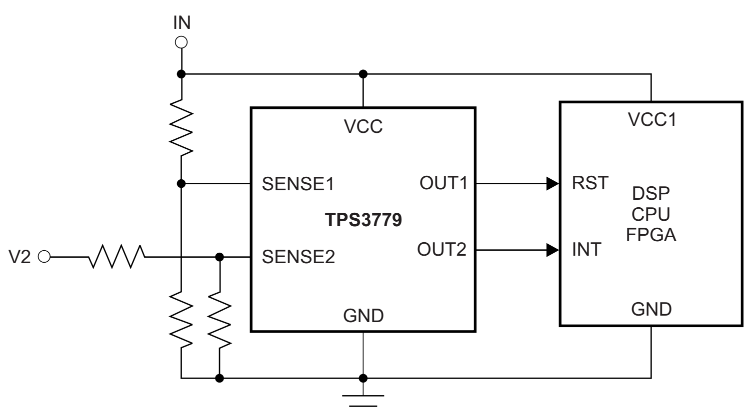
DESCRIPTION

The TPS3779 and TPS3780 are a family of two-channel voltage detectors with low-power and high-accuracy comparators, and are available in a very small µSON package. The SENSE1 and SENSE2 inputs include a built-in hysteresis for filtering to reject brief glitches, thereby ensuring stable output operation without false triggering. This family offers different factory-set hysteresis options of 0.5%, 1%, 5%, or 10%.

The TPS3779 and TPS3780 have adjustable SENSE inputs that can be configured by an external resistor divider. When the voltage at the SENSE1 or SENSE2 input goes below the falling threshold, OUT1 or OUT2 is driven low, respectively. When SENSE1 or SENSE2 rises above the rising threshold, OUT1 or OUT2 goes high, respectively.

The devices have a very low quiescent current of 1.8 µA (typical) and provide a precise, space-conscious solution for voltage detection suitable for low-power system-monitoring and portable applications. The TPS3779 and TPS3780 operate from 1.5 V to 6.5 V, over the –40°C to +125°C temperature range.





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DEVICE INFORMATION

PRODUCT	HYSTERESIS (%)	OUTPUT
TPS3779A	0.5	Push-pull
TPS3779B	5	Push-pull
TPS3779C	10	Push-pull
TPS3779D	1	Push-pull
TPS3780A	0.5	Open-drain
TPS3780B	5	Open-drain
TPS3780C	10	Open-drain
TPS3780D	1	Open-drain

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
Voltage(2)	VCC	–0.3 to +7	V
	OUT1, OUT2	–0.3 to +7	V
	SENSE1, SENSE2	–0.3 to +7	V
Current	OUT pin	±20	mA
Temperature(3)	Operating junction, T_J	–40 to +125	°C
	Storage, T_{stg}	–65 to +150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM)	2	kV
	Charge device model (CDM)	500	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute maximum- rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to the network ground terminal.
(3) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS3779 TPS3780	UNITS
		DRY (μSON)	
		6 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	306.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	174.1	
θ_{JB}	Junction-to-board thermal resistance	173.4	
ψ_{JT}	Junction-to-top characterization parameter	30.9	
ψ_{JB}	Junction-to-board characterization parameter	171.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	65.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

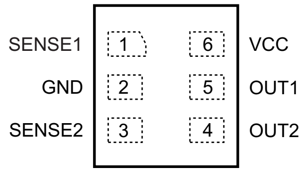
All specifications are over the operating temperature range of –40°C < T_J < +125°C and 1.5 V ≤ V_{CC} ≤ 6.5 V, unless otherwise noted. Typical values are at T_J = +25°C and V_{CC} = 3.3 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CC}	Input supply range			1.5		6.5	V
$V_{(POR)}$	Power-on reset voltage[1]	V_{OL} (max) = 0.2 V, I_{OL} = 15 µA				0.8	V
I_{CC}	Supply current (into VCC pin)	V_{CC} = 3.3 V, no load, –40°C < T_J < +85°C			1.8	3.3	µA
		V_{CC} = 3.3 V, no load, –40°C < T_J < +125°C				4.5	µA
		V_{CC} = 6.5 V, no load, –40°C < T_J < +85°C			2	3.5	µA
		V_{CC} = 6.5 V, no load, –40°C < T_J < +125°C				5	µA
V_{IT+}	Positive-going input threshold voltage	$V_{(SENSE)}$ rising			1.20		V
			0°C < T_J < +85°C	–1%		+1%	
			–40°C < T_J < +125°C	–1%		+1.3%	
V_{IT-}	Negative-going input threshold voltage	$V_{(SENSE)}$ falling	TPS37xxA (0.5% hysteresis)		1.194		V
			TPS37xxB (5% hysteresis)		1.14		V
			TPS37xxC (10% hysteresis)		1.08		V
			TPS37xxD (1% hysteresis)		1.188		V
			TPS37xxA, TPS37xxD, 0°C < T_J < +85°C	–1%		+1%	
			TPS37xxA, TPS37xxD, –40°C < T_J < +125°C	–1%		+1.3%	
			TPS37xxB, TPS37xxC, –40°C < T_J < +125°C	–1.3%		+1.3%	
$I_{(SENSE)}$	Input current[2]	$V_{(SENSE)}$ = 0 V or V_{CC}		–5		5	nA
V_{OL}	Low-level output voltage	V_{CC} ≥ 1.2 V, I_{SINK} = 0.4 mA				0.25	V
		V_{CC} ≥ 2.7 V, I_{SINK} = 2 mA				0.25	V
		V_{CC} ≥ 4.5 V, I_{SINK} = 3.2 mA				0.3	V
V_{OH}	High-level output voltage (push-pull)	V_{CC} ≥ 1.7 V, I_{SINK} = 0.4 mA		0.8 V_{CC}			V
		V_{CC} ≥ 2.7 V, I_{SINK} = 1 mA		0.8 V_{CC}			V
		V_{CC} ≥ 4.5 V, I_{SINK} = 2.5 mA		0.8 V_{CC}			V
$I_{lkg(OD)}$	Open-drain output leakage current	High impedance, $V_{(SENSE\_OUT)}$ = 6.5 V, –40°C < T_J < +85°C		–50		50	nA
		High impedance, $V_{(SENSE\_OUT)}$ = 6.5 V, –40°C < T_J < +125°C		–250		250	nA
$t_{PD(r)}$	SENSE (rising) to OUT propagation delay				4		µs
$t_{PD(f)}$	SENSE (falling) to OUT propagation delay				6		µs
	Startup delay[3] [2]				350		µs

(1) The lowest supply voltage (V_{CC}) at which the output is active ($t_{rise(VCC)}$ > 15 µs/V). Below $V_{(POR)}$, the output cannot be determined.
(2) Specified by design.
(3) During power-up, V_{CC} must exceed 1.5 V for the start-up delay time before the output is in the correct state.

PIN CONFIGURATION

DRY PACKAGE
1.45-mm × 1-mm USON
(TOP VIEW)



PIN DESCRIPTIONS

PIN		DESCRIPTION
NAME	NO.	
GND	2	Ground
OUT2	4	OUT2 is the output for SENSE2. OUT2 is asserted (driven low) when the voltage at SENSE2 falls below V_{IT-}. OUT2 is deasserted (goes high) after SENSE2 rises higher than V_{IT+}. OUT2 is a push-pull output for the TPS3779 and an open-drain output for the TPS3780. The open-drain device (TPS3780) can be pulled up to 6.5 V independent of VCC; a pull-up resistor is required for this device.
OUT1	5	OUT1 is the output for SENSE1. OUT1 is asserted (driven low) when the voltage at SENSE1 falls below V_{IT-}. OUT1 is deasserted (goes high) after SENSE1 rises higher than V_{IT+}. OUT1 is a push-pull output for the TPS3779 and an open-drain output for the TPS3780. The open-drain device (TPS3780) can be pulled up to 6.5 V independent of VCC; a pull-up resistor is required for this device.
SENSE1	1	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal drops below the threshold voltage (V_{IT-}), OUT1 is asserted.
SENSE2	3	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal drops below the threshold voltage (V_{IT-}), OUT2 is asserted.
VCC	6	Supply voltage input. Connect a 1.5-V to 6.5-V supply to VCC in order to power the device. It is good analog design practice to place a 0.1-µF ceramic capacitor close to this pin.

FUNCTIONAL BLOCK DIAGRAM

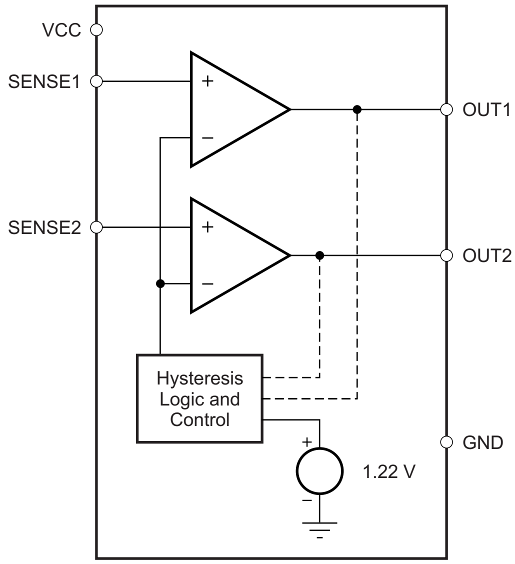


Figure 1. Block Diagram

TYPICAL CHARACTERISTICS

At T_J = +25°C and V_{CC} = 3.3 V, unless otherwise noted

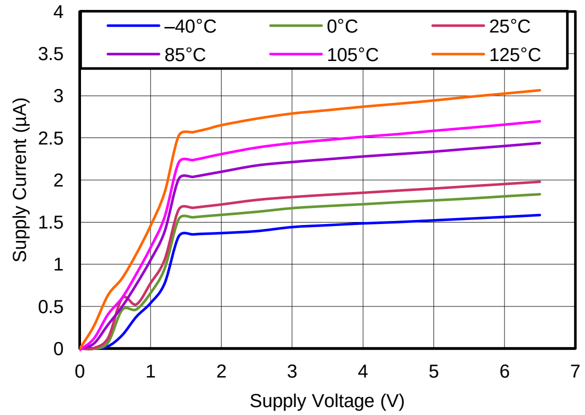


Figure 2. SUPPLY CURRENT vs SUPPLY VOLTAGE

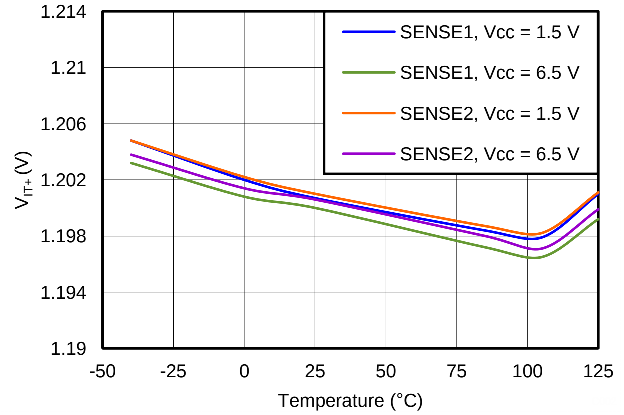


Figure 3. SENSE THRESHOLD (V_{IT+}) vs TEMPERATURE

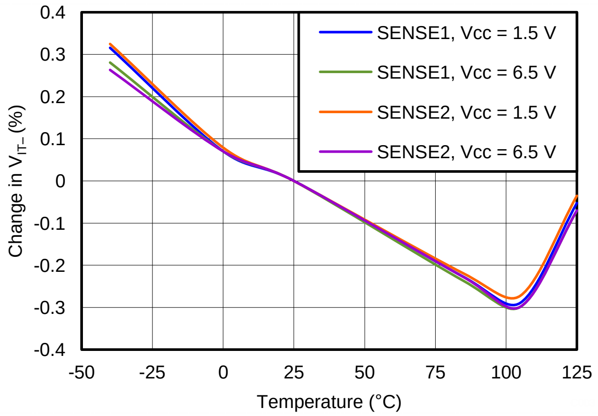


Figure 4. SENSE THRESHOLD (V_{IT-}) vs TEMPERATURE

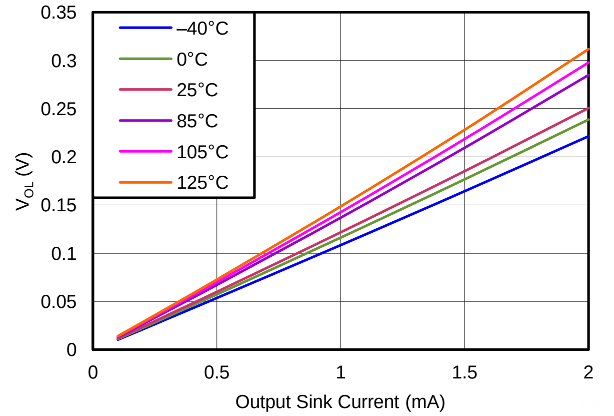


Figure 5. OUTPUT VOLTAGE LOW vs OUTPUT CURRENT (V_{CC} = 1.5 V)

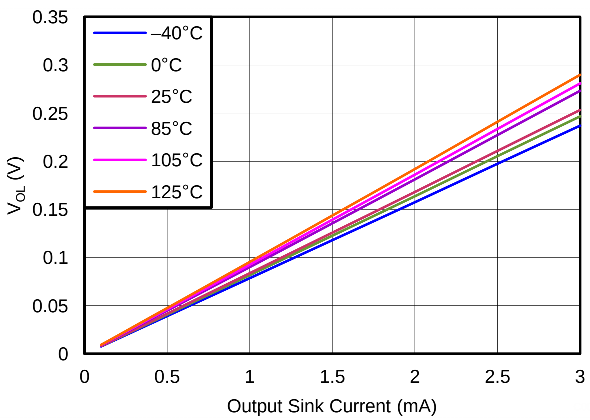


Figure 6. OUTPUT VOLTAGE LOW vs OUTPUT CURRENT (V_{CC} = 3.3 V)

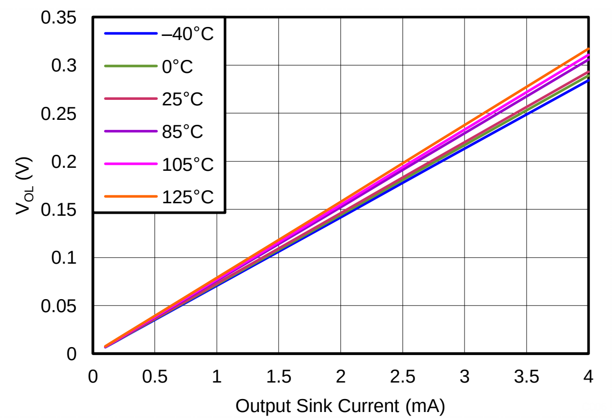


Figure 7. OUTPUT VOLTAGE LOW vs OUTPUT CURRENT (V_{CC} = 6.5 V)

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C and V_{CC} = 3.3 V, unless otherwise noted

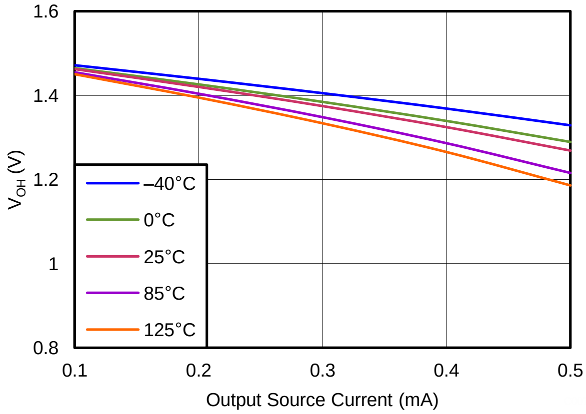


Figure 8. OUTPUT VOLTAGE HIGH vs OUTPUT CURRENT (V_{CC} = 1.5 V)

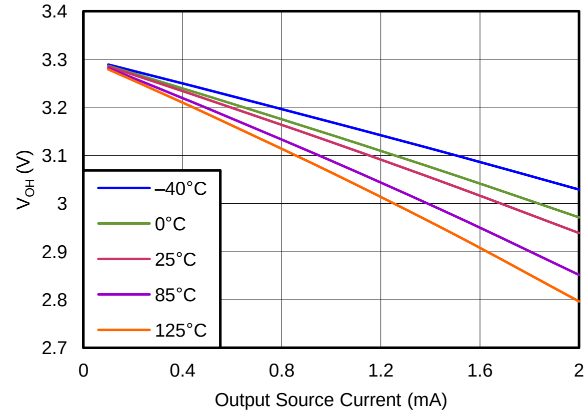


Figure 9. OUTPUT VOLTAGE HIGH vs OUTPUT CURRENT (V_{CC} = 3.3 V)

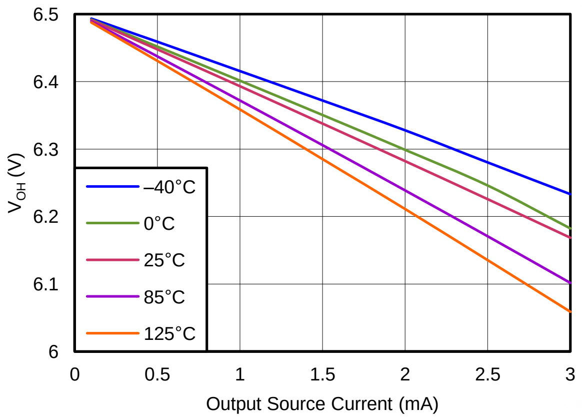


Figure 10. OUTPUT VOLTAGE HIGH vs OUTPUT CURRENT (V_{CC} = 6.5 V)

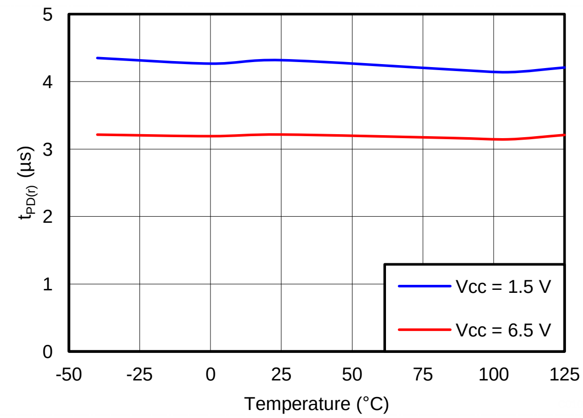


Figure 11. PROPAGATION DELAY FROM SENSE HIGH TO OUTPUT HIGH (SENSE1 and SENSE2 = 0 V to 1.3 V)

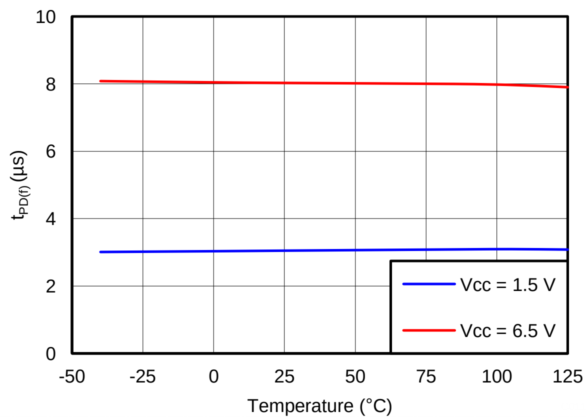


Figure 12. PROPAGATION DELAY FROM SENSE LOW TO OUTPUT LOW (SENSE1 and SENSE2 = 1.3 V to 0 V)

DETAILED DESCRIPTION

OVERVIEW

The TPS3779 and TPS3780 belong to a family of ultrasmall, low quiescent current (I_{CC}), dual-channel voltage detectors. These devices have high-accuracy, rising and falling input thresholds, and assert the output as shown in Table 1. The output (OUTx pin) goes low when the SENSEx pin is less than V_{IT-} and goes high when the pin is greater than V_{IT+}. The TPS3779 and TPS3780 offer multiple hysteresis options from 0.5% to 10% for use in wide variety of applications. These devices have two independent voltage detection channels that can be used in systems where multiple voltage rails are required to be monitored, or where one channel can be used as an early warning signal and the other channel used as the system reset signal.

Table 1. TPS33779, TPS3780 Truth Table

CONDITIONS	OUTPUT
SENSE1 < V_{IT-}	OUT1 = low
SENSE2 < V_{IT-}	OUT2 = low
SENSE1 > V_{IT+}	OUT1 = high
SENSE2 > V_{IT+}	OUT2 = high

INPUTS (SENSE1, SENSE2)

The TPS3779 and TPS3780 have two comparators for voltage detection. Each comparator has one external input; the other input is connected to the internal reference. The comparator rising threshold is designed and trimmed to be equal to V_{IT+} and the falling threshold is trimmed to be equal to V_{IT-}. The built-in falling hysteresis options make the devices immune to supply rail noise and ensures stable operation.

The comparator inputs can swing from ground to 6.5 V, regardless of the device supply voltage used. Although not required in most cases, it is good analog design practice to place a 1-nF to 10-nF bypass capacitor at the comparator input for extremely noisy applications in order to reduce sensitivity to transients and layout parasitic.

For each SENSE input, the corresponding output (OUTx) is driven to logic low when the input voltage drops below V_{IT-}. When the voltage exceeds V_{IT+}, the output (OUTx) goes to a high-impedance state, as shown in Figure 13.

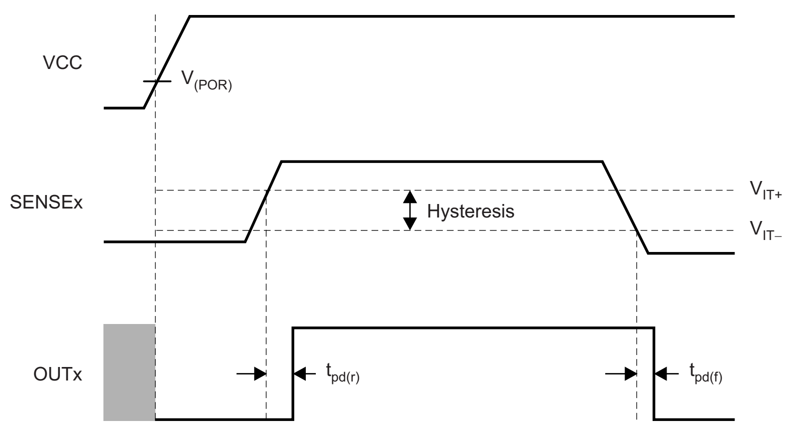


Figure 13. Timing Diagram

The TPS3779 and TPS3780 also have adjustable sense inputs that can be configured to monitor voltages using external resistor divider, as shown in Figure 14.

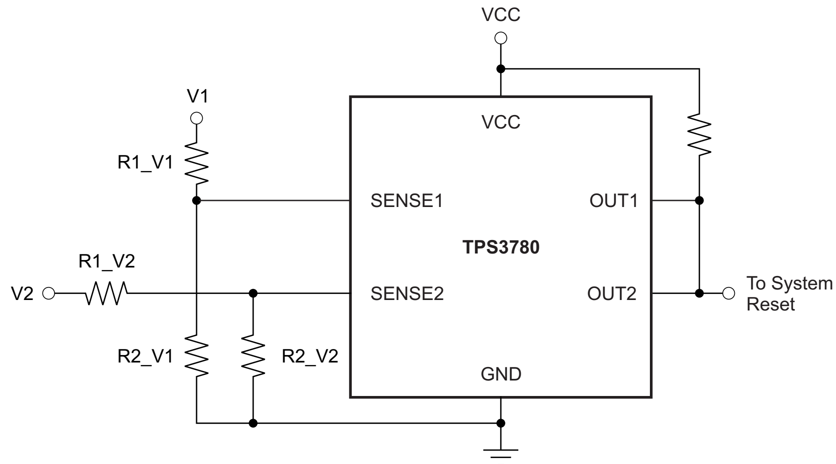


Figure 14. Application Diagram

The resistor divider values and target threshold voltage can be calculated by using Equation 1 and Equation 2 to determine $V_{MON(no\ UV)}$ and $V_{MON(UV)}$, respectively.

$$V_{MON(UV)} = \left(1 + \frac{R1}{R2}\right) \times V_{IT-} \quad (1)$$

$$V_{MON(no\ UV)} = \left(1 + \frac{R1}{R2}\right) \times V_{IT+} \quad (2)$$

Where:

- R1 and R2 are the resistor values for the resistor divider on the SENSEx pins.
- $V_{MON(UV)}$ is the target voltage at which an undervoltage condition is detected.
- $V_{MON(no\ UV)}$ is the target voltage at which an undervoltage condition is removed when V_{MON} rises.

Choose RTOTAL (= R1 + R2) so that the current through the divider is approximately 100 times higher than the input current at the SENSEx pins. The resistors can have high values to minimize current consumption as a result of low input bias current without adding significant error to the resistive divider. For details on sizing input resistors, refer to Application Report SLVA450, *Optimizing Resistor Dividers at a Comparator Input*, available for download from www.ti.com.

OUTPUTS (OUT1, OUT2)

In a typical device application, the outputs are connected to a reset or enable input of the processor, such as a digital signal processor (DSP), central processing unit (CPU), field-programmable gate array (FPGA), or application-specific integrated circuit (ASIC); or the outputs are connected to the enable input of a voltage regulator, such as a dc-dc or low-dropout (LDO) regulator.

The TPS3779 provides two push-pull outputs. The logic high level of the outputs is determined by the VCC pin voltage. With this configuration, pull-up resistors are not required and some board area can be saved. However, all interface logic levels should be examined. All OUT connections must be compatible with the VCC pin logic level.

The TPS3780 provides two open-drain outputs (OUT1 and OUT2); pull-up resistors must be used to hold these lines high when the output goes to a high impedance condition (not asserted). By connecting pull-up resistors to the proper voltage rails, the outputs can be connected to other devices at correct interface voltage levels. The outputs can be pulled up to 6.5 V, independent of the device supply voltage. To ensure proper voltage levels, make sure to choose the correct pull-up resistor values. The pull-up resistor value is determined by V_{OL}, the sink current capability, and the output leakage current ($I_{lkg(OD)}$). These values are specified in the Electrical Characteristics table. By using wired-AND logic, OUT1 and OUT2 can be merged into one logic signal. The *Inputs (SENSE1, SENSE2)* section describes how the outputs are asserted or deasserted. Refer to Figure 13 for a description of the relationship between threshold voltages and the respective output.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from the page numbers in the current version.

Changes from Revision A (March 2013) to Revision B	Page
• Changed V_{IT-} parameter in Electrical Characteristics table	3

Changes from Original (September 2012) to Revision A	Page
• Changed data sheet from product preview to production data	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS3779ADRYR	PREVIEW	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZQ	
TPS3779ADRYT	PREVIEW	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZQ	
TPS3779BDRYR	PREVIEW	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZR	
TPS3779BDRYT	PREVIEW	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZR	
TPS3779CDRYR	PREVIEW	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZT	
TPS3779CDRYT	PREVIEW	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZT	
TPS3779DDRYR	PREVIEW	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZS	
TPS3779DDRYT	PREVIEW	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZS	
TPS3780ADRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZU	Samples
TPS3780ADRYT	ACTIVE	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZU	Samples
TPS3780BDRYR	PREVIEW	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZV	
TPS3780BDRYT	PREVIEW	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZV	
TPS3780CDRYR	PREVIEW	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZW	
TPS3780CDRYT	PREVIEW	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZW	
TPS3780DDRYR	PREVIEW	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZX	
TPS3780DDRYT	PREVIEW	SON	DRY	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZX	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

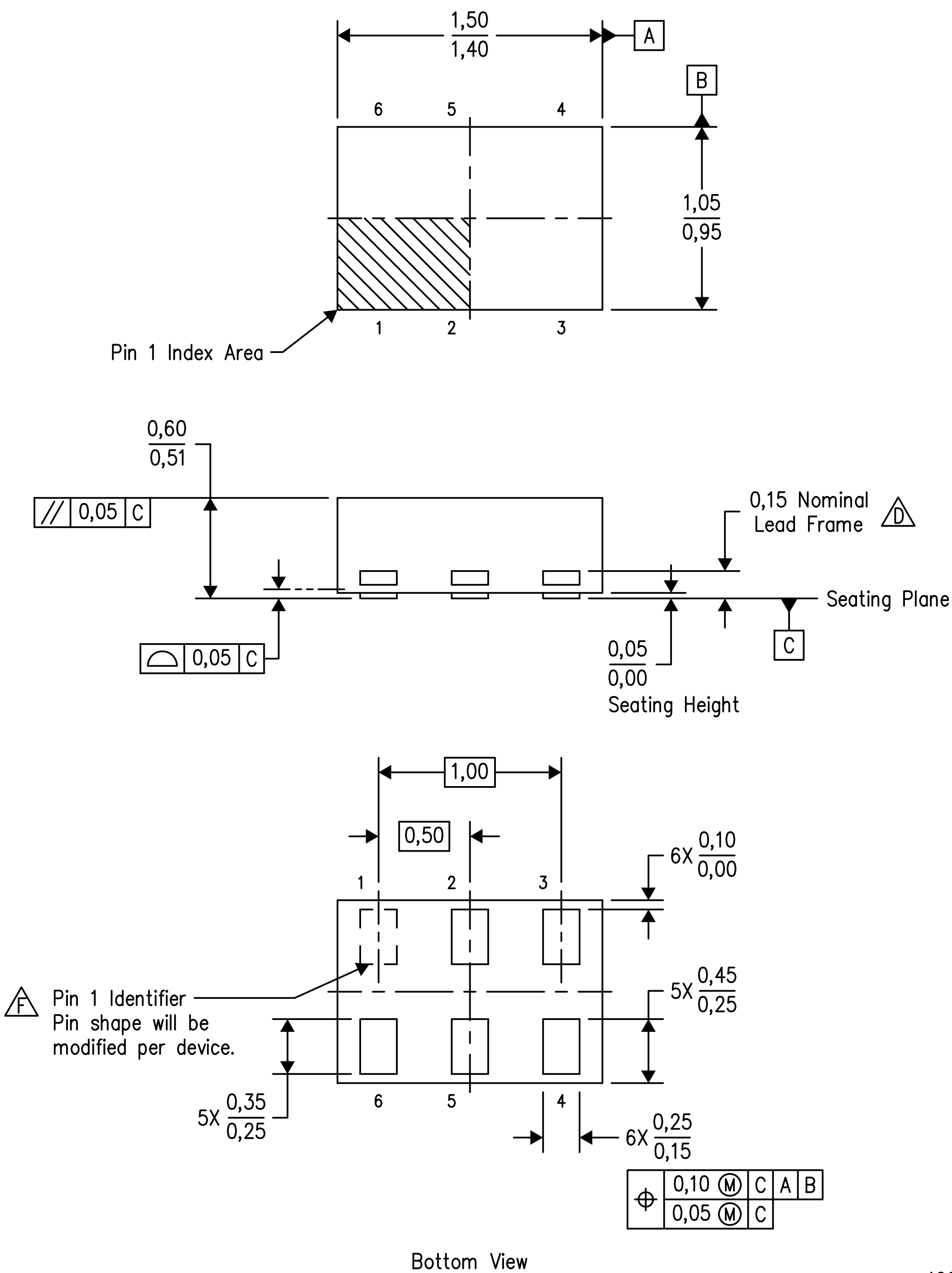
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

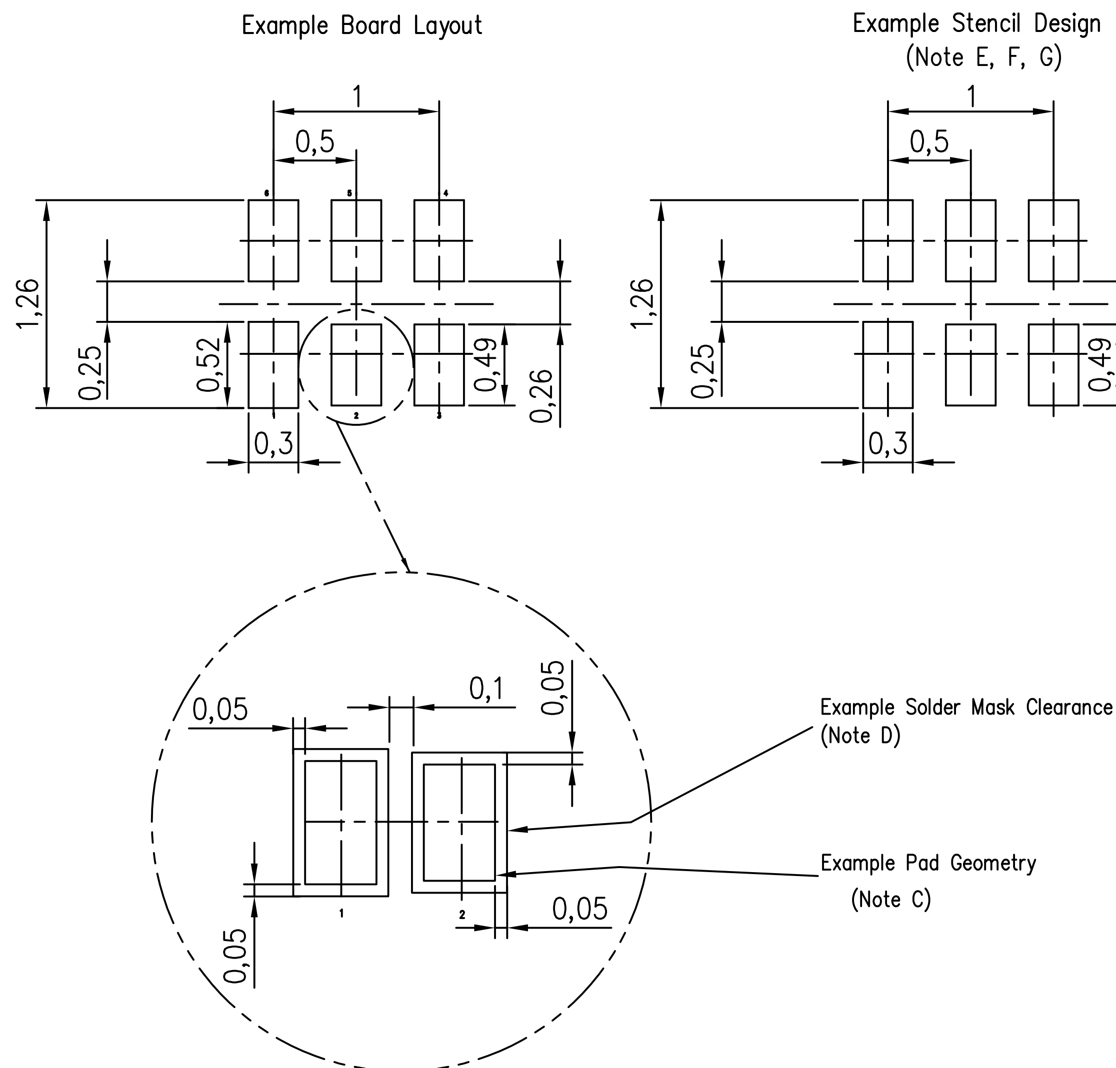


4207181/F 12/11

NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
E. This package complies to JEDEC MO–287 variation UFAD.
F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4208310/E 02/13

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

IMPORTANT NOTICE

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265