

Capacitor-Free, Dual, 150-mA, Low-Dropout Regulator in 1,2-mm x 1,2-mm SON Package

FEATURES

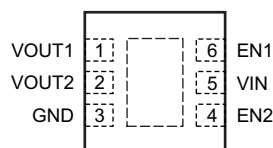
- **Stable With or Without Output Capacitors⁽¹⁾**
- **Accuracy: 1%**
- **Input Voltage Range: 1.4 V to 5.5 V**
- **Multiple Fixed Output Voltage Combinations Possible from 1.0 V to 3.3 V**
- **Foldback Overcurrent Protection**
- **Dedicated V_{REF} for Each Output Minimizes Crosstalk**
- **Package: 1,2-mm x 1,2-mm SON-6 (DPQ)**

⁽¹⁾ See the *Input and Output Capacitor Requirements* section in the *Application Information*.

APPLICATIONS

- **Wireless Handsets, Smart Phones, PDAs**
- **Portable Battery-Powered Products**

DPQ PACKAGE⁽¹⁾
1.2-mm x 1.2-mm SON
(TOP VIEW)



⁽¹⁾ The thermal pad is GND.

DESCRIPTION

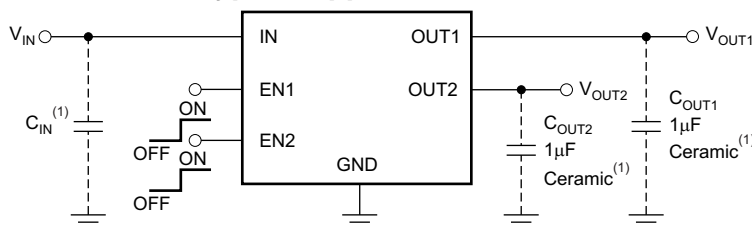
The TLV716 is a series of dual-channel, 150-mA, low-dropout (LDO) linear regulators with multiple fixed output options available from 1.0 V to 3.3 V. These devices provide a typical accuracy of 1% over temperature.

The TLV716 series is designed to be stable without an output capacitor. The removal of the output capacitor allows for very small solution size. However, the TLV716 series is also stable with a ceramic output capacitor if an output capacitor is used. The TLV716P series provides an active pull-down circuit to quickly discharge the outputs.

In addition, the TLV716 also provides inrush current control during device power-up and enabling. The TLV716 limits the input current to the defined current limit to avoid large currents from flowing from the input power source. This functionality is especially important in battery-operated devices.

The TLV716 series is available in a 1.2-mm x 1.2-mm SON-6 package and is ideal for handheld applications.

Typical Application Circuit



⁽¹⁾ Optional.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION⁽¹⁾

PRODUCT	V _{OUT} ⁽²⁾
TLV716XX(X)YY(Y)PWWWZ	<p>XX(X) is the nominal output voltage of channel 1. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 18 = 1.8 V; 185 = 1.85 V).</p> <p>YY is the nominal output voltage of channel 2. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 18 = 1.8 V; 185 = 1.85 V).</p> <p>P is optional. Use <i>P</i> for devices with an active output discharge.</p> <p>WWW is the package designator.</p> <p>Z is the package quantity. Use <i>R</i> for reel (3000 pieces), and <i>T</i> for tape (250 pieces).</p>

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
- (2) Output voltages from 1.2 V to 3.3 V in 50-mV increments are available through the use of innovative factory OTP programming; minimum order quantities may apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

At T_J = –40°C to +125°C, unless otherwise noted.

		VALUE		UNIT
		MIN	MAX	
Voltage ⁽²⁾	IN	–0.3	+6.0	V
	EN	–0.3	V _{IN} + 0.3	V
	OUT	–0.3	+3.6	V
Current	OUT	Internally limited		A
Output short-circuit duration		Indefinite		s
Temperature	Operating junction, T _J	–55	+150	°C
	Storage, T _{stg}	–55	+150	°C
Electrostatic discharge (ESD) rating	Human body model (HBM) QSS 009-105 (JESD22-A114A)	2		kV
	Charged device model (CDM) QSS 009-147 (JESD22-C101B.01)	500		V

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground.

THERMAL INFORMATION⁽¹⁾

THERMAL METRIC ⁽²⁾⁽¹⁾		TLV716, TLV716P	UNITS
		DPQ (SON)	
		6 PINS	
θ _{JA}	Junction-to-ambient thermal resistance	149.3	°C/W
θ _{JCtop}	Junction-to-case (top) thermal resistance	93.0	
θ _{JB}	Junction-to-board thermal resistance	110.1	
ψ _{JT}	Junction-to-top characterization parameter	3.4	
ψ _{JB}	Junction-to-board characterization parameter	114.9	
θ _{JCbot}	Junction-to-case (bottom) thermal resistance	91.0	

- (1) See the [Power Dissipation](#) section for more details.
- (2) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

ELECTRICAL CHARACTERISTICS

At $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $T_J = +25^\circ\text{C}$, $V_{IN} = V_{OUT(TYP)} + 0.5\text{ V}$ or 2.0 V (whichever is greater), $I_{OUT} = 1\text{ mA}$, $V_{EN1} = V_{EN2} = 0.9\text{ V}$, and $C_{OUT1} = C_{OUT2} = 0.47\text{ }\mu\text{F}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
V_{IN}	Input voltage range	1.4		5.5	V		
V_{OUT}	Output voltage accuracy	$T_J = +25^\circ\text{C}$, $V_{OUT} > 1.2\text{ V}$	-1		1	%	
		$T_J = +25^\circ\text{C}$, $V_{OUT} < 1.2\text{ V}$	-20		20	mV	
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{OUT} > 1.2\text{ V}$	-1.5		1.5	%	
		$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{OUT} < 1.2\text{ V}$	-50		50	mV	
I_{OUT}	Output current	Each channel			150	mA	
ΔV_{OUT}	Line regulation	$V_{OUT} + 0.5\text{ V} < V_{IN} < 5.0\text{ V}$			0.2	5	mV
ΔV_{OUT1}	Load regulation	$0.5\text{ mA} < I_{OUT} < 150\text{ mA}$			10	30	mV
ΔV_{OUT1}	Cross load regulation	$1\text{ mA} < I_{OUT} < 150\text{ mA}$			0.3	10	mV
V_{DO}	Dropout voltage	$I_{OUT} = 150\text{ mA}$, $1.0\text{ V} < V_{OUT} < 1.2\text{ V}$			0.78	TBD	V
		$I_{OUT} = 150\text{ mA}$, $1.2\text{ V} < V_{OUT} < 1.8\text{ V}$			0.6	0.9	V
		$I_{OUT} = 150\text{ mA}$, $1.8\text{ V} < V_{OUT} < 2.1\text{ V}$			0.35	0.575	V
		$I_{OUT} = 150\text{ mA}$, $2.1\text{ V} < V_{OUT} < 2.5\text{ V}$			0.29	0.48	V
		$I_{OUT} = 150\text{ mA}$, $2.5\text{ V} < V_{OUT} < 3.0\text{ V}$			0.23	0.45	V
		$I_{OUT} = 150\text{ mA}$, $3.0\text{ V} < V_{OUT} < 3.3\text{ V}$			0.21	0.42	V
V_{HI}	Enable high voltage	0.9		V_{IN}	V		
V_{LO}	Enable low voltage	0		0.4	V		
R_{PD}	Output pull-down resistance (optional)		120		Ω		
I_{CL}	Output current limit	$V_{EN1} = V_{EN2} = V_{IN}$			200	mA	
I_{SC}	Output short current limit	$V_{OUT} = 0\text{ V}$			40	mA	
I_{GND}	Ground pin current	$I_{OUT} = 0\text{ mA}$, per channel			50	75	μA
$I_{SHUTDOWN}$	Shutdown current	$EN = 0\text{ V}$, per channel, $V_{IN} = 5.5\text{ V}$, $T_A = +25^\circ\text{C}$			0.1	1	μA
PSRR	Power-supply rejection ratio	$f = 100\text{ Hz}$, $V_{OUT} = 3.3\text{ V}$, $I_{OUT} = 30\text{ mA}$			70		dB
		$f = 10\text{ kHz}$, $V_{OUT} = 3.3\text{ V}$, $I_{OUT} = 30\text{ mA}$			55		dB
V_N	Output noise voltage	BW = 10 Hz to 100 kHz, $V_{OUT} = 1.8\text{ V}$, $V_{IN} = 2.3\text{ V}$, $I_{OUT} = 10\text{ mA}$			70		μV_{RMS}
t_{STR}	Startup time ⁽¹⁾	$I_{OUT} = 150\text{ mA}$, $C_{OUT} = 1\text{ }\mu\text{F}$			100		μs
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing			+158		$^\circ\text{C}$
		Reset, temperature decreasing			+140		$^\circ\text{C}$
T_J	Operating junction temperature	-40		+125		$^\circ\text{C}$	

(1) Startup time = time from EN assertion to $0.98 \times V_{OUT(NOM)}$.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV7162818PDPQR	PREVIEW	X2SON	DPQ	6	3000	TBD	Call TI	Call TI	-40 to 125		
TLV7162818PDPQT	PREVIEW	X2SON	DPQ	6	250	TBD	Call TI	Call TI	-40 to 125		
TLV7162828PDPQR	PREVIEW	X2SON	DPQ	6	3000	TBD	Call TI	Call TI	-40 to 125		
TLV7162828PDPQT	PREVIEW	X2SON	DPQ	6	250	TBD	Call TI	Call TI	-40 to 125		
TLV7163030PDPQR	PREVIEW	X2SON	DPQ	6	3000	TBD	Call TI	Call TI	-40 to 125		
TLV7163030PDPQT	PREVIEW	X2SON	DPQ	6	250	TBD	Call TI	Call TI	-40 to 125		
TLV7163318PDPQR	PREVIEW	X2SON	DPQ	6	3000	TBD	Call TI	Call TI	-40 to 125		
TLV7163318PDPQT	PREVIEW	X2SON	DPQ	6	250	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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