3-Channel, 8-Bit, PWM LED Driver with Single-Wire Interface (EasySet™)

Check for Samples: TLC59731

FEATURES

- **Three Sink Current Channels**
- **Current Capability:**
  - **50 mA per Channel**
- **Grayscale (GS) Control with PWM:**
  - **8-Bit (256 Steps) with Simple Gamma Correction**
- **Single-Wire Interface (EasySet)**
- **Power-Supply (VCC) Voltage Range:**
  - **No Internal Shunt Regulator Mode: 3 V to 5.5 V**
  - **Internal Shunt Regulator Mode: 3 V to 6 V**
- **OUT Terminals Maximum Voltage: Up to 21 V**
- **Integrated Shunt Regulator**
- **Data Transfer Maximum Rate:**
  - **Bits per Second (bps): 600 kbps**
- **Internal GS Clock Oscillator: 6 MHz (typ)**
- **Display Repeat Rate: 3.1 kHz (typ)**
- **Output Delay Switching to Prevent Inrush Current**
- **Unlimited Device Cascading**
- **Operating Temperature: –40°C to +85°C**

APPLICATIONS

- **RGB LED Cluster Lamp Display**

DESCRIPTION

The TLC59731 is an easy-to-use, 3-channel, 50-mA sink current LED driver. The single-wire, 600-kbps serial interface (EasySet) provides a solution for minimizing wiring cost. The LED driver provides 8-bit pulse width modulation (PWM) resolution and a simple gamma correction feature. The display repeat rate is achieved at 3.1 kHz (typ) with an integrated 6-MHz grayscale (GS) clock oscillator. The driver also provides unlimited cascading capability.

Output sink current can be set by each external resistor connected to the OUT*n* terminal in series. The TLC59731 has an internal shunt regulator that can be used for higher VCC power-supply voltage applications.

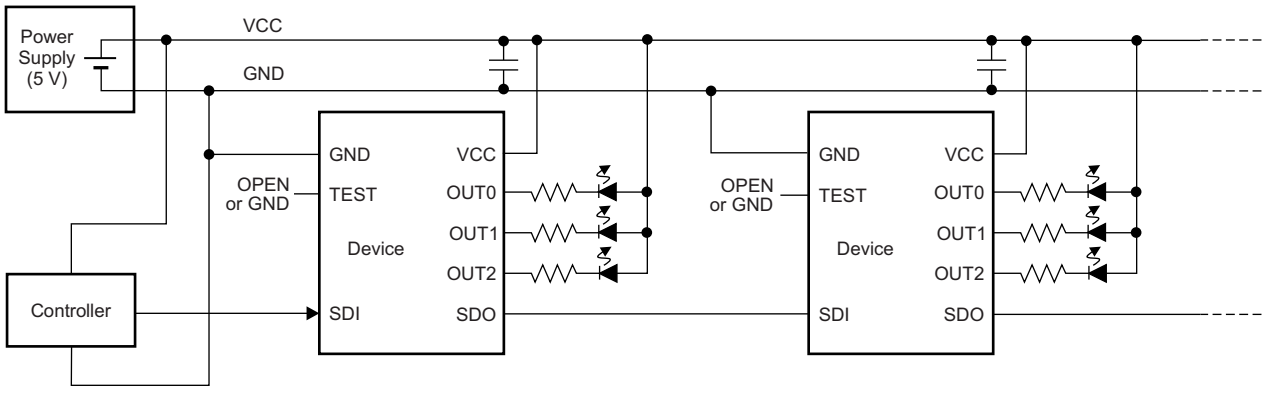


Figure 1. Typical Application Circuit Example 1 (No Internal Shunt Regulator Mode)

DESCRIPTION (CONTINUED)

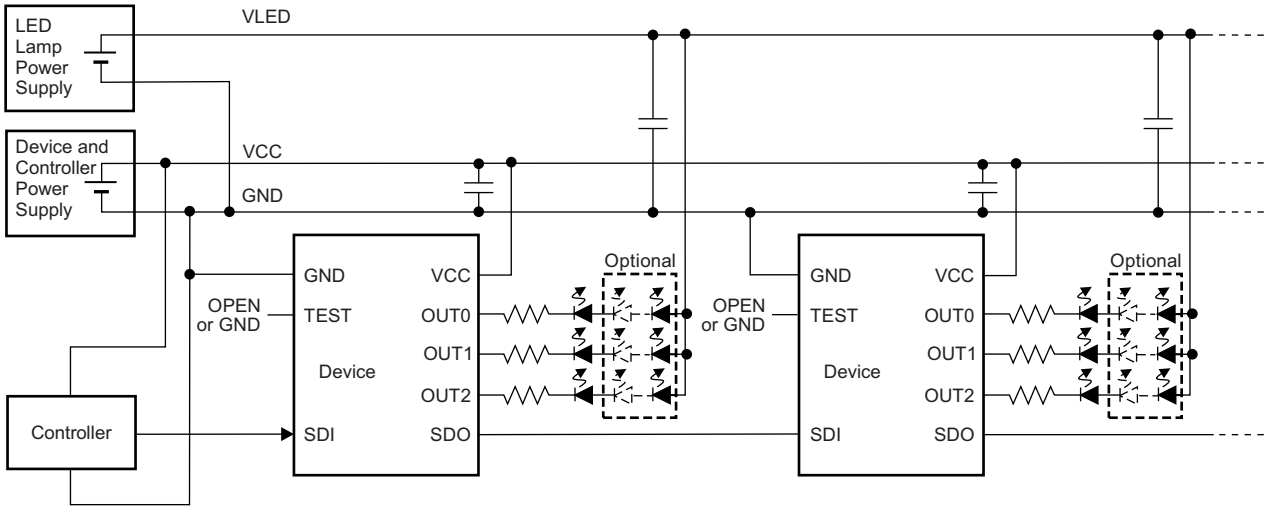


Figure 2. Typical Application Circuit Example 2 (No Internal Shunt Regulator Mode)

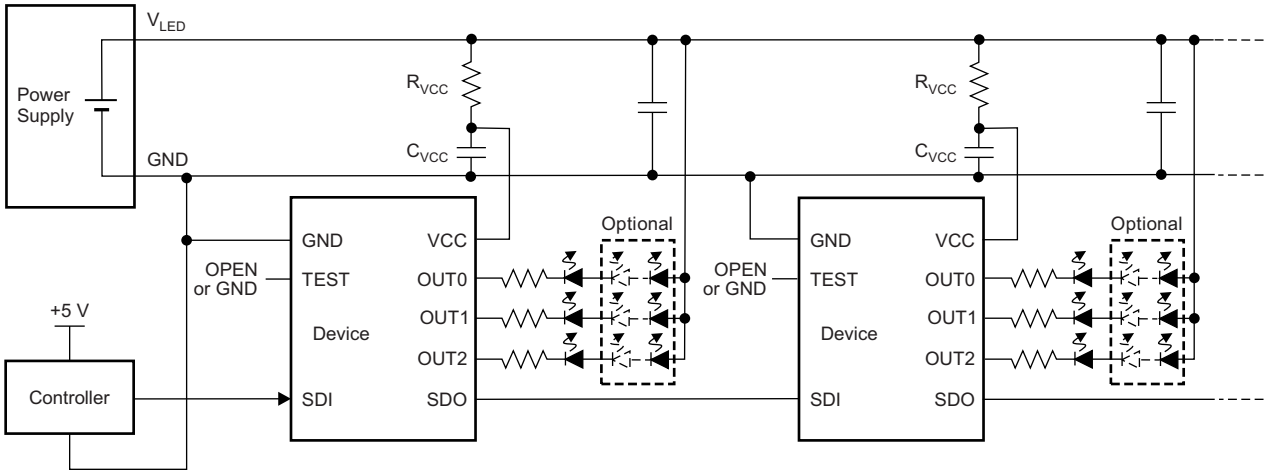


Figure 3. Typical Application Circuit Example 3 (Internal Shunt Regulator Mode)

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE AND ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TLC59731	SO-8	TLC59731DR	Tape and Reel, 2500
		TLC59731D	Tube, 75

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

			VALUE		UNIT
			MIN	MAX	
Voltage(2)	Supply, V_{CC}	VCC	–0.3	+7.0	V
	Input range, V_{IN}	SDI	–0.3	V_{CC} + 1.2	V
	Output range, V_{OUT}	OUT0 to OUT2	–0.3	+21	V
		SDO	–0.3	+7.0	V
Current	Output (dc), I_{OUT}	OUT0 to OUT2	0	+60	mA
Temperature	Operating junction, T_J		–40	+150	°C
	Storage, T_{stg}		–55	+150	°C
Electrostatic discharge (ESD) ratings:	Human body model (HBM)			8000	V
	Charged device model (CDM)			2000	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		TLC59731 D (SO) 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	134.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	88.6	
θ_{JB}	Junction-to-board thermal resistance	75.3	
ψ_{JT}	Junction-to-top characterization parameter	37.7	
ψ_{JB}	Junction-to-board characterization parameter	74.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
DC CHARACTERISTICS						
V_{CC}	Supply voltage	No internal shunt regulator mode	3.0	5.0	5.5	V
		Internal shunt regulator mode			6.0	V
V_O	Voltage applied to output	OUT0 to OUT2			21	V
V_{IH}	High-level input voltage	SDI	0.7 × V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage	SDI	GND		0.3 × V_{CC}	V
V_{IHYST}	Input voltage hysteresis	SDI		0.2 × V_{CC}		V
I_{OH}	High-level output current	SDO			–2	mA
I_{OL}	Low-level output current	SDO			2	mA
		OUT0 to OUT2			50	mA
I_{REG}	Shunt regulator sink current	VCC			20	mA
T_A	Operating free-air temperature range		–40		+85	°C
T_J	Operating junction temperature range		–40		+125	°C
AC CHARACTERISTICS						
$f_{CLK\ (SDI)}$	Data transfer rate	SDI	20		600	kHz
t_{SDI}	SDI input pulse duration	SDI	275		0.5 / f_{CLK}	ns
t_{WH}	Pulse duration, high	SDI	14			ns
t_{WL}	Pulse duration, low	SDI	14			ns
t_{H0}	Hold time: end of sequence (EOS)	SDI↑ to SDI↑	3.5 / f_{CLK}		5.5 / f_{CLK}	µs
t_{H1}	Hold time: data latch (GSLAT)	SDI↑ to SDI↑	8 / f_{CLK}			µs

ELECTRICAL CHARACTERISTICS

At T_A = –40°C to +85°C, V_{CC} = 3 V to 6.0 V, and C_{VCC} = 0.1 µF. Typical values at T_A = +25°C and V_{CC} = 5.0 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage (SDO)	I_{OH} = –2 mA		V_{CC} – 0.4		V_{CC}	V
V_{OL}	Low-level output voltage (SDO)	I_{OL} = 2 mA		0		0.4	V
V_R	Shunt regulator output voltage (V_{CC})	I_{CC} = 1 mA, SDI = low			5.9		V
I_{CC0}	Supply current (V_{CC})	V_{CC} = 3.0 V to 5.5 V, SDI = low, all grayscale (GS*n*) = FFh, V_{OUTn} = 0.6 V, SDO = 15 pF			2.3	3.5	mA
I_{CC1}		V_{CC} = 3.0 V to 5.5V , SDI = 600 kHz, GS*n* = FFh, V_{OUTn} = 0.6 V, SDO = 15 pF			2.6	4.5	mA
I_{OL}	LED output current (OUT0 to OUT2)	All OUT*n* = on, V_{OUTn} = 0.6 V		32	40		mA
I_{OLKG}	Output leakage current (OUT0 to OUT2)	GS*n* = 00h, V_{OUTn} = 21 V	T_J = –40°C to +85°C			0.1	µA
			T_J = +85°C to +125°C			0.2	µA
R_{PD}	Internal pull-down resistance (SDI)	At SDI			1		MΩ

SWITCHING CHARACTERISTICS

At T_A = –40°C to +85°C, V_{CC} = 3.0 V to 5.5 V, C_L = 15 pF, R_L = 110 Ω, and V_{LED} = 5.0 V, unless otherwise noted. Typical values are at T_A = +25°C and V_{CC} = 5.0 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{R0}	Rise time	SDO	2	6	12	ns
t_{R1}		OUT*n* (on → off)		200	400	ns
t_{F0}	Fall time	SDO	2	6	12	ns
t_{F1}		OUT*n* (off → on)		200	400	ns
t_{D0}	Propagation delay	SDI↑ to SDO↑		30	50	ns
t_{D1}		OUT0↓ to OUT1↓, OUT1↓to OUT2↓, OUT0↑ to OUT1↑, OUT1↑to OUT2↑		25		ns
t_{WO}	Shift data output one pulse duration	SDO↑ to SDO↓	75	125	250	ns
f_{OSC}	Internal GS oscillator frequency		4	6	8	MHz

PARAMETER MEASUREMENT INFORMATION

PIN-EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

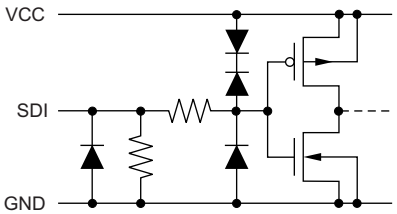


Figure 4. SDI

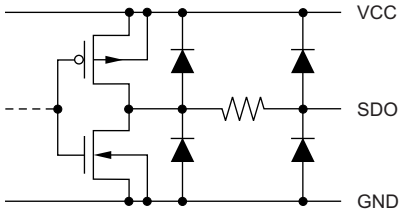
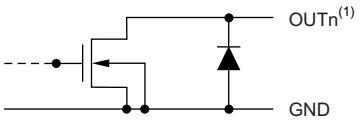


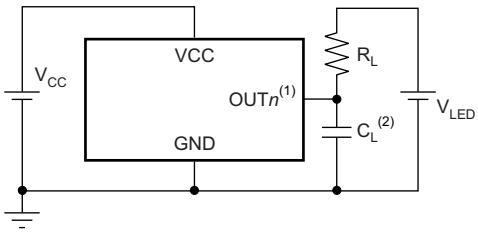
Figure 5. SDO



(1) n = 0 to 2.

Figure 6. OUT0 Through OUT2

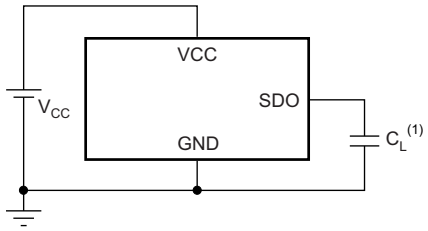
TEST CIRCUITS



(1) n = 0 to 2.

(2) C_L includes measurement probe and jig capacitance.

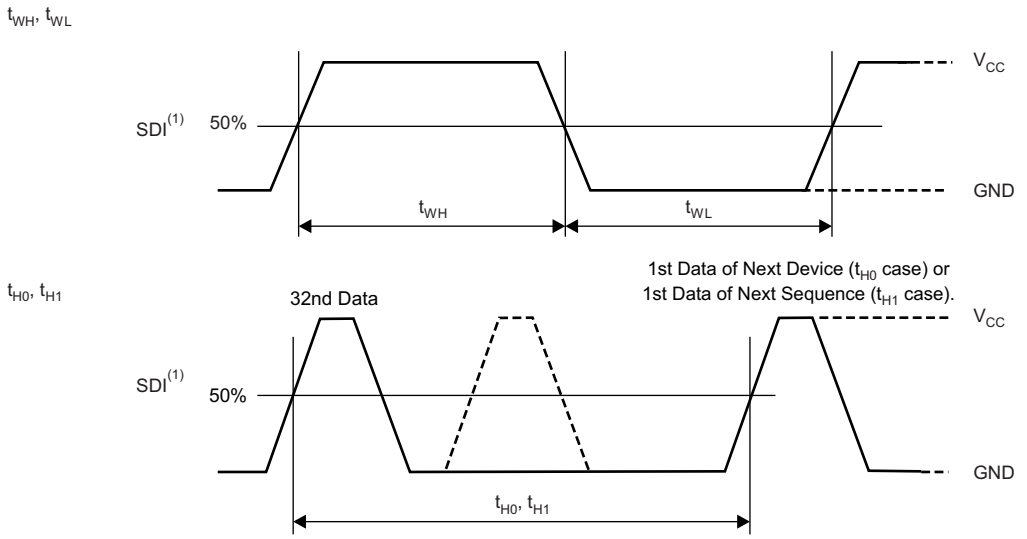
Figure 7. Rise Time and Fall Time Test Circuit for OUT*n*



(1) C_L includes measurement probe and jig capacitance.

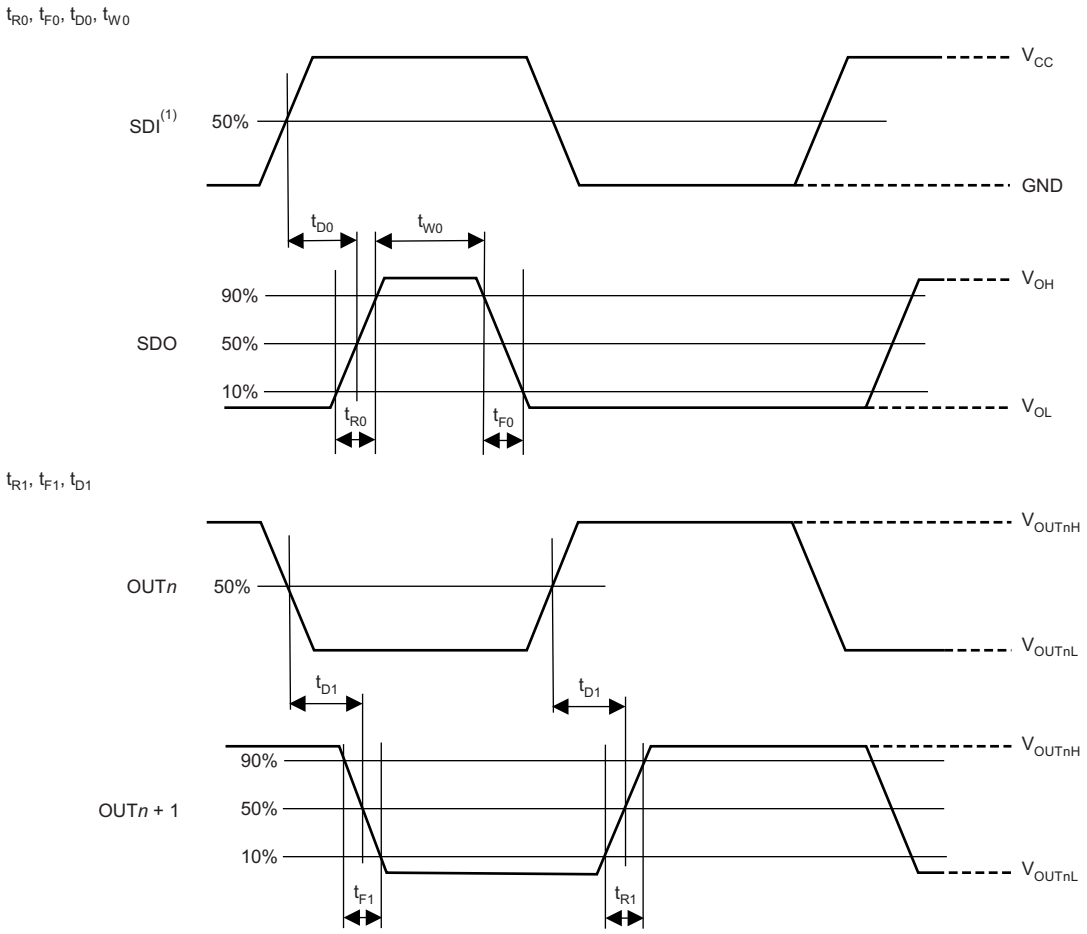
Figure 8. Rise Time and Fall Time Test Circuit for SDO

TIMING DIAGRAMS



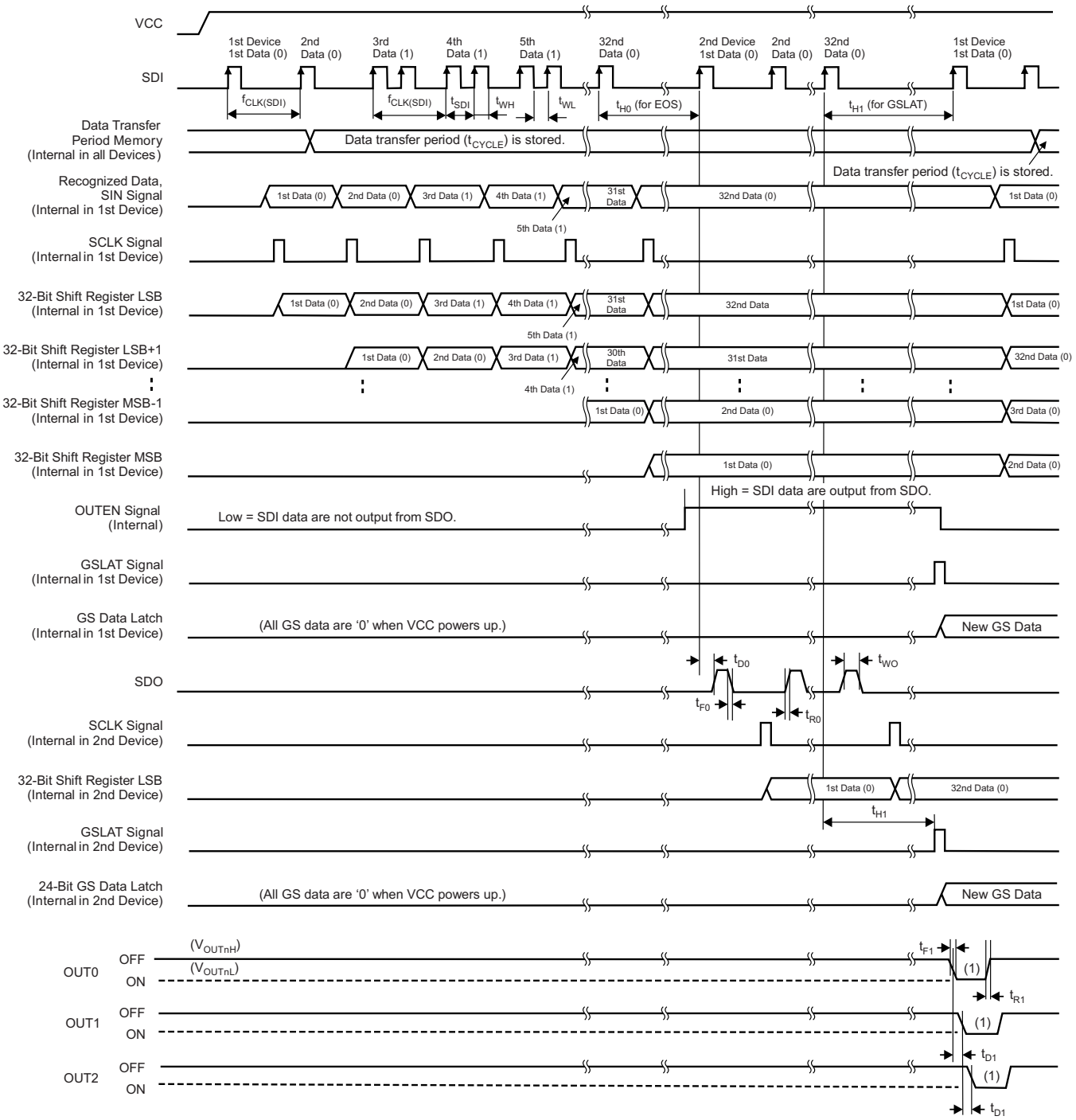
(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 9. Input Timing



(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 10. Output Timing

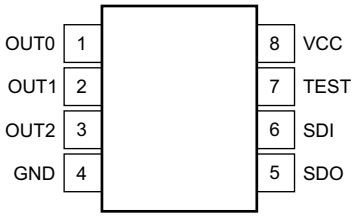


(1) OUT*n* on-time changes, depending on the data in the 24-bit GS data latch.

Figure 11. Data Write and OUT*n* Switching Timing

PIN CONFIGURATION

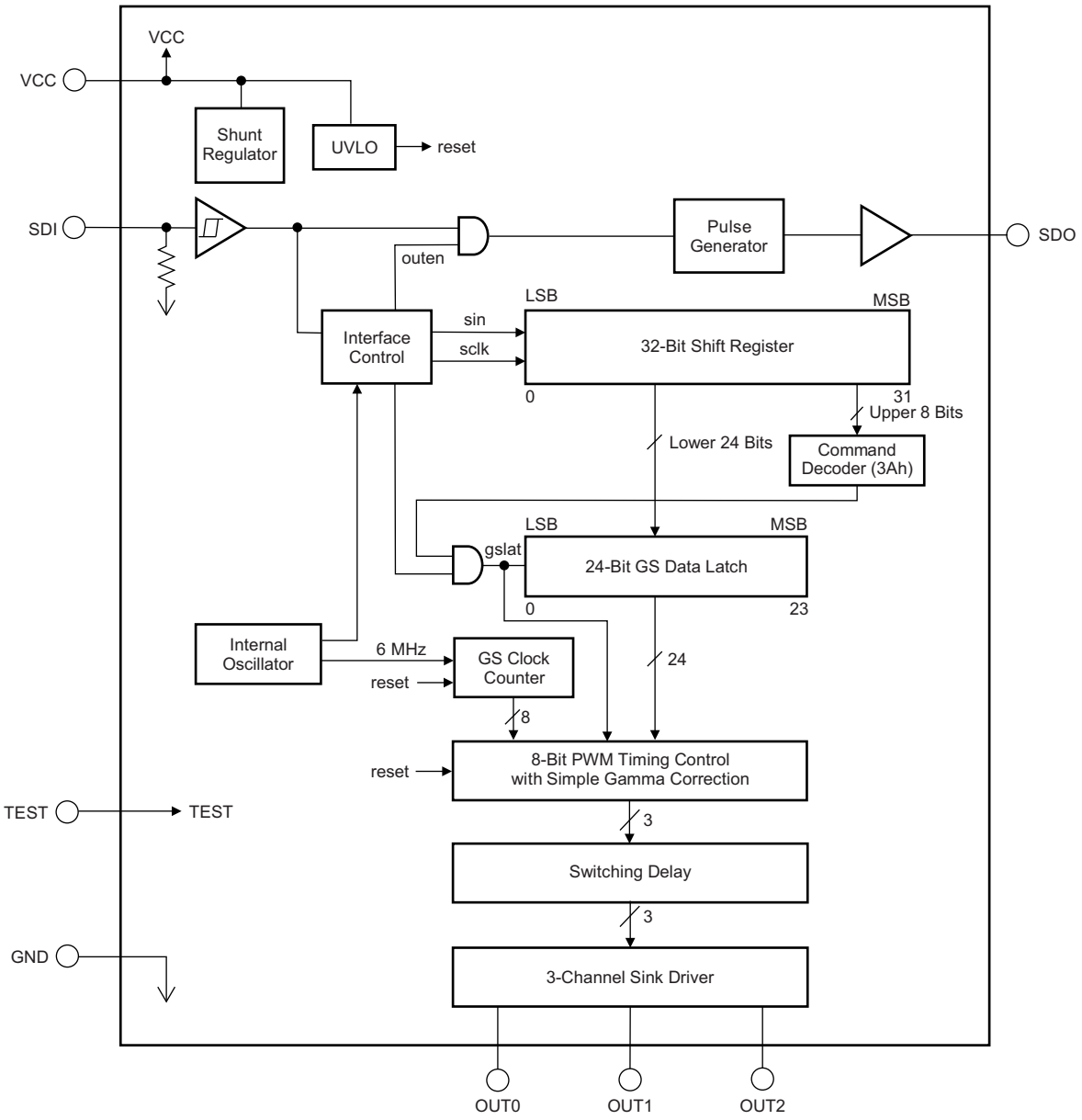
D PACKAGE
SO-8
(Top View)



PIN DESCRIPTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	4	—	Power ground
OUT0	1	O	Sink driver outputs. Multiple outputs can be configured in parallel to increase the sink drive current capability. Different voltages can be applied to each output.
OUT1	2	O	
OUT2	3	O	
SDI	6	I	Serial data input. This pin is internally pulled down to GND with a 1-MΩ (typ) resistor.
SDO	5	O	Serial data output
TEST	7	—	TI internal test terminal. This pin must be connected to GND or left open.
VCC	8	—	Power-supply voltage

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

At T_A = +25°C and V_{CC} = 12 V, unless otherwise noted.

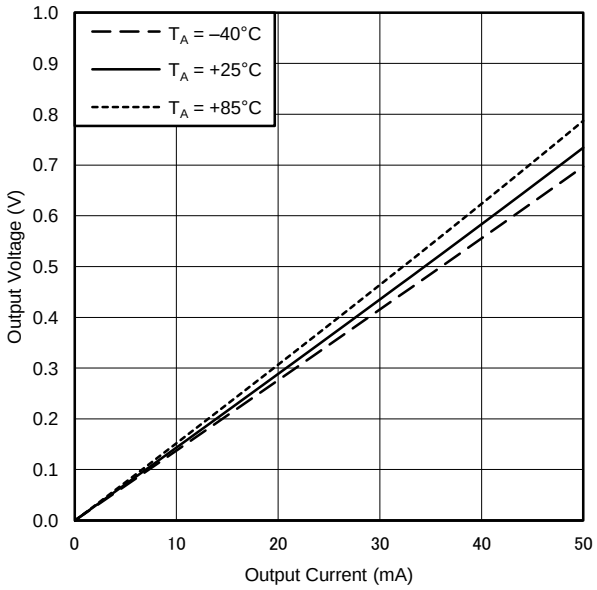


Figure 12. OUTPUT CURRENT vs OUTPUT VOLTAGE (OUT*n*)

DETAILED DESCRIPTION

SINK CURRENT VALUE SETTING

The typical sink current value of each channel (I_{OUTn}) can be set by resistor (R_{Ln}) that is placed between the LED cathode and OUT*n* pins, as shown in Figure 13. The typical sink current value can be calculated by Equation 1 and the typical resistor value can be calculated by Equation 2.

$$I_{OUTn}\,(mA) = \frac{V_{LED}\,(V) - V_{F\_TOTAL}\,(V) - V_{OUTn}\,(V)}{R_{Ln}\,(\Omega)}$$

NOTE: n = 0 to 2. (1)

$$R_{Ln}\,(\Omega) = \frac{V_{LED}\,(V) - V_{F\_TOTAL}\,(V) - V_{OUTn}\,(V)}{I_{OUTn}\,(mA)}$$

NOTE: n = 0 to 2. (2)

Where:

V_{LED} = the LED anode voltage, V_{F_TOTAL} = the total LED forward voltage, and V_{OUTn} = the OUT*n* output voltage. Note that the typical V_{OUTn} value is 0.6 V with a 40-mA output current; see Figure 12.

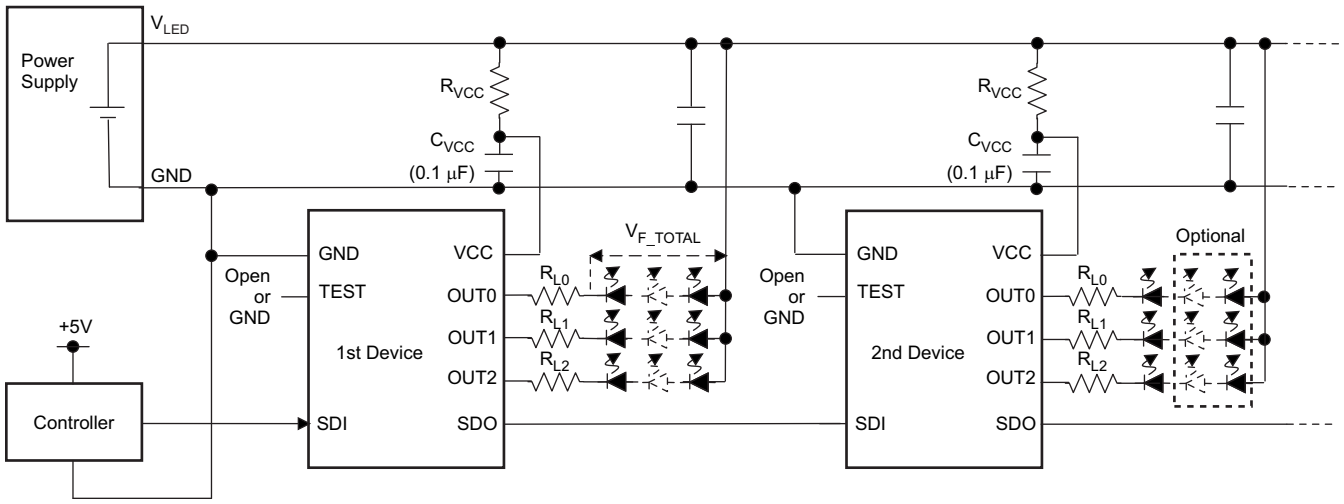


Figure 13. Internal Shunt Regulator Mode Application Circuit

RESISTOR AND CAPACITOR VALUE SETTING FOR SHUNT REGULATOR

The TLC59731 internally integrates a shunt regulator to regulate V_{CC} voltage. Refer to Figure 12 for an application circuit that uses the internal shunt regulator through a resistor, R_{VCC}. The recommended R_{VCC} value can be calculated by Equation 3.

$$\frac{V_{LED}\,(V) - 5.9\ V}{8\ mA} < R_{VCC} < \frac{V_{LED}\,(V) - 5.9\ V}{6\ mA} \quad (3)$$

Table 1 shows the typical resistor value for several V_{LED} voltages. Note that the C_{VCC} value should be 0.1 µF.

Table 1. Resistor Example for Shunt Resistor versus LED Voltage

V_{LED} (V)	R_{VCC} (Ω)	RESISTOR WATTAGE (W)
9	470	0.02
12	910	0.04
18	1800	0.08
24	2700	0.12

GRAYSCALE (GS) FUNCTION (PWM CONTROL)

The TLC59731 can adjust the brightness of each output channel using a pulse width modulation (PWM) control scheme. The PWM data bit length for each output is 8 bits. The architecture of 8 bits per channel results in 256 brightness steps, from 0% to 99.9% on-time duty cycle.

The PWM operation for OUT*n* is controlled by an 8-bit grayscale (GS) counter. The GS counter increments on each internal GS clock (GSCLK) rising edge. All OUT*n* turn on when the GS count is '1', except when OUT*n* are programed to GS data '0' in the 24-bit GS data latch. After turning on, each output is turns off when the GS counter value exceeds the programmed GS data for the output. The GS counter resets to 00h and all outputs are forced off when the GS data are written to the 24-bit GS data latch. Afterwards, the GS counter begins incrementing and PWM control is started from the next internal GS clock.

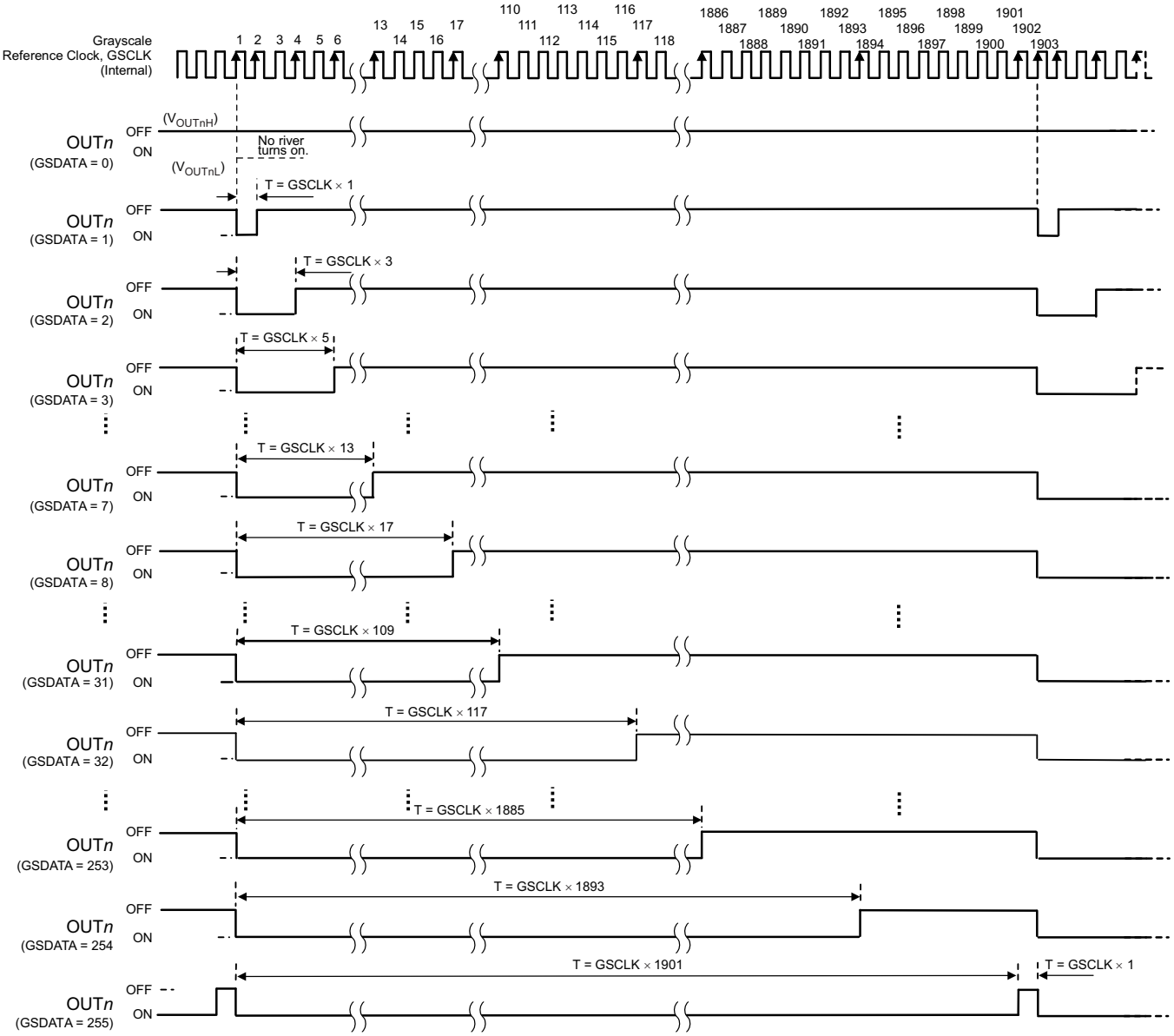
Table 2 summarizes the GS data values versus the output ideal on-time duty cycle. The on-time duty cycle is not proportional to the GS data because a simple gamma correction is implemented in the TLC59731. Furthermore, actual on-time differs from the ideal on-time because the output drivers and control circuit have some timing delay. When the device is powered on, all outputs are forced off and remain off until the non-zero GS data are written to the 24-bit GS data latch.

Table 2. Output Duty Cycle and Total On-Time versus GS Data

GS DATA		NO. OF GSCLKs OUT*n* TURNS ON	NO. OF GSCLKs OUT*n* TURNS OFF	TOTAL IDEAL TIME (µs)	ON-TIME DUTY (%)
DECIMAL	HEX				
0	0	Off	Off	0	0
1	1	1	2	0.2	0.1
2	2	1	4	0.5	0.2
3	3	1	6	0.8	0.3
—	—	—	—	—	—
6	6	1	12	1.8	0.6
7	7	1	14	2.2	0.7
8	8	1	18	2.8	0.9
9	9	1	22	3.5	1.1
10	10	1	26	4.2	1.3
—	—	—	—	—	—
30	1E	1	106	17.5	5.5
31	1F	1	110	18.2	5.7
32	20	1	118	19.5	6.2
33	21	1	126	20.8	6.6
34	22	1	134	22.2	7.0
—	—	—	—	—	—
62	3E	1	358	59.5	18.8
63	3F	1	366	60.8	19.2
64	40	1	374	62.2	19.6
65	41	1	382	63.5	20.0
66	42	1	390	64.8	20.5
—	—	—	—	—	—
127	7F	1	878	146.2	46.1
128	80	1	886	147.5	46.5
129	81	1	894	148.8	47.0
—	—	—	—	—	—
253	FD	1	1886	314.2	99.1
254	FE	1	1894	315.5	99.5
255	FF	1	1902	316.8	99.9

PWM Control

The GS counter keeps track of the number of grayscale reference clocks (GSCLKs) from the internal oscillator. Each output stays on while the counter is less than or equal to the programmed GS value. Each output turns off when the GS counter is greater than the GS value in the 24-bit GS data latch. Figure 14 illustrates the PWM operation timing.



(1) Actual on-time differs from the ideal on-time.

Figure 14. PWM Operation

REGISTER AND DATA LATCH CONFIGURATION

The TLC59731 has a 32-bit shift register and a 24-bit data latch that stores GS data. When the internal GS data latch pulse is generated and the data of the eight MSBs in the shift register are 3Ah, the lower 24-bit data in the 32-bit shift register are copied into the 24-bit GS data latch. If the data of the eight MSBs is not 3Ah, the 24-bit data are not copied into the 24-bit GS data latch. Figure 15 shows the shift register and GS data latch configurations. Table 3 shows the 32-bit shift register bit assignment.

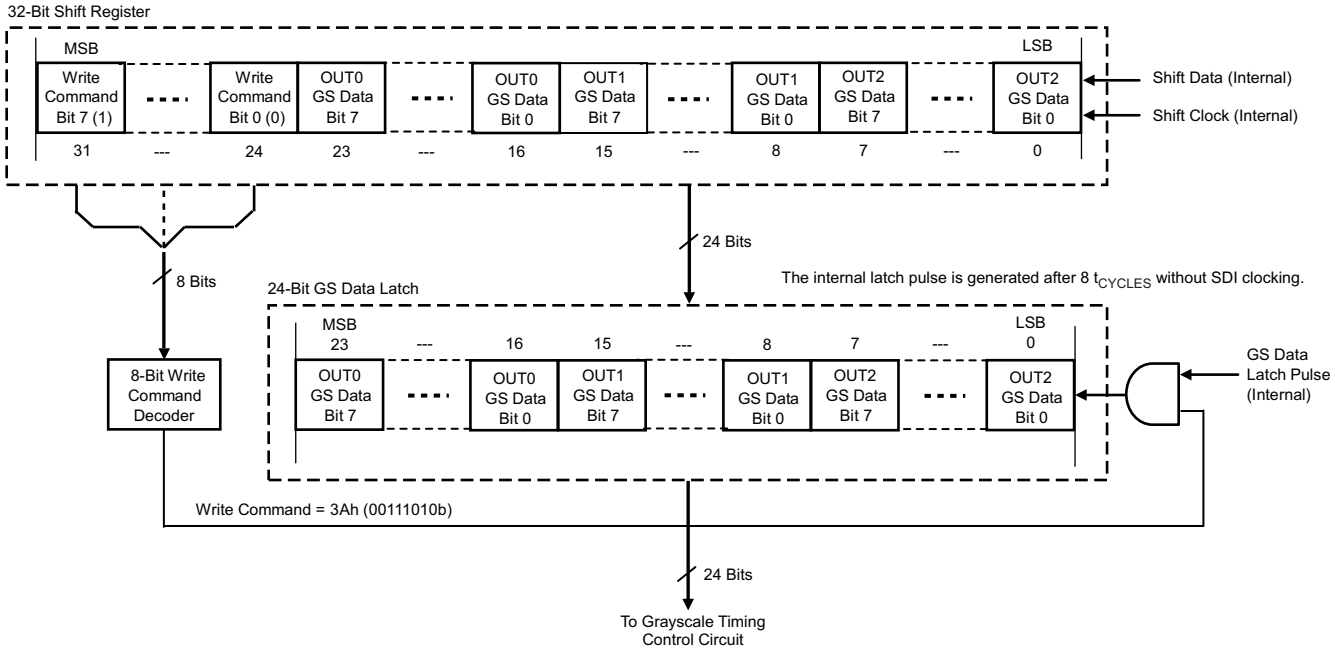


Figure 15. Common Shift Register and Control Data Latches Configuration

Table 3. 32-Bit Shift Register Data Bit Assignment

BITS	BIT NAME	CONTROLLED CHANNEL AND FUNCTIONS
0 to 7	GSOUT2	GS data bits 0 to 7 for OUT2
8 to 15	GSOUT1	GS data bits 0 to 7 for OUT1
16 to 23	GSOUT0	GS data bits 0 to 7 for OUT0
24 to 32	WRTCMD	Data write command (3Ah) for GS data. The lower 24-bit GS data in the 32-bit shift register are copied to the GS data latch when the internal GS latch is generated (when these data bits are 3Ah, *00111010b*).

ONE-WIRE INTERFACE (EasySet) DATA WRITING METHOD

There are four sequences to write GS data into the TLC59731 via a single-wire interface. This section discusses each sequence in detail.

Data Transfer Rate (t_{CYCLE}) Measurement Sequence

The TLC59731 measures the time between the first and second SDI rising edges either after the device is powered up or when the GS data latch sequence is executed (as described in the *GS Data Latch Sequence (GSLAT)* section) and the time is internally stored as t_{CYCLE}. t_{CYCLE} serves as a base time used to recognize one complete data write operation, a 32-bit data write operation, and a GS data write operation to the GS data latch. t_{CYCLE} can be set between 1.66 µs and 50 µs ($f_{CLK(SDI)}$ = 20 kHz to 600 kHz). In this sequence, two instances of data '0' are written to the LSB side of the 32-bit shift register. Figure 16 shows the t_{CYCLE} measurement timing.

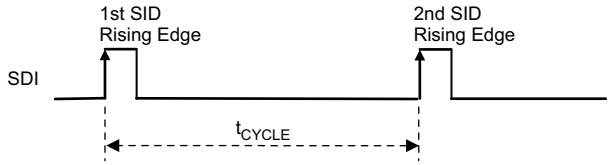


Figure 16. Data Transfer Rate (t_{CYCLE}) Measurement

Data '0' and Data '1' Write Sequence (Data Write Sequence)

When the second SDI rising edge is not input before 50% of t_{CYCLE} elapses from the first SDI rising edge input, the second rising edge is recognized as data '0'. When the second SDI rising edge is input before 50% of t_{CYCLE} elapses from the first SDI rising edge input, the second rising edge is recognized as data '1'. This write sequence must be repeated 30 times after the t_{CYCLE} measurement sequence in order to send the write command to the lower 6-bit (3Ah) and 24-bit GS data. Figure 17 shows the data '0' and '1' write timing.

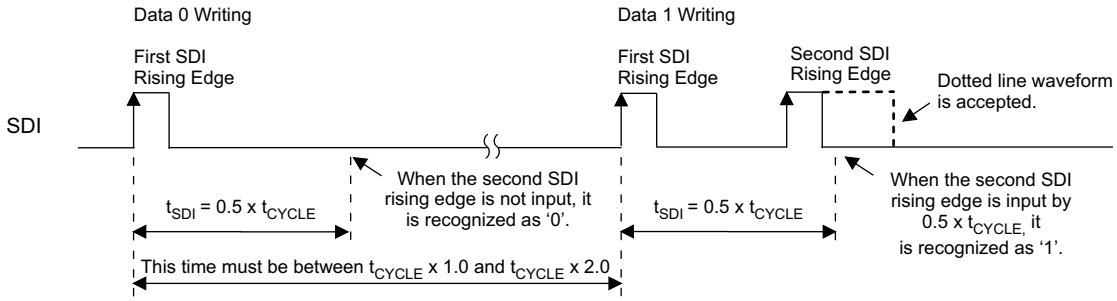


Figure 17. Data '0' and '1' Write Operation

One Communication Cycle End of Sequence (EOS)

One communication cycle end of sequence (EOS) must be input after the 32-bit data are written because the TLC59731 does not count the number of input data. When SDI is held low for the EOS hold time (t_{H0}), the 32-bit shift register values are locked and a buffered SDI signal is output from SDO to transfer GS data to the next device. Figure 18 shows the EOS timing.

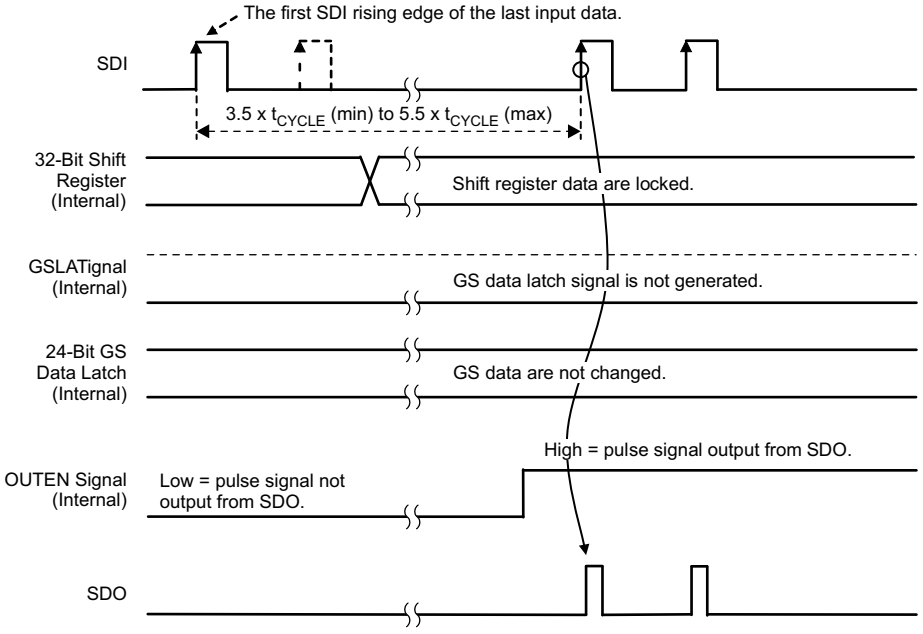


Figure 18. End of Sequence (EOS)

GS Data Latch (GSLAT) Sequence

A GS data latch (GSLAT) sequence must be input after the 32-bit data for all cascaded devices are written. When SDI is held low for the data latch hold time (t_{H1}), the 32-bit shift register data in all devices are copied to the GS data latch in each device. Furthermore, PWM control starts with the new GS data at the same time. Figure 19 shows the GSLAT timing.

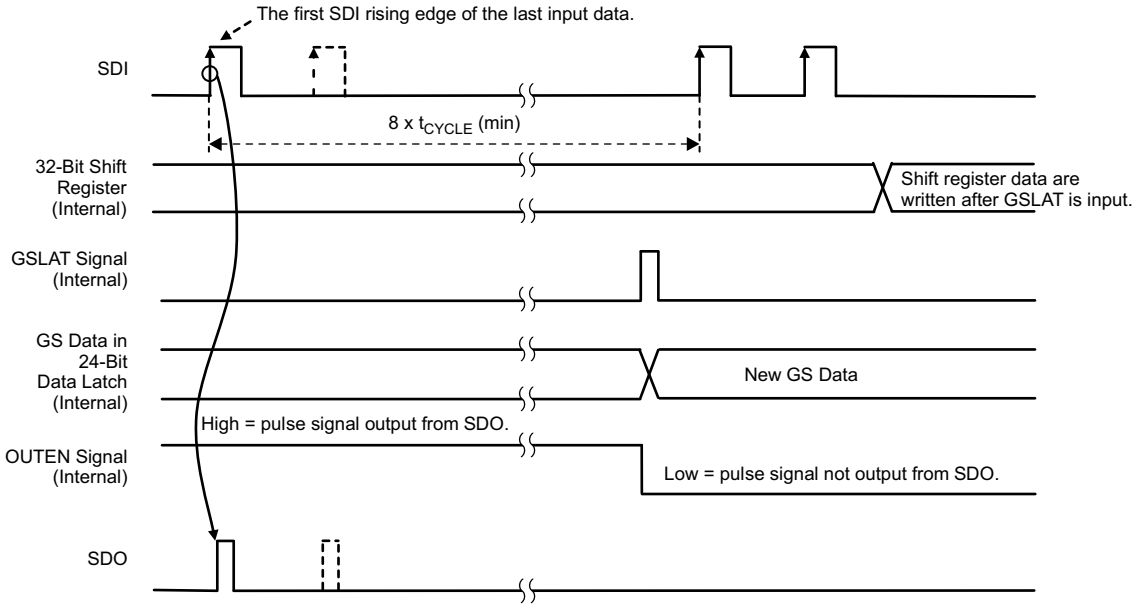


Figure 19. GS Data Latch Sequence (GSLAT)

HOW TO CONTROL DEVICES CONNECTED IN SERIES

The 8-bit write command and 24-bit grayscale (GS) data for OUT0 to OUT2 (for a total of 32 bits of data) must be written to the device.Figure 20 shows the 32-bit data packet configuration. When multiple devices are cascaded (as shown in Figure 21), *N* times the packet must be written into each TLC59731 in order to control all devices. There is no limit on how many devices can be cascaded, as long as proper VCC voltage is supplied. The packet for all devices must be written again whenever any GS data changes.

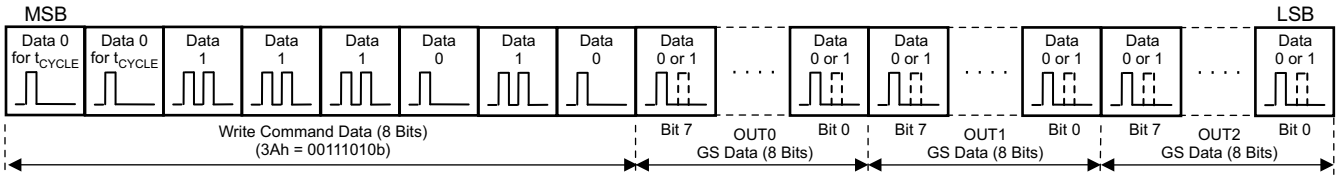


Figure 20. 32-Bit Data Packet Configuration for One TLC59731

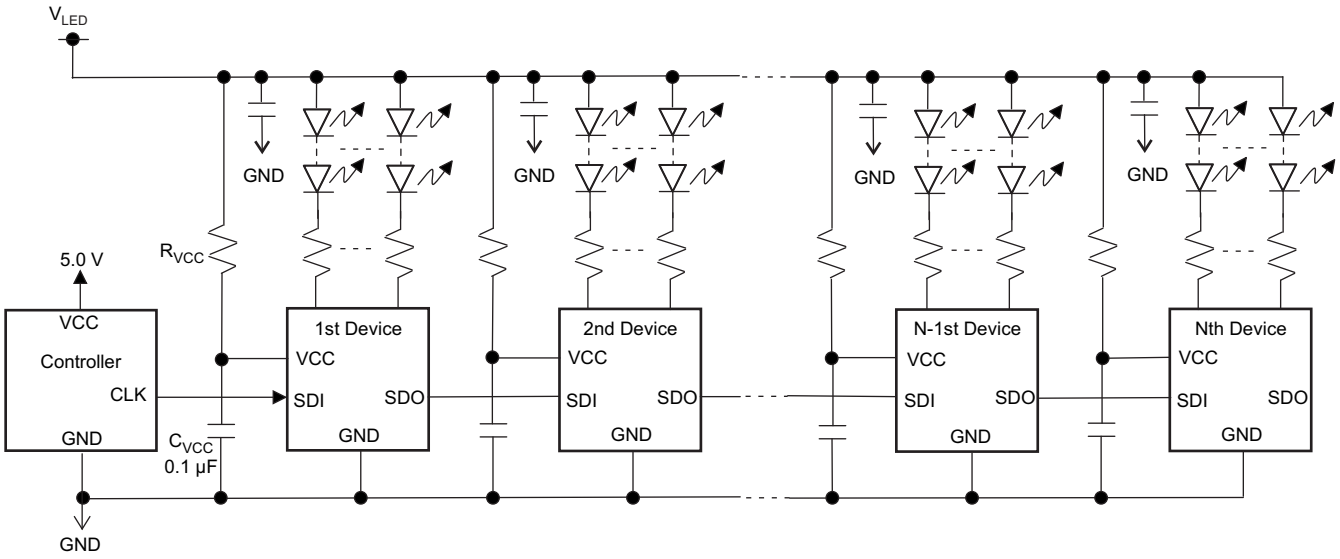


Figure 21. Cascade Connection of *N* TLC59731 Units (Internal Shunt Regulator Mode)

Refer to Figure 22 for the 32-bit data packet, EOS, and GSLAT input timing of all devices. The function setting write procedure and display control is as follows:

1. Power-up VCC (V_{LED}); all OUT*n* are off because GS data are not written yet.
2. Write the 32-bit data packet (MSB-first) for the first device using t_{CYCLE} and the data write sequences illustrated in Figure 16 and Figure 17. The first 8-bits of the 32-bit data packet are used as the write command. The write command must be 3Ah (00111010b); otherwise, the 24-bit GS data in the 32-bit shift register are not copied to the 24-bit GS data latch.
3. Execute one communication cycle EOS (refer to Figure 18) for the first device.
4. Write the 32-bit data packet for the second TLC59731 as described step 2. However, t_{CYCLE} should be set to the same timing as the first device.
5. Execute one communication cycle EOS for the second device.
6. Repeat steps 4 and 5 until all devices have GS data.
7. The number of total bits is 32 × *N*. After all data are written, execute a GSLAT sequence as described in Figure 19 in order to copy the 24-bit LSBs in the 32-bit shift resister to the 24-bit GS data latch in each device; PWM control starts with the written GS data at the same time.

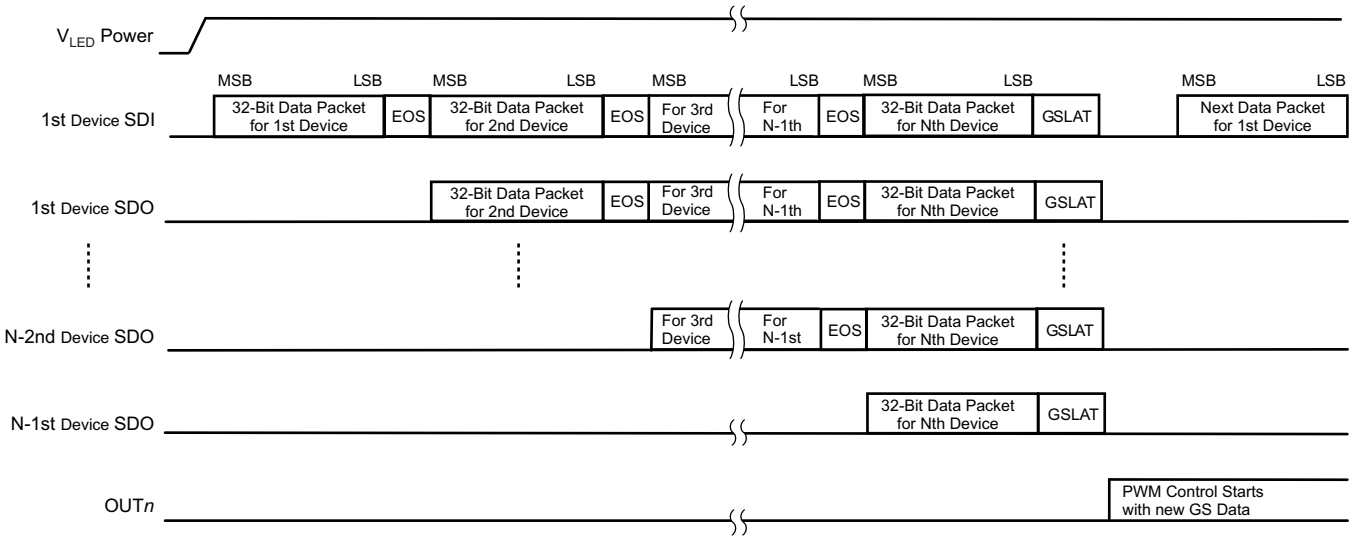


Figure 22. Data Packet Input Order for *N* TLC59731 Units

CONNECTOR DESIGN APPLICATION

When the connector pin of the device application printed circuit board (PCB) is connected or disconnected to other PCBs, the power must be turned off to avoid device malfunction or failure. Furthermore, designing the connector GND pin to be longer than other pins (as shown in Figure 23) is preferable. This arrangement allows the GND line to either be connected first or disconnected last, which is imperative for proper device function.

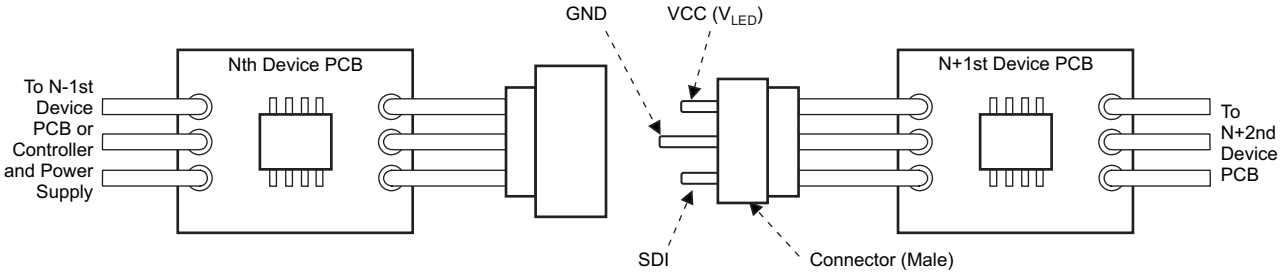


Figure 23. Connector Pin Design Application

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2013) to Revision A	Page
• Added EasySet trademark	1
• Changed bps value in Data Transfer Rate Features bullet	1
• Changed bps value in Description section	1
• Changed AC Characteristics, $f_{CLK\ (SDI)}$ parameter maximum specification in Recommended Operating Conditions table	4
• Changed I_{CC1} parameter test conditions in Electrical Characteristics table	5
• Changed second paragraph in *Grayscale (GS) Function (PWM Control)* section	13
• Updated Figure 15	15
• Updated Table 3	15
• Changed *Data Transfer Rate (t_{CYCLE}) Measurement Sequence* section	16
• Updated Figure 20	19

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLC59731D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	59731	Samples
TLC59731DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	59731	Samples

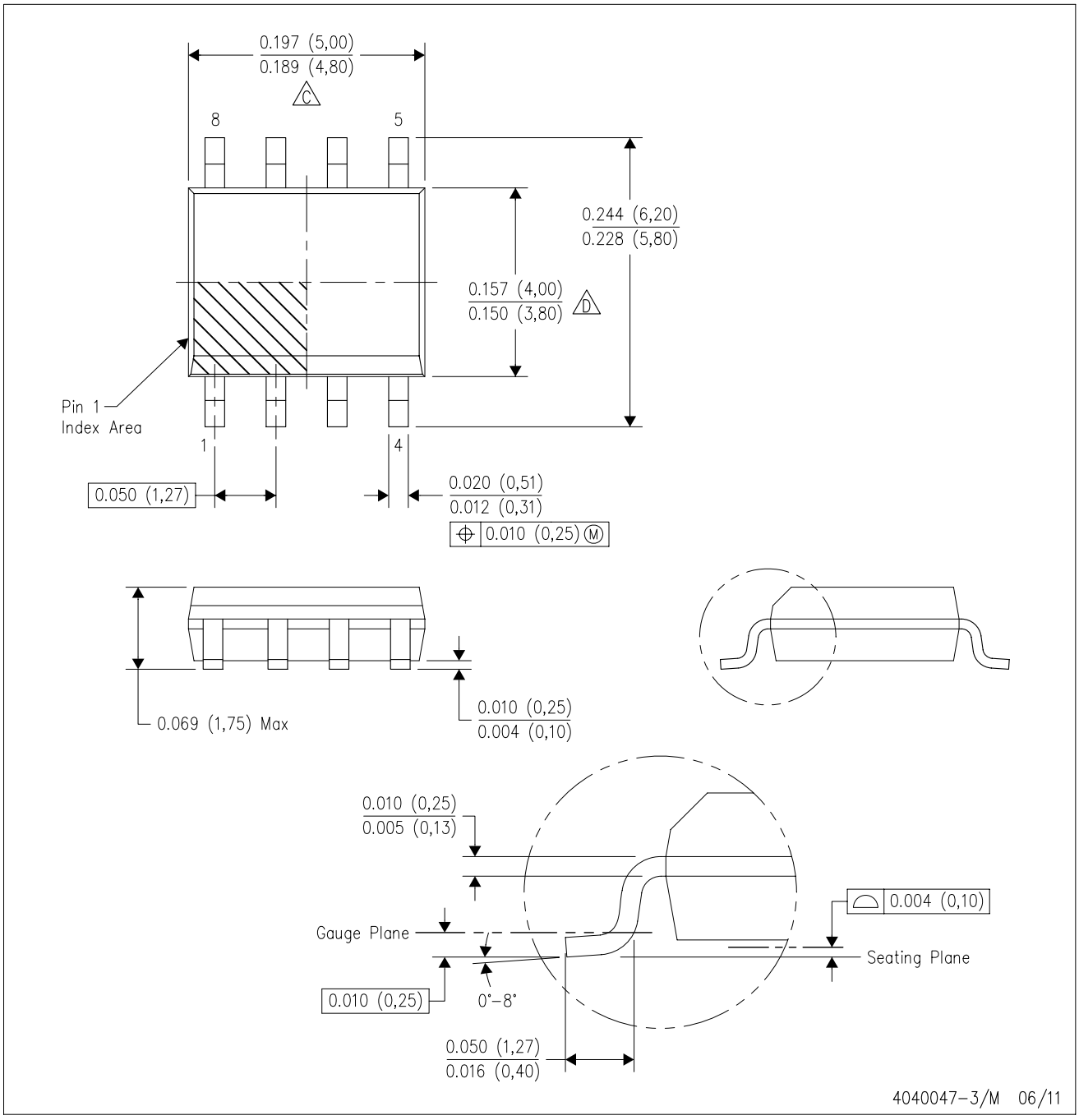
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

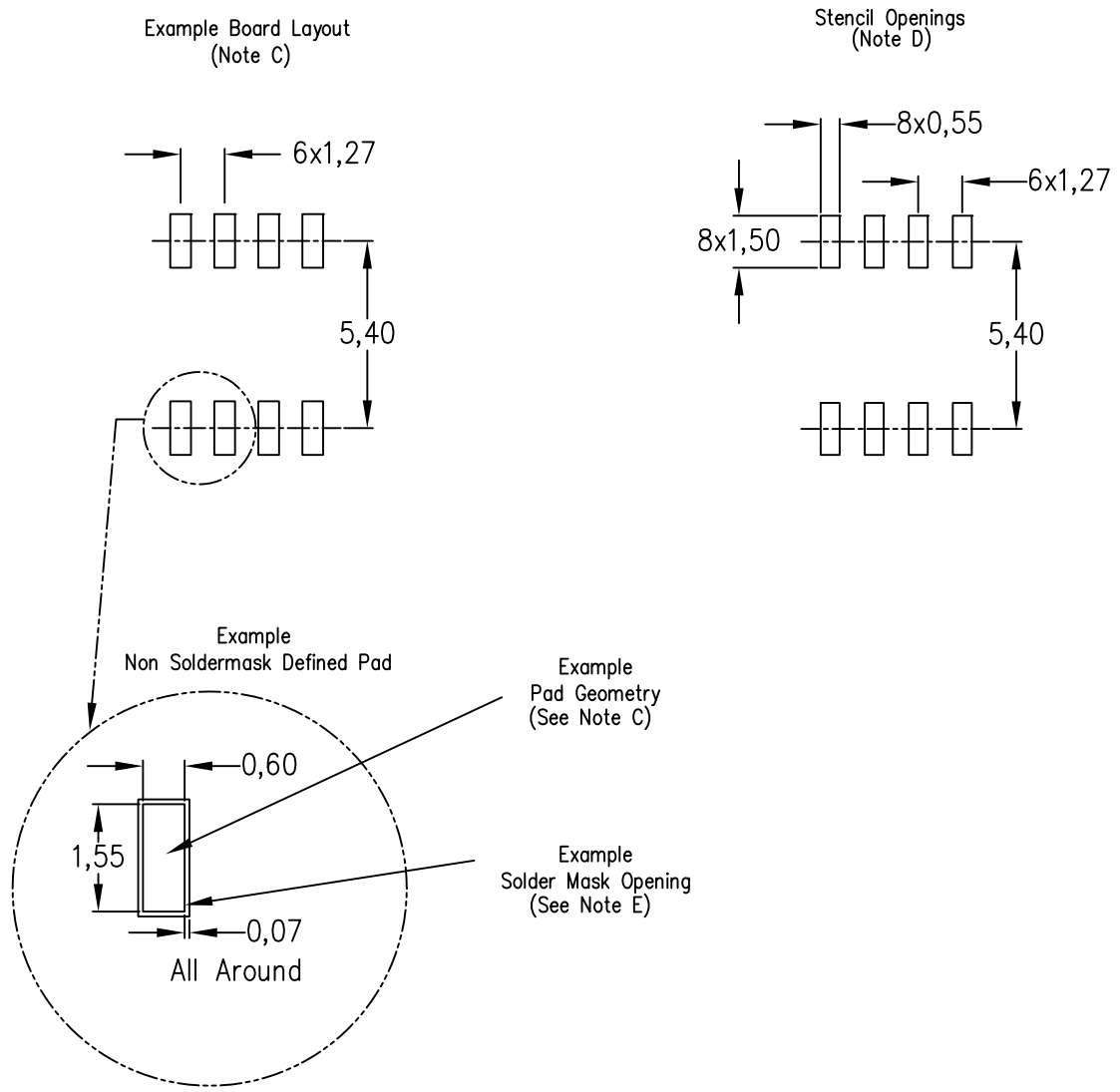
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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