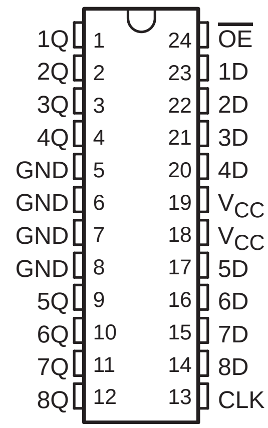
- **Specifically Designed for Data Synchronization Applications**
- **3-State Outputs Drive Bus Lines Directly**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-µm Process**
- **Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs**

DW OR NT PACKAGE
(TOP VIEW)



description

The 74AC11478 is an 8-bit dual-rank synchronizer circuit designed specifically for data synchronization applications in which the normal setup and hold time specifications are frequently violated.

Synchronization of two digital signals operating at different frequencies is a common system problem. This problem is typically solved by synchronizing one of the signals to the local clock through a flip-flop. This solution, however, causes the setup and hold time specifications associated with the flip-flop to be violated. When the setup or hold time of a flip-flop is violated, the output response is uncertain. A flip-flop is metastable if its output hangs up in the region between V_{IL} and V_{IH}. The metastable condition lasts until the flip-flop recovers into one of its two stable states. With conventional flip-flops, this recovery time can be longer than the specified maximum propagation delay.

The problem of metastability is typically solved by adding an additional layer of synchronization. This dual-rank approach is employed in the 74AC11478. The probability of the second stage entering the metastable state is exponentially reduced by this dual-rank architecture. The 74AC11478 provides a one-chip solution for system designers in asynchronous applications.

The 74AC11478 is characterized for operation from −40°C to 85°C.

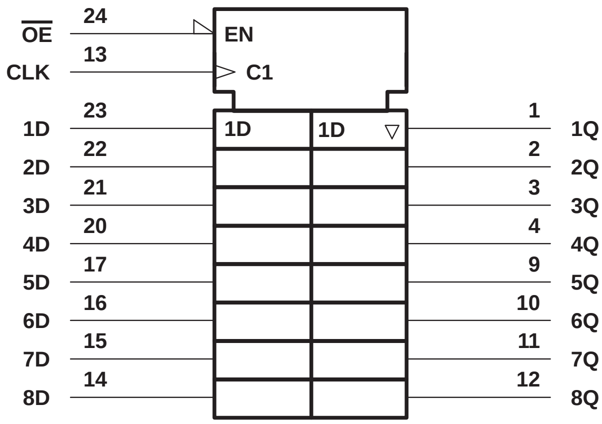
FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}$	CLK†	D	Q
H	X	X	Z
L	↑	L	L
L	↑	H	H
L	L	X	Q_0

† Data presented at the D inputs requires two clock cycles to appear at the Q outputs.

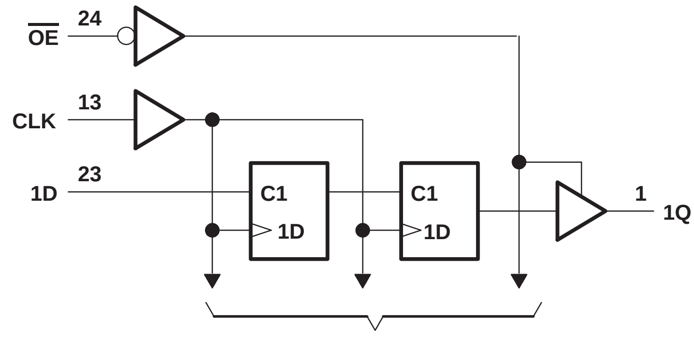
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND pins	±200 mA
Storage temperature range	−65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	TA = 25°C MIN	TA = 25°C TYP	TA = 25°C MAX	MIN	MAX	UNIT
V_{OH}	I_{OH} = − 50 µA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = − 4 mA	3 V	2.58			2.48		
	I_{OL} = − 24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = −75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 µA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	µA
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±5	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	µA
C_i	V_I = V_{CC} or GND	5 V		4.5				pF
C_o	V_O = V_{CC} or GND	5 V		10				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C MIN	T_A = 25°C MAX	MIN	MAX	UNIT
f_{clock}	Clock frequency		55		55	MHz
t_{su}	Setup time, data before CLK↑	3		3		ns
t_h	Hold time, data after CLK↑	1.5		1.5		ns
t_w	Pulse duration, CLK high or low	9		9		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

		T_A = 25°C MIN	T_A = 25°C MAX	MIN	MAX	UNIT
f_{clock}	Clock frequency		83		83	MHz
t_{su}	Setup time, data before CLK↑	2.5		2.5		ns
t_h	Hold time, data after CLK↑	1.5		1.5		ns
t_w	Pulse duration, CLK high or low	6		6		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	MIN	MAX	UNIT
f_{max}			55			55		MHz
t_{PLH}	CLK	Q	3.8	10.5	13.3	3.8	15	ns
t_{PHL}			5.5	13.2	16.8	5.5	18.4	
t_{PZH}	$\overline{OE}$	Q	3.7	10.8	13.9	3.7	16	ns
t_{PZL}			5.4	14.7	19.2	5.4	22.5	
t_{PHZ}	$\overline{OE}$	Q	3.9	7.1	9.3	3.9	10.1	ns
t_{PLZ}			4	6.9	8.9	4	9.6	

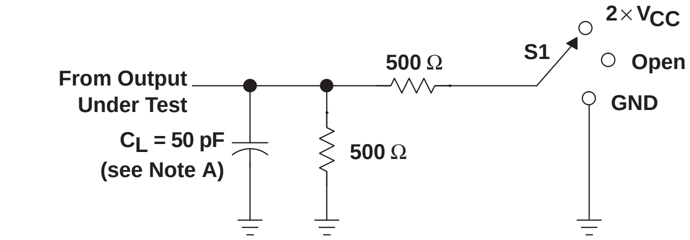
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	MIN	MAX	UNIT
f_{max}			83			83		MHz
t_{PLH}	CLK	Q	2.9	6.1	8.9	2.9	10	ns
t_{PHL}			4.3	7.9	11.2	4.3	12.3	
t_{PZH}	$\overline{OE}$	Q	2.9	6.4	9.6	2.9	10.8	ns
t_{PZL}			4.1	8.1	12.3	4.1	14.0	
t_{PHZ}	$\overline{OE}$	Q	3.2	5.7	8	3.2	8.6	ns
t_{PLZ}			3.5	5.4	7.4	3.5	8	

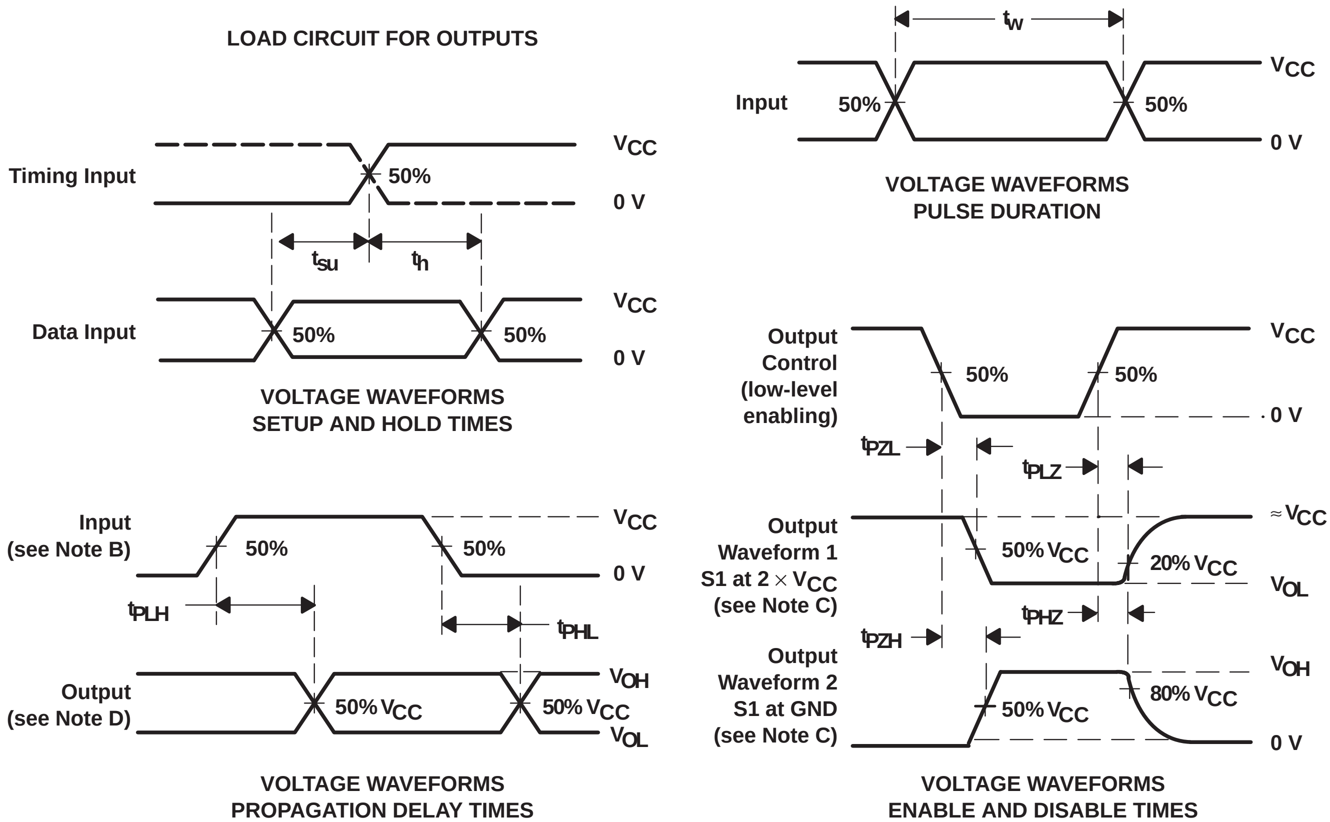
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	C_L = 50 pF, f = 1 MHz	46	pF
		Outputs disabled		33	

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns. For testing pulse duration: t_r = t_f = 1 to 3 ns. Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
74AC11478DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI
74AC11478NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
74AC11478NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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