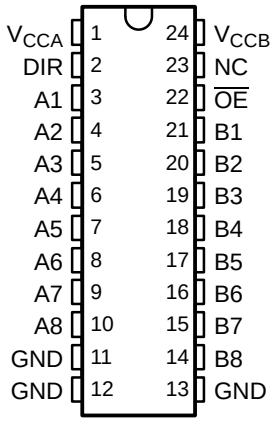
# SN74LVCC4245A
# OCTAL DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

SCAS584M – NOVEMBER 1996 – REVISED MARCH 2005

## FEATURES

- **Bidirectional Voltage Translator**
- **4.5 V to 5.5 V on A Port and 2.7 V to 5.5 V on B Port**
- **Control Inputs $V_{IH}/V_{IL}$ Levels Are Referenced to $V_{CCA}$ Voltage**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

**DB, DW, NS, OR PW PACKAGE**
**(TOP VIEW)**




NC - No internal connection

## DESCRIPTION/ORDERING INFORMATION

This 8-bit (octal) noninverting bus transceiver uses two separate power-supply rails. The A port, $V_{CCA}$, is dedicated to accepting a 5-V supply level, and the configurable B port, which is designed to track $V_{CCB}$, accepts voltages from 3 V to 5 V. This allows for translation from a 3.3-V to a 5-V environment and vice versa.

The SN74LVCC4245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses effectively are isolated. The control circuitry (DIR, $\overline{OE}$) is powered by $V_{CCA}$.

**ORDERING INFORMATION**

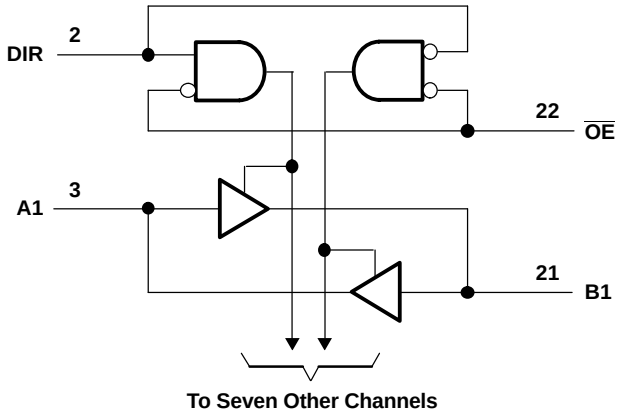
| $T_A$ | PACKAGE(1) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | SOIC – DW | Tube of 25 | SN74LVCC4245ADW | LVCC4245A |
| | | Reel of 2000 | SN74LVCC4245ADWR | |
| | SOP – NS | Reel of 2000 | SN74LVCC4245ANSR | LVCC4245A |
| | SSOP – DB | Reel of 2000 | SN74LVCC4245ADBR | LG245A |
| | TSSOP – PW | Tube of 60 | SN74LVCC4245APW | LG245A |
| | | Reel of 2000 | SN74LVCC4245APWR | |
| | | Reel of 250 | SN74LVCC4245APWT | |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE**
**(EACH TRANSCEIVER)**

| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

**LOGIC DIAGRAM (POSITIVE LOGIC)**




## Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CCA}$ $V_{CCB}$ | Supply voltage range | | –0.5 | 6 | V |
| $V_I$ | Input voltage range(2) | I/O ports (A port) | –0.5 | $V_{CCA}$ + 0.5 | V |
| | | I/O ports (B port) | –0.5 | $V_{CCB}$ + 0.5 | |
| | | Except I/O ports | –0.5 | $V_{CCA}$ + 0.5 | |
| $V_O$ | Output voltage range(2) | A port | –0.5 | $V_{CCA}$ + 0.5 | V |
| | | B port | –0.5 | $V_{CCB}$ + 0.5 | |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through $V_{CCA}$, $V_{CCB}$, or GND | | | ±100 | mA |
| $\theta_{JA}$ | Package thermal impedance(3) | DB package | | 63 | °C/W |
| | | DW package | | 46 | |
| | | NS package | | 65 | |
| | | PW package | | 88 | |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This value is limited to 6 V maximum.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions(1)

| | | $V_{CCA}$ | $V_{CCB}$ | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{CCA}$ | Supply voltage | | | 4.5 | 5 | 5.5 | V |
| $V_{CCB}$ | Supply voltage | | | 2.7 | 3.3 | 5.5 | V |
| $V_{IHA}$ | High-level input voltage | 4.5 V | 2.7 V | 2 | | | V |
| | | | 3.6 V | 2 | | | |
| | | 5.5 V | 5.5 V | 2 | | | |
| $V_{IHB}$ | High-level input voltage | 4.5 V | 2.7 V | 2 | | | V |
| | | | 3.6 V | 2 | | | |
| | | 5.5 V | 5.5 V | 3.85 | | | |
| $V_{ILA}$ | Low-level input voltage | 4.5 V | 2.7 V | | | 0.8 | V |
| | | | 3.6 V | | | 0.8 | |
| | | 5.5 V | 5.5 V | | | 0.8 | |
| $V_{ILB}$ | Low-level input voltage | 4.5 V | 2.7 V | | | 0.8 | V |
| | | | 3.6 V | | | 0.8 | |
| | | 5.5 V | 5.5 V | | | 1.65 | |
| $V_{IH}$ | High-level input voltage (control pins) (referenced to $V_{CCA}$) | 4.5 V | 2.7 V | 2 | | | V |
| | | | 3.6 V | 2 | | | |
| | | 5.5 V | 5.5 V | 2 | | | |
| $V_{IL}$ | Low-level input voltage (control pins) (referenced to $V_{CCA}$) | 4.5 V | 2.7 V | | | 0.8 | V |
| | | | 3.6 V | | | 0.8 | |
| | | 5.5 V | 5.5 V | | | 0.8 | |
| $V_{IA}$ | Input voltage | | | 0 | | $V_{CCA}$ | V |
| $V_{IB}$ | Input voltage | | | 0 | | $V_{CCB}$ | V |
| $V_{OA}$ | Output voltage | | | 0 | | $V_{CCA}$ | V |
| $V_{OB}$ | Output voltage | | | 0 | | $V_{CCB}$ | V |
| $I_{OHA}$ | High-level output current | 4.5 V | 3 V | | | –24 | mA |
| $I_{OHB}$ | High-level output current | 4.5 V | 2.7 V to 4.5 V | | | –24 | mA |
| $I_{OLA}$ | Low-level output current | 4.5 V | 3 V | | | 24 | mA |
| $I_{OLB}$ | Low-level output current | 4.5 V | 2.7 V to 4.5 V | | | 24 | mA |
| $T_A$ | Operating free-air temperature | | | –40 | | 85 | °C |

(1) All unused inputs of the device must be held at the associated $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CCA}$ | $V_{CCB}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OHA}$ | | $I_{OH}$ = –100 μA | 4.5 V | 3 V | 4.4 | 4.49 | | V |
| | | $I_{OH}$ = –24 mA | 4.5 V | 3 V | 3.76 | 4.25 | | |
| $V_{OHB}$ | | $I_{OH}$ = –100 μA | 4.5 V | 3 V | 2.9 | 2.99 | | V |
| | | $I_{OH}$ = –12 mA | 4.5 V | 2.7 V | 2.2 | 2.5 | | |
| | | | | 3 V | 2.46 | 2.85 | | |
| | | $I_{OH}$ = –24 mA | 4.5 V | 2.7 V | 2.1 | 2.3 | | |
| | | | | 3 V | 2.25 | 2.65 | | |
| | | | | 4.5 V | 3.76 | 4.25 | | |
| $V_{OLA}$ | | $I_{OL}$ = 100 μA | 4.5 V | 3 V | | | 0.1 | V |
| | | $I_{OL}$ = 24 mA | 4.5 V | 3 V | | 0.21 | 0.44 | |
| $V_{OLB}$ | | $I_{OL}$ = 100 μA | 4.5 V | 3 V | | | 0.1 | V |
| | | $I_{OL}$ = 12 mA | 4.5 V | 2.7 V | | 0.11 | 0.44 | |
| | | $I_{OL}$ = 24 mA | 4.5 V | 2.7 V | | 0.22 | 0.5 | |
| | | | | 3 V | | 0.21 | 0.44 | |
| | | | | 4.5 V | | 0.18 | 0.44 | |
| $I_I$ | Control inputs | $V_I = V_{CCA}$ or GND | 5.5 V | 3.6 V | | ±0.1 | ±1 | μA |
| | | | | 5.5 V | | ±0.1 | ±1 | |
| $I_{OZ}$(1) | A or B ports | $V_O = V_{CCA/B}$ or GND, $V_I = V_{IL}$ or $V_{IH}$ | 5.5 V | 3.6 V | | ±0.5 | ±5 | μA |
| $I_{CCA}$ | B to A | $A_n = V_{CC}$ or GND | 5.5 V | Open | | 8 | 80 | μA |
| | | $I_O$ (A port) = 0, $B_n = V_{CCB}$ or GND | 5.5 V | 3.6 V | | 8 | 80 | |
| | | | | 5.5 V | | 8 | 80 | |
| $I_{CCB}$ | A to B | $A_n = V_{CCA}$ or GND, $I_O$ (B port) = 0 | 5.5 V | 3.6 V | | 5 | 50 | μA |
| | | | | 5.5 V | | 8 | 80 | |
| $\Delta I_{CCA}$(2) | A port | $V_I = V_{CCA}$ – 2.1 V, Other inputs at $V_{CCA}$ or GND, $\overline{OE}$ at GND and DIR at $V_{CCA}$ | 5.5 V | 5.5 V | | 1.35 | 1.5 | mA |
| | $\overline{OE}$ | $V_I = V_{CCA}$ – 2.1 V, Other inputs at $V_{CCA}$ or GND, DIR at $V_{CCA}$ or GND | 5.5 V | 5.5 V | | 1 | 1.5 | |
| | DIR | $V_I = V_{CCA}$ – 2.1 V, Other inputs at $V_{CCA}$ or GND, $\overline{OE}$ at $V_{CCA}$ or GND | 5.5 V | 3.6 V | | 1 | 1.5 | |
| $\Delta I_{CCB}$(2) | B port | $V_I = V_{CCB}$ – 0.6 V, Other inputs at $V_{CCB}$ or GND, $\overline{OE}$ at GND and DIR at GND | 5.5 V | 3.6 V | | 0.35 | 0.5 | mA |
| $C_i$ | Control inputs | $V_I = V_{CCA}$ or GND | Open | Open | | 5 | | pF |
| $C_{io}$ | A or B ports | $V_O = V_{CCA/B}$ or GND | 5 V | 3.3 V | | 11 | | pF |

(1) For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
(2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or the associated $V_{CC}$.

## Switching Characteristics

over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1 through Figure 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCA}$ = 5 V ± 0.5 V, $V_{CCB}$ = 5 V ± 0.5 V | | $V_{CCA}$ = 5 V ± 0.5 V, $V_{CCB}$ = 2.7 V to 3.6 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{PHL}$ | A | B | 1 | 7.1 | 1 | 7 | ns |
| $t_{PLH}$ | | | 1 | 6 | 1 | 7 | |
| $t_{PHL}$ | B | A | 1 | 6.8 | 1 | 6.2 | ns |
| $t_{PLH}$ | | | 1 | 6.1 | 1 | 5.3 | |
| $t_{PZL}$ | $\overline{OE}$ | A | 1 | 9 | 1 | 9 | ns |
| $t_{PZH}$ | | | 1 | 8.3 | 1 | 8 | |
| $t_{PZL}$ | $\overline{OE}$ | B | 1 | 8.2 | 1 | 10 | ns |
| $t_{PZH}$ | | | 1 | 8.1 | 1 | 10.2 | |
| $t_{PLZ}$ | $\overline{OE}$ | A | 1 | 4.7 | 1 | 5.2 | ns |
| $t_{PHZ}$ | | | 1 | 4.9 | 1 | 5.2 | |
| $t_{PLZ}$ | $\overline{OE}$ | B | 1 | 5.4 | 1 | 5.4 | ns |
| $t_{PHZ}$ | | | 1 | 6.3 | 1 | 7.4 | |

## Operating Characteristics

$V_{CCA}$ = 5 V, $V_{CCB}$ = 3.3 V, $T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per transceiver | Outputs enabled | $C_L$ = 0, f = 10 MHz | 20 | pF |
| | | Outputs disabled | | 6.5 | |

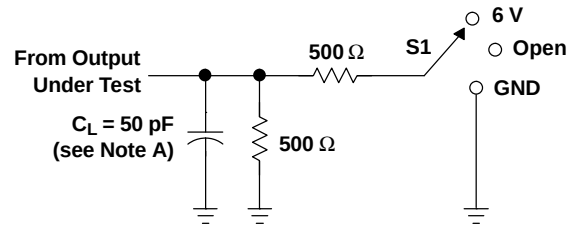
## Power-Up Considerations(1)

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins. Take these precautions to guard against such power-up problems:

1. Connect ground before any supply voltage is applied.
2. Power up the control side of the device ($V_{CCA}$ for all four of these devices).
3. Tie $\overline{OE}$ to $V_{CCA}$ with a pullup resistor so that it ramps with $V_{CCA}$.
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with $V_{CCA}$. Otherwise, keep DIR low.

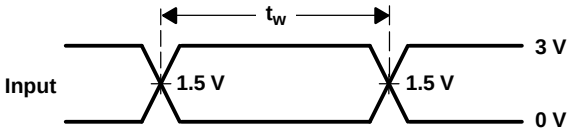
(1) Refer to the TI application report, *Texas Instruments Voltage-Level-Translation Devices*, literature number SCEA021.

## PARAMETER MEASUREMENT INFORMATION FOR A TO B
## $V_{CCA}$ = 4.5 V TO 5.5 V AND $V_{CCB}$ = 2.7 V TO 3.6 V

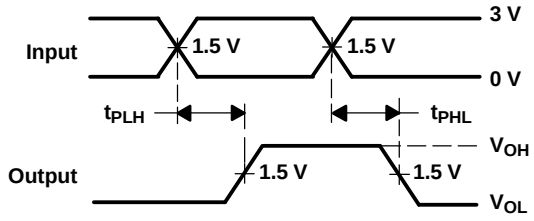



LOAD CIRCUIT

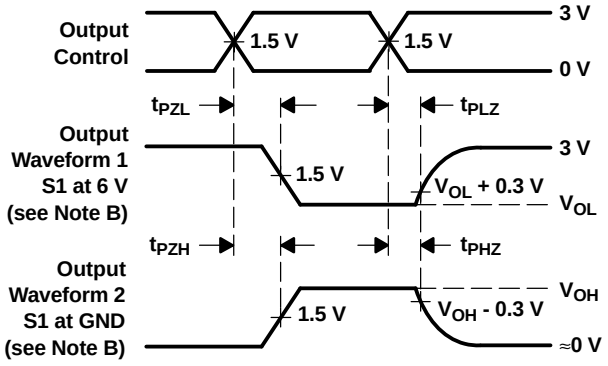
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS

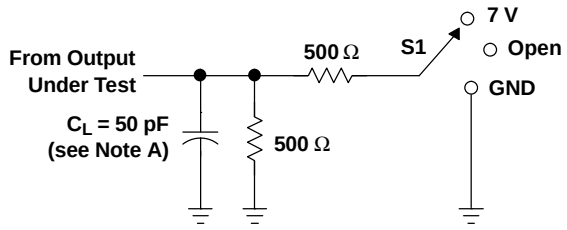



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

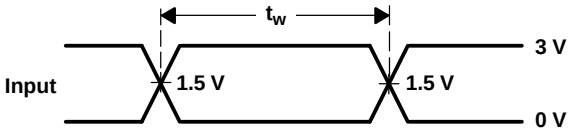
**Figure 1. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION FOR A TO B
## $V_{CCA}$ = 4.5 V TO 5.5 V AND $V_{CCB}$ = 3.6 V TO 5.5 V

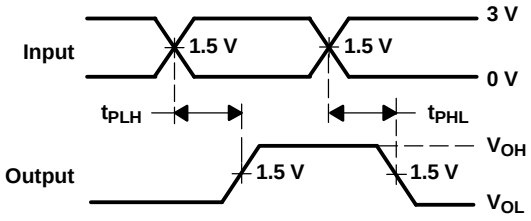



LOAD CIRCUIT

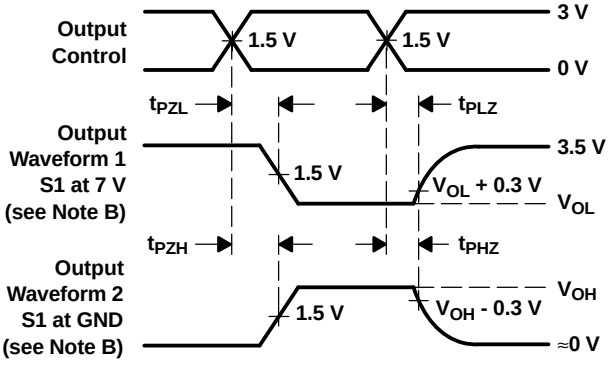
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS

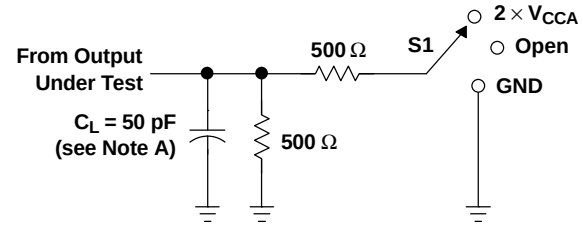



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

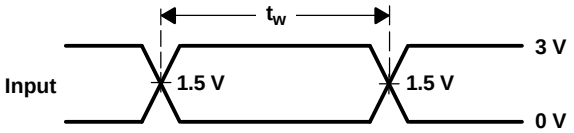
**Figure 2. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION FOR B TO A
## $V_{CCA}$ = 4.5 V to 5.5 V AND $V_{CCB}$ = 2.7 V TO 3.6 V

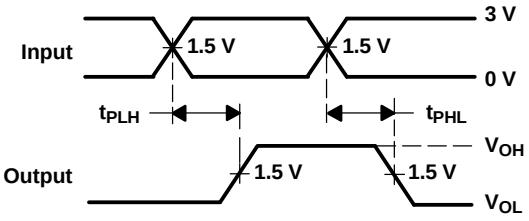



LOAD CIRCUIT

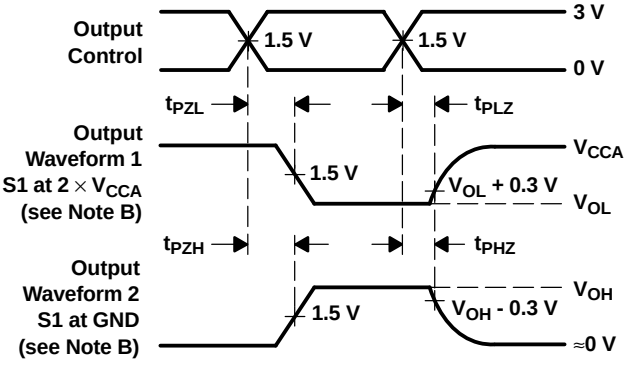
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CCA}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS

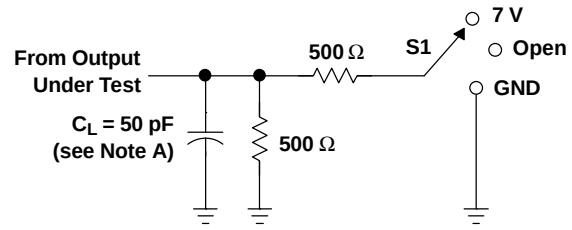



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

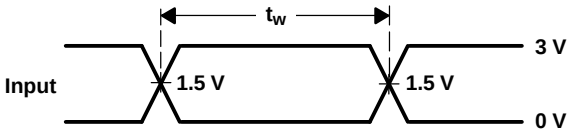
**Figure 3. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION FOR B TO A
## $V_{CCA}$ = 4.5 V TO 5.5 V AND $V_{CCB}$ = 3.6 V TO 5.5 V

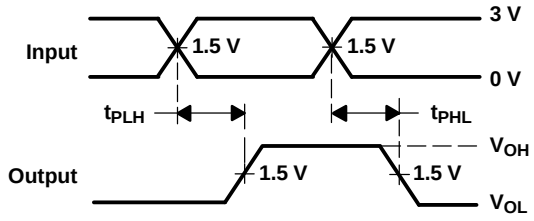



LOAD CIRCUIT

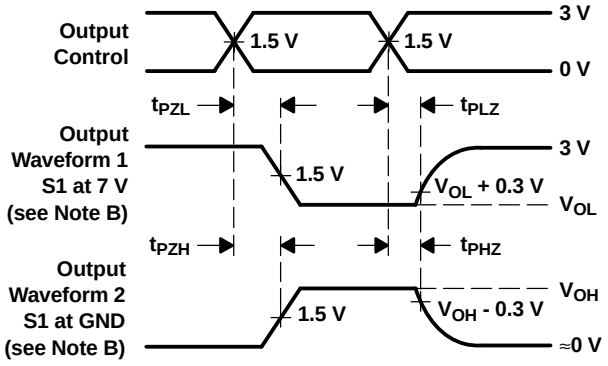
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

**Figure 4. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| SN74LVCC4245ADBLE | OBSOLETE | SSOP | DB | 24 | | TBD | Call TI | Call TI | |
| SN74LVCC4245ADBR | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVCC4245ADBRE4 | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVCC4245ADBRG4 | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVCC4245ADW | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVCC4245ADWE4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVCC4245ADWG4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVCC4245ADWR | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVCC4245ADWRE4 | ACTIVE | SOIC | DW | 24 | | TBD | Call TI | Call TI | |
| SN74LVCC4245ADWRG4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVCC4245ANSR | ACTIVE | SO | NS | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVCC4245ANSRE4 | ACTIVE | SO | NS | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVCC4245ANSRG4 | ACTIVE | SO | NS | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVCC4245APW | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVCC4245APWE4 | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVCC4245APWG4 | ACTIVE | TSSOP | PW | 24 | 60 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVCC4245APWLE | OBSOLETE | TSSOP | PW | 24 | | TBD | Call TI | Call TI | |
| SN74LVCC4245APWR | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| SN74LVCC4245APWRE4 | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVCC4245APWRG4 | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVCC4245APWT | ACTIVE | TSSOP | PW | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVCC4245APWTE4 | ACTIVE | TSSOP | PW | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LVCC4245APWTG4 | ACTIVE | TSSOP | PW | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



**OTHER QUALIFIED VERSIONS OF SN74LVCC4245A :**

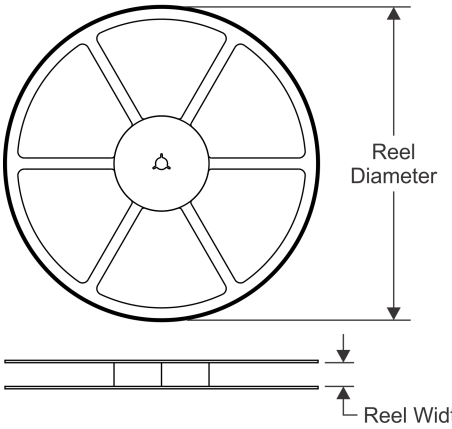
- Enhanced Product: SN74LVCC4245A-EP

NOTE: Qualified Version Definitions:

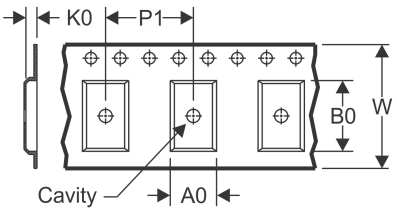
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

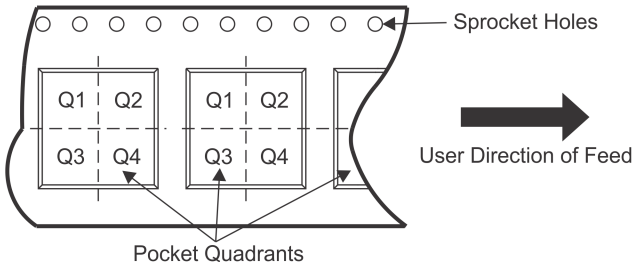



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

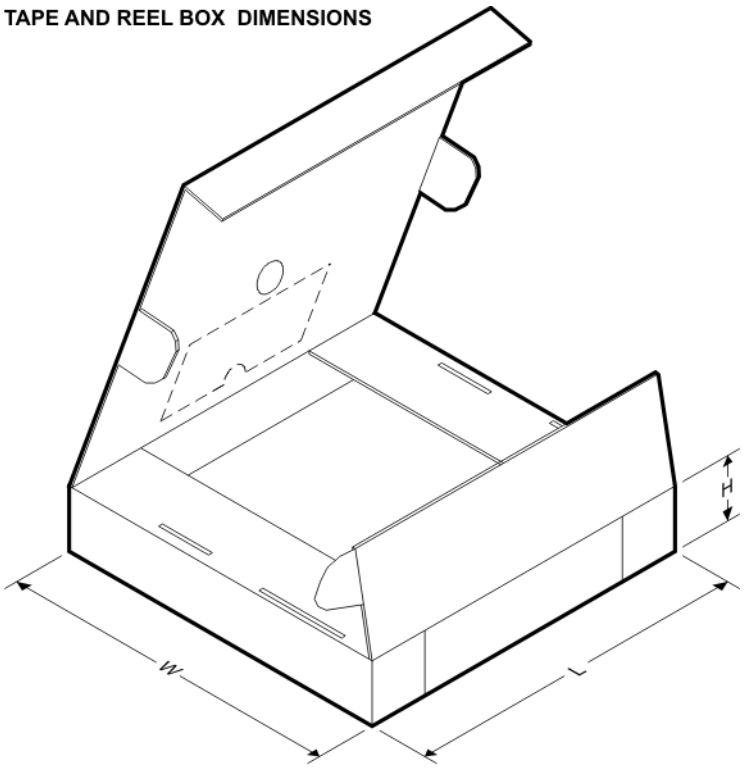
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVCC4245ADBR | SSOP | DB | 24 | 2000 | 330.0 | 16.4 | 8.2 | 8.8 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVCC4245ADWR | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LVCC4245ADWRG4 | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LVCC4245ANSR | SO | NS | 24 | 2000 | 330.0 | 24.4 | 8.2 | 15.4 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74LVCC4245APWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74LVCC4245APWT | TSSOP | PW | 24 | 250 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

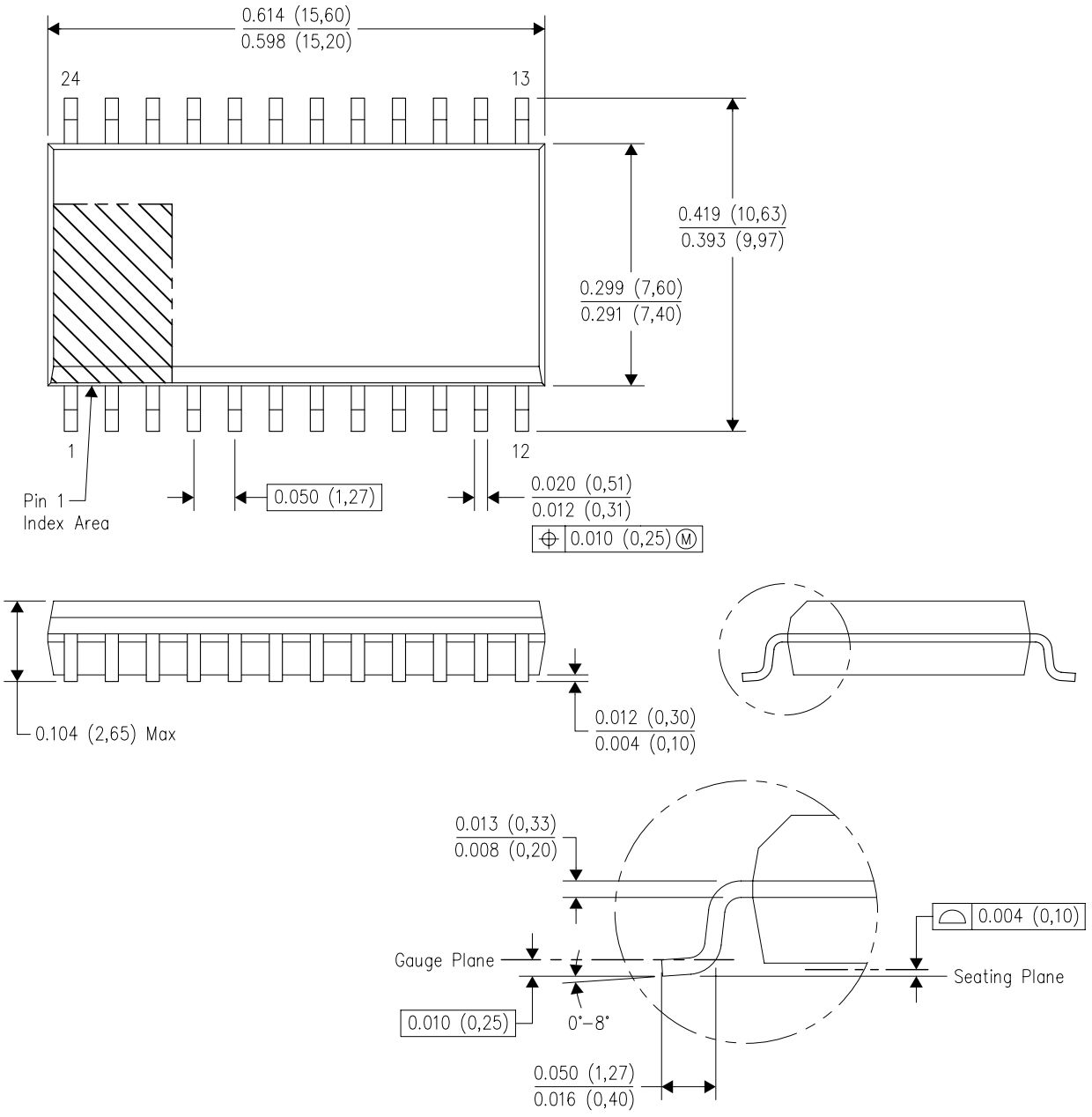
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

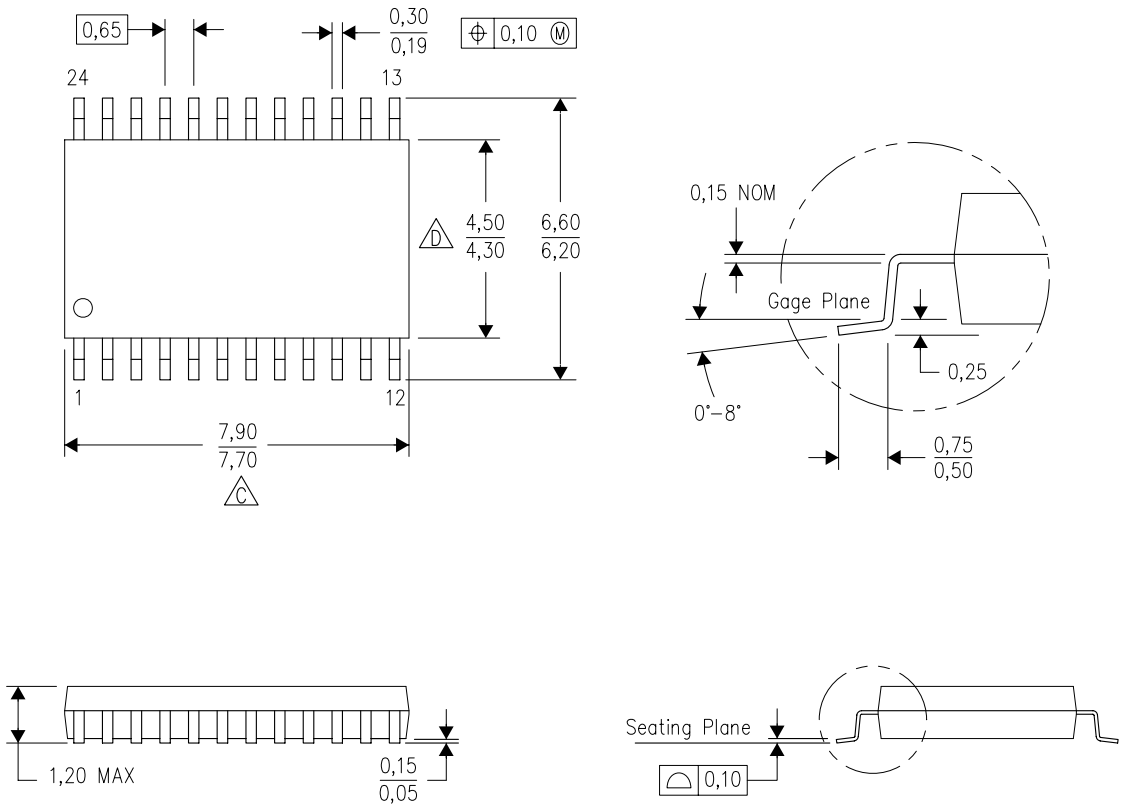
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LVCC4245ADBR | SSOP | DB | 24 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LVCC4245ADWR | SOIC | DW | 24 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LVCC4245ADWRG4 | SOIC | DW | 24 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LVCC4245ANSR | SO | NS | 24 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LVCC4245APWR | TSSOP | PW | 24 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LVCC4245APWT | TSSOP | PW | 24 | 250 | 367.0 | 367.0 | 38.0 |

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

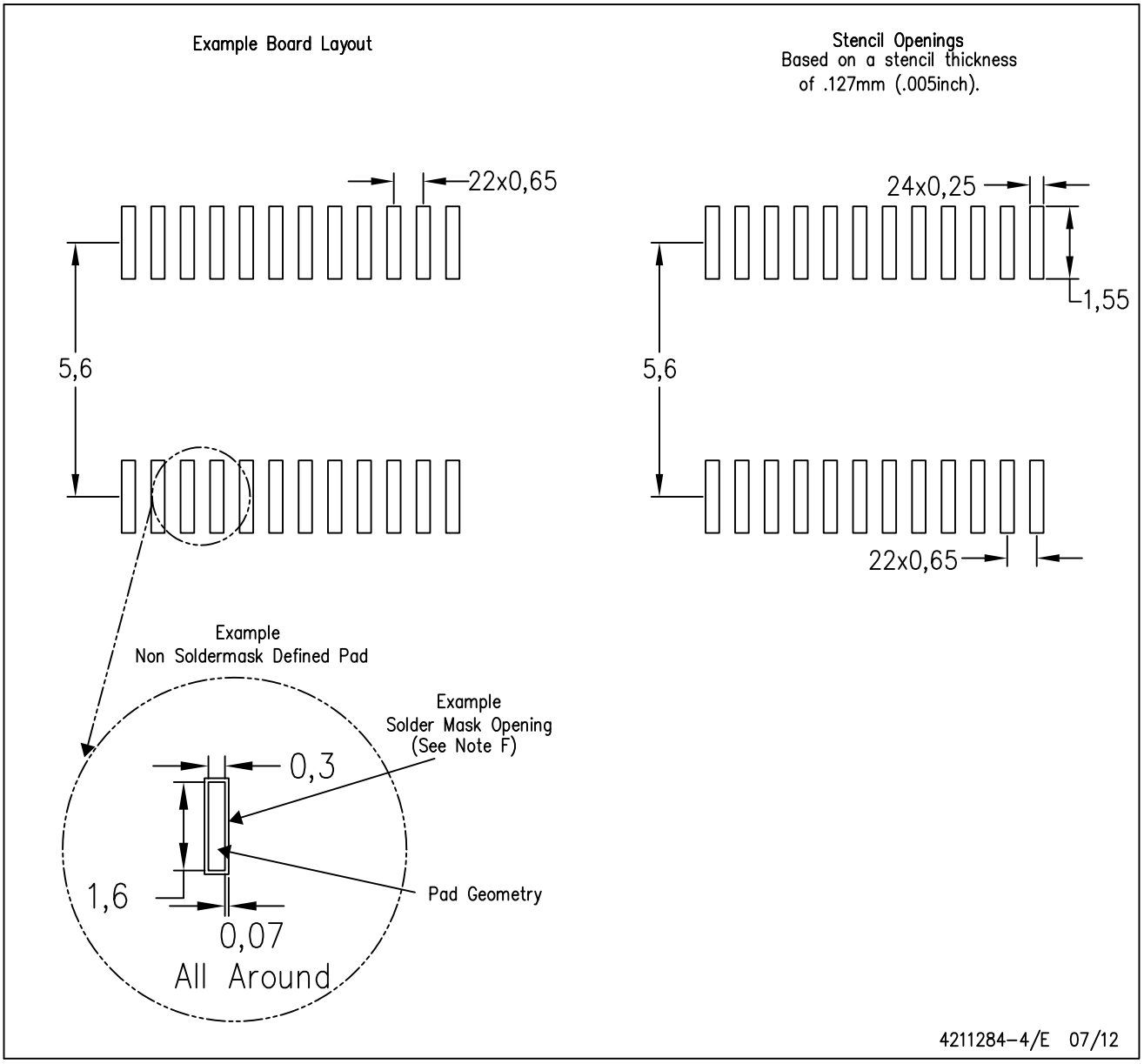
PW (R–PDSO–G24) PLASTIC SMALL OUTLINE




4040064–6/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE

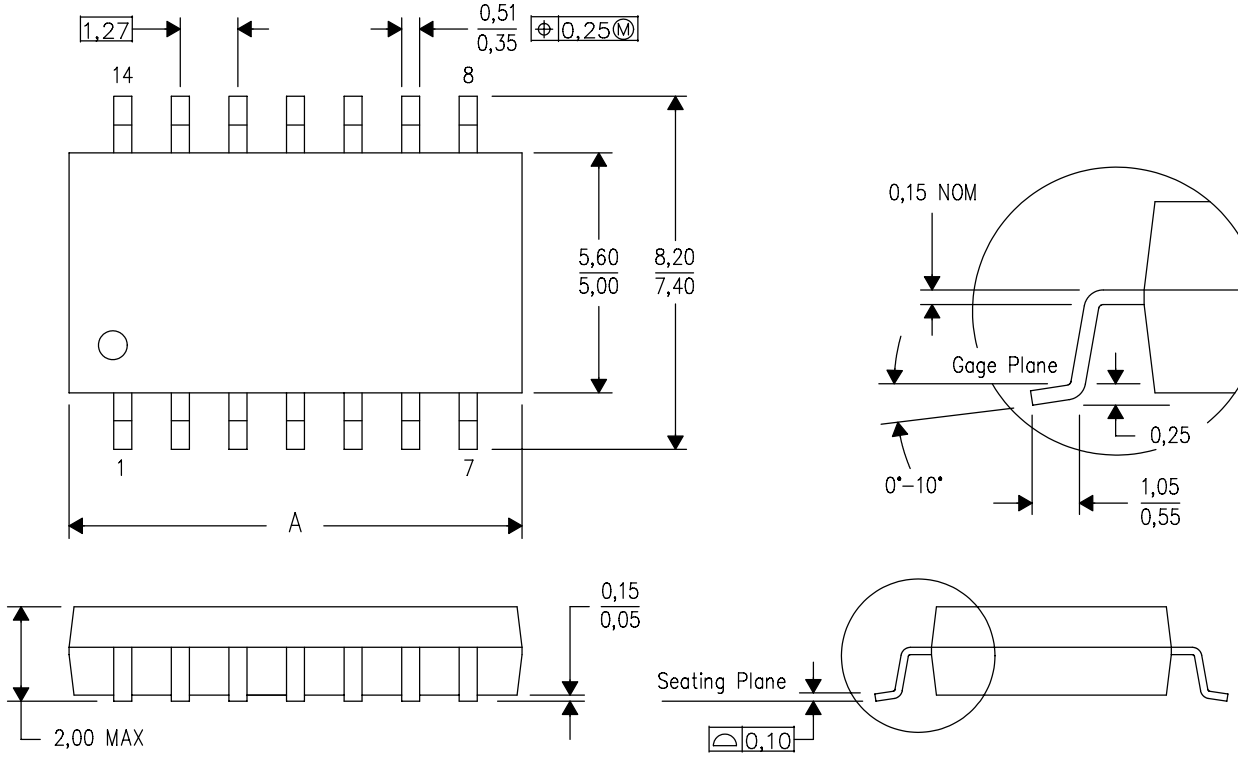



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

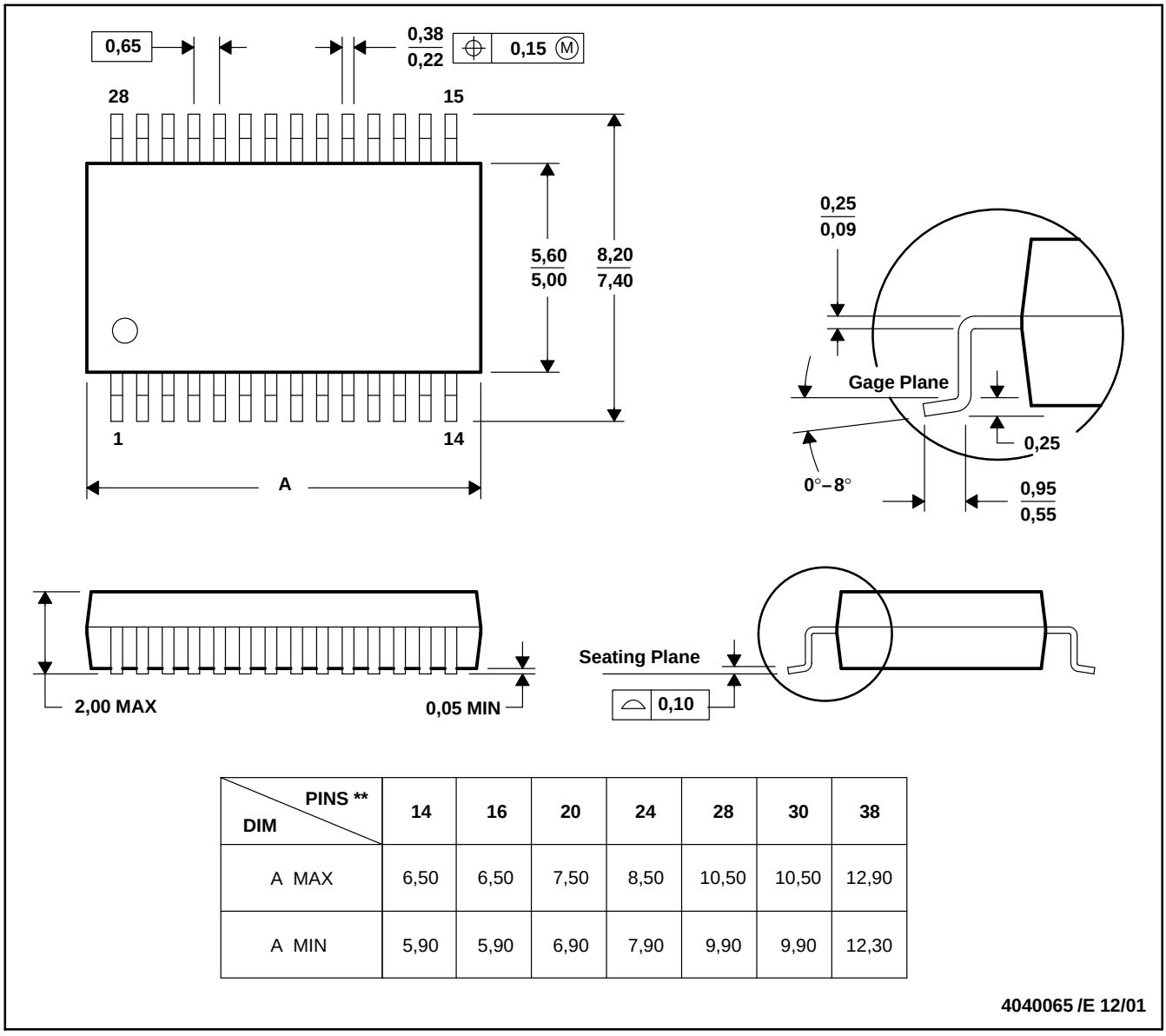
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

**DB (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**28 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

**4040065 /E 12/01**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

| **Products** | | **Applications** | |
|---|---|---|---|
| Audio | www.ti.com/audio | Automotive and Transportation | www.ti.com/automotive |
| Amplifiers | amplifier.ti.com | Communications and Telecom | www.ti.com/communications |
| Data Converters | dataconverter.ti.com | Computers and Peripherals | www.ti.com/computers |
| DLP® Products | www.dlp.com | Consumer Electronics | www.ti.com/consumer-apps |
| DSP | dsp.ti.com | Energy and Lighting | www.ti.com/energy |
| Clocks and Timers | www.ti.com/clocks | Industrial | www.ti.com/industrial |
| Interface | interface.ti.com | Medical | www.ti.com/medical |
| Logic | logic.ti.com | Security | www.ti.com/security |
| Power Mgmt | power.ti.com | Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Microcontrollers | microcontroller.ti.com | Video and Imaging | www.ti.com/video |
| RFID | www.ti-rfid.com | | |
| OMAP Applications Processors | www.ti.com/omap | **TI E2E Community** | e2e.ti.com |
| Wireless Connectivity | www.ti.com/wirelessconnectivity | | |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265