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SN74LVCH16652A-EP
16-BIT BUS TRANSCEIVER AND REGISTER
WITH 3-STATE OUTPUTS
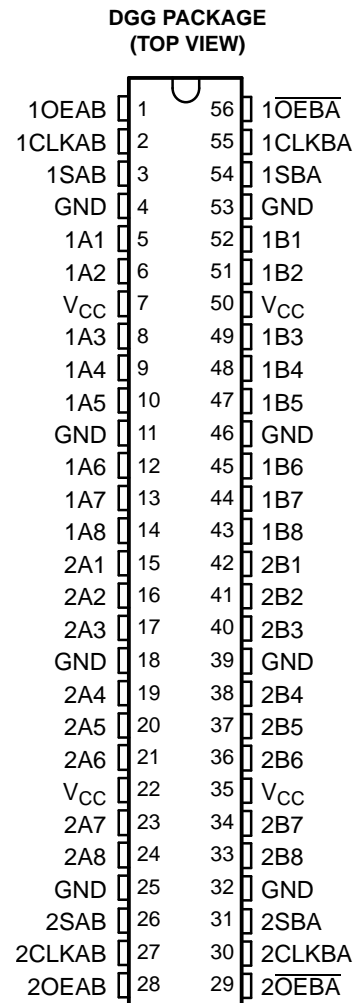SCAS743A−DECEMBER 2003−REVISED AUGUST 2005

FEATURES

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** [1]
- **Member of the Texas Instruments Widebus™ Family**
- **Operates From 1.65 V to 3.6 V**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 6.3 ns at 3.3 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

DGG PACKAGE
(TOP VIEW)

1OEAB	1	56	1$\overline{OEBA}$
1CLKAB	2	55	1CLKBA
1SAB	3	54	1SBA
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
V_{CC}	7	50	V_{CC}
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V_{CC}	22	35	V_{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2SAB	26	31	2SBA
2CLKAB	27	30	2CLKBA
2OEAB	28	29	2$\overline{OEBA}$

DESCRIPTION/ORDERING INFORMATION

This 16-bit bus transceiver and register is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVCH16652A consists of D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

Complementary output-enable (OEAB and $\overline{\text{OEBA}}$) inputs control the transceiver functions. Select-control (SAB and SBA) inputs select whether real-time or stored data is transferred. A low input level selects real-time data, and a high input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74LVCH16652A.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs, regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in the real-time transfer mode, it also is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. In this configuration, each output reinforces its input. When all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last-level configuration.

To ensure the high-impedance state during power up or power down, $\overline{\text{OEBA}}$ should be tied to V_{CC} through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended. The bus-hold circuitry is part of the input circuit and is not disabled by $\overline{\text{OE}}$ or DIR.

ORDERING INFORMATION

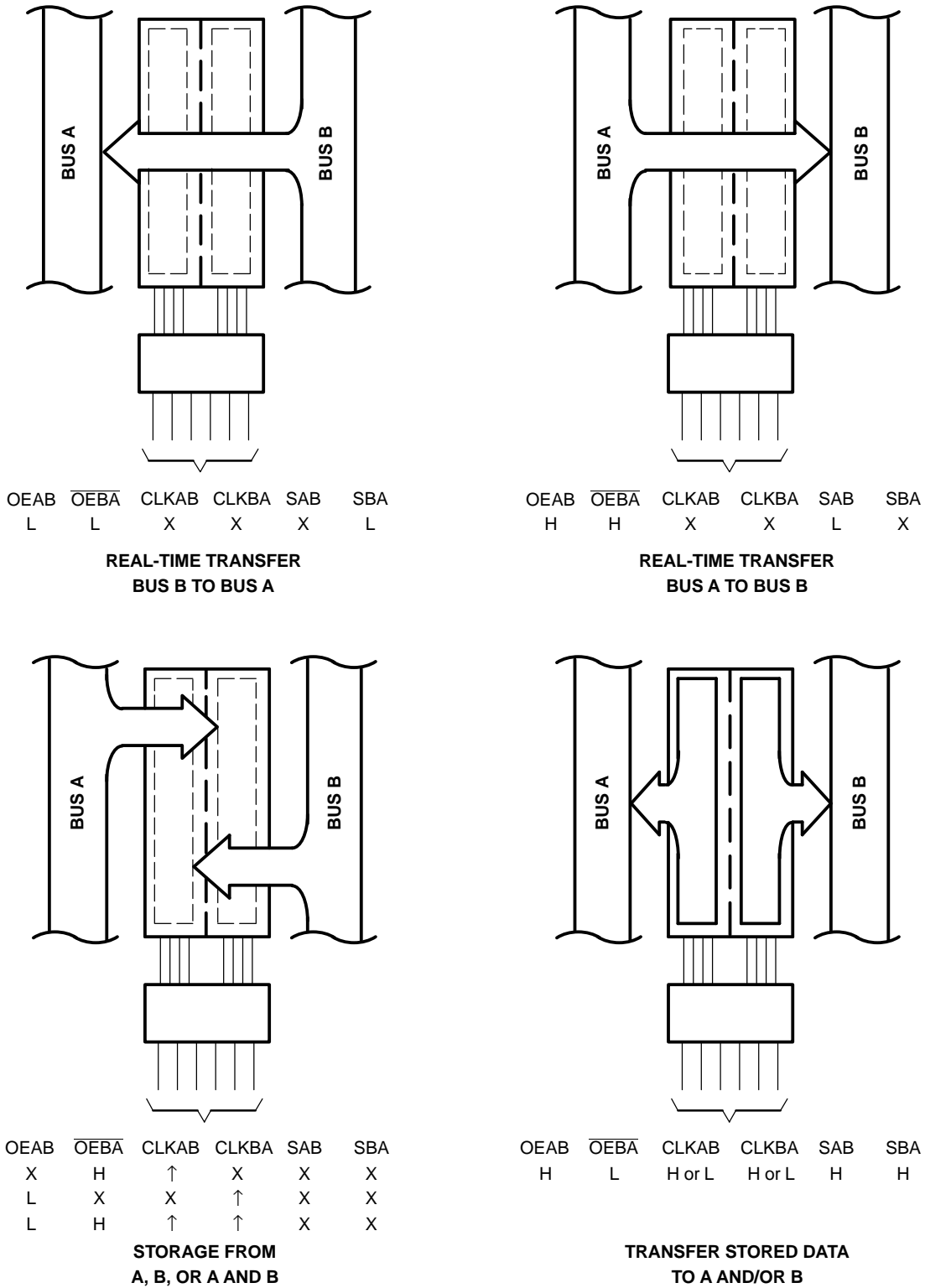| T_A	PACKAGE[1]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	TSSOP – DGG	Tape and reel	CLVCH16652AIDGGREP	CH16652AEP

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS						DATA I/O[1]		OPERATION OR FUNCTION
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA	A1−A8	B1−B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified[2]	Store A, hold B
H	H	↑	↑	X[2]	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified[2]	Input	Hold A, store B
L	L	↑	↑	X	X[2]	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Stored A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data to A bus

(1) The data-output functions can be enabled or disabled by a variety of level combinations at OEAB or $\overline{\text{OEBA}}$. Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.
(2) Select control = L, clocks can occur simultaneously. Select control = H, clocks must be staggered to load both registers.
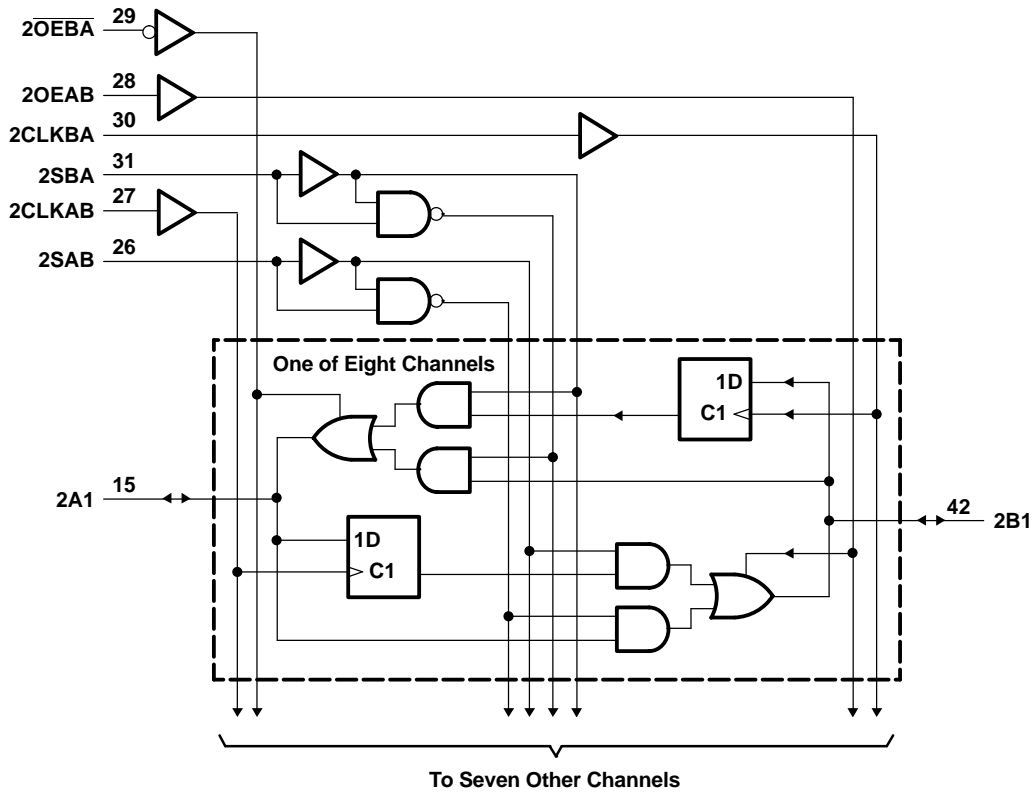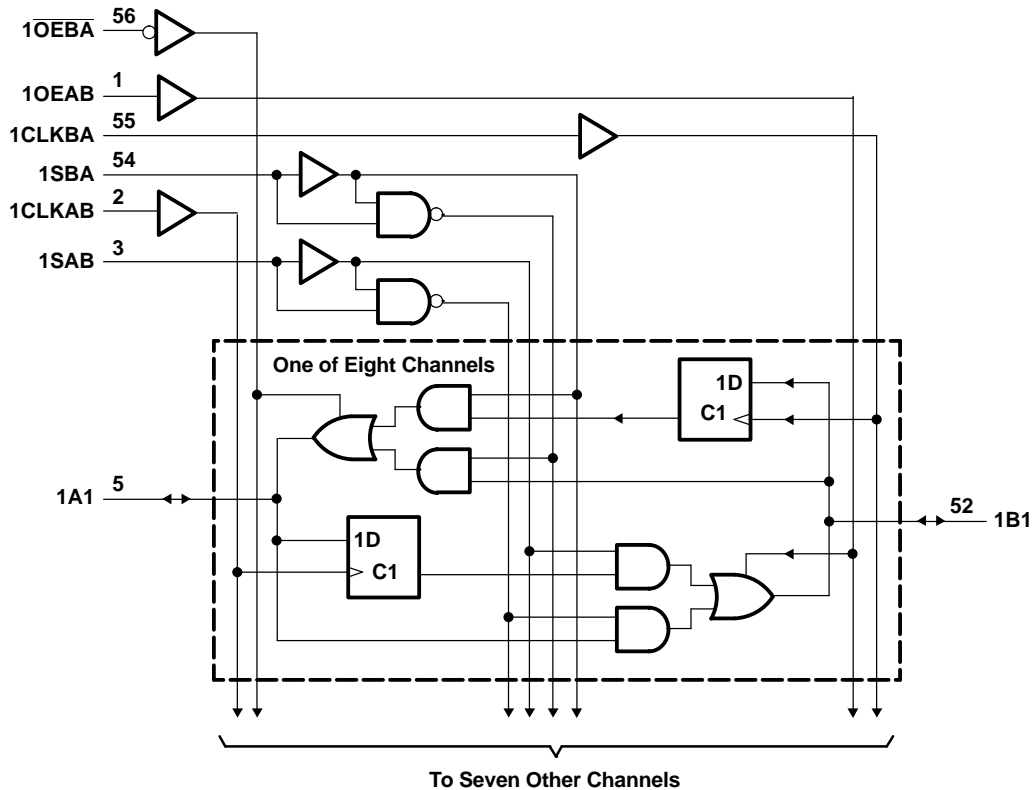
OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A

OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B

OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B

OEAB	$\overline{\text{OEBA}}$	CLKAB	CLKBA	SAB	SBA
H	L	H or L	H or L	H	H

TRANSFER STORED DATA
TO A AND/OR B

Figure 1. Bus-Management Functions

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LOGIC DIAGRAM (POSITIVE LOGIC)

To Seven Other Channels

To Seven Other Channels

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Absolute Maximum Ratings[(1)]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	6.5	V
V_I	Input voltage range[(2)]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[(2)]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state[(2)][(3)]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		−50	mA
I_{OK}	Output clamp current	V_O < 0		−50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance[(4)]			64	°C/W
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[(1)]

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 1.65 V		−4	mA
		V_{CC} = 2.3 V		−8	
		V_{CC} = 2.7 V		−12	
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		−40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{OH}		I_{OH} = −100 µA		1.65 V to 3.6 V	V_{CC} − 0.2			V
		I_{OH} = −4 mA		1.65 V	1.2			
		I_{OH} = -8 mA		2.3 V	1.7			
		I_{OH} = −12 mA		2.7 V	2.2			
				3 V	2.4			
		I_{OH} = −24 mA		3 V	2.2			
V_{OL}		I_{OL} = 100 µA		1.65 V to 3.6 V			0.2	V
		I_{OL} = 4 mA		1.65 V			0.45	
		I_{OL} = 8 mA		2.3 V			0.7	
		I_{OL} = 12 mA		2.7 V			0.4	
		I_{OL} = 24 mA		3 V			0.55	
I_I	Control inputs	V_I = 0 to 5.5 V		3.6 V			±5	µA
$I_{I(hold)}$	A or B port	V_I = 0.58 V		1.65 V		[2]		µA
		V_I = 1.07 V				[2]		
		V_I = 0.7 V		2.3 V		45		
		V_I = 1.7 V				−45		
		V_I = 0.8 V		3 V		75		
		V_I = 2 V				−75		
		V_I = 0 to 3.6 V[3]		3.6 V			±500	
I_{off}		V_I or V_O = 5.5 V		0			±10	µA
I_{OZ}[4]		V_O = 0 V or (V_{CC} to 5.5 V)		3.6 V			±10	µA
I_{CC}		V_I = V_{CC} or GND	I_O = 0	3.6 V			20	µA
		3.6 V ≤ V_I ≤ 5.5 V[5]					20	
ΔI_{CC}		One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND		2.7 V to 3.6 V			500	µA
C_i	Control inputs	V_I = V_{CC} or GND		3.3 V		5		pF
C_{io}	A or B port	V_O = V_{CC} or GND		3.3 V		8		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) This information was not available at the time of publication.
(3) This is the bus-hold maximum dynamic current required to switch the input from one state to another.
(4) For the total leakage current in an I/O port, please consult the $I_{I(hold)}$ specification for the input voltage condition 0 V < V_I < V_{CC}, and the I_{OZ} specification for the input voltage conditions V_I = 0 V or V_I = V_{CC} to 5.5 V. The bus-hold current, at input voltage greater than V_{CC}, is negligible.
(5) This applies in the disabled state only.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

		V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		[1]		[1]		150		150	MHz
t_w	Pulse duration, CLK high or low	[1]		[1]		3.3		3.3		ns
t_{su}	Setup time, A or B before CLKAB↑ or CLKBA↑	[1]		[1]		3.4		3		ns
t_h	Hold time, A or B after CLKAB↑ or CLKBA↑	[1]		[1]		0		0.2		ns

(1) This information was not available at the time of publication.

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Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\,V \pm 0.15\,V$		$V_{CC} = 2.5\,V \pm 0.2\,V$		$V_{CC} = 2.7\,V$		$V_{CC} = 3.3\,V \pm 0.3\,V$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			(1)		(1)		150		150		MHz
t_{pd}	A or B	B or A	(1)	(1)	(1)	(1)		6.4	1.4	6.3	ns
	CLKAB or CLKBA	A or B	(1)	(1)	(1)	(1)		7.3	2.4	6.4	
	SAB or SBA	B or A	(1)	(1)	(1)	(1)		8.8	1.9	7.4	
t_{en}	$\overline{OE}$ or OE	A or B	(1)	(1)	(1)	(1)		6.6	1.6	6.3	ns
t_{dis}	$\overline{OE}$ or OE	A or B	(1)	(1)	(1)	(1)		6.6	1.2	6.2	ns

(1) This information was not available at the time of publication.

Operating Characteristics

$T_A = 25°C$

PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\,V \pm 0.15\,V$	$V_{CC} = 2.5\,V \pm 0.2\,V$	$V_{CC} = 3.3\,V \pm 0.3\,V$	UNIT
			TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per transceiver — Outputs enabled	f = 10 MHz	(1)	(1)	55	pF
	Outputs disabled		(1)	(1)	12	

(1) This information was not available at the time of publication.

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PARAMETER MEASUREMENT INFORMATION
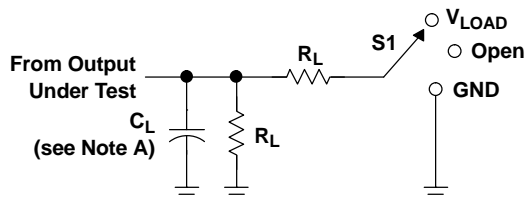
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	V_{CC}/2	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	V_{CC}/2	2 × V_{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
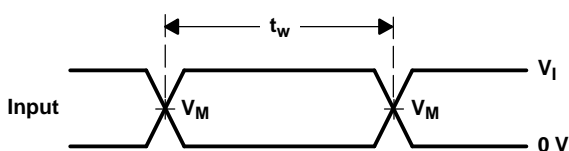
**VOLTAGE WAVEFORMS
PULSE DURATION**
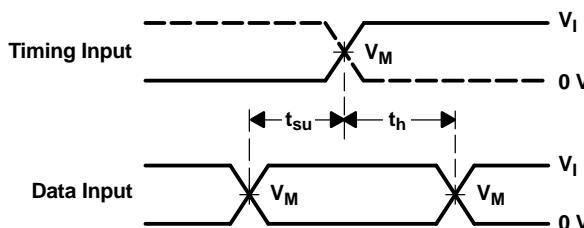
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**
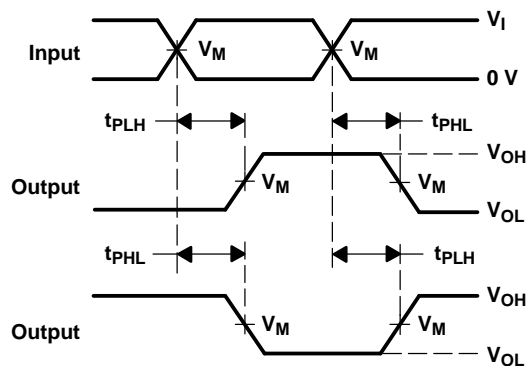
**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**
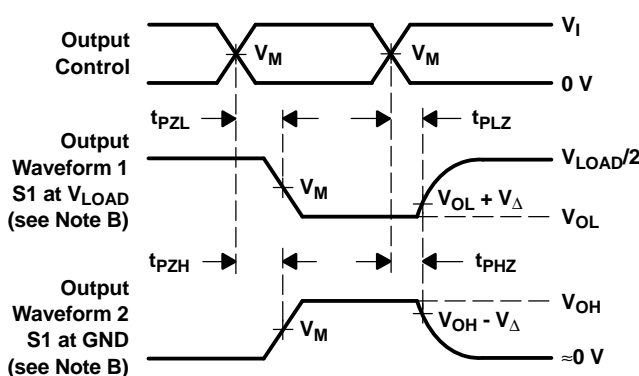
**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
CLVCH16652AIDGGREP	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04710-01XE	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVCH16652A-EP :
● Catalog: SN74LVCH16652A

NOTE: Qualified Version Definitions:
   ● Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

Q1 Q2 Q1 Q2
Q3 Q4 Q3 Q4

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLVCH16652AIDGGREP	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLVCH16652AIDGGREP	TSSOP	DGG	56	2000	346.0	346.0	41.0

DGG (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

	PINS **	48	56	64
DIM				
A MAX		12,60	14,10	17,10
A MIN		12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

TEXAS
INSTRUMENTS
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